



OMAP5432 Multimedia Device

ECCN: 3E991

1 Device Overview

1.1 Features

- ARM® Dual Cortex™-A15 Microprocessor Subsystem
 - Up to 1.5 GHz
 - NEON™ SIMD coprocessor and VFPv4
 - 2-MiB Unified L2 Cache Memory
 - 6 Power Domains
- IVA-HD Hardware Accelerator Subsystem
- ARM Dual Cortex™-M4 Image Processing Unit (IPU)
 - Dual-core, 200 MHz per Core
- On-Chip Debug with 14-Pin JTAG and CTools Technologies
- Display Subsystem
 - Display Controller with DMA Engine
 - Support for 3 LCD Outputs and 1 TV
 - 3 Video, 1 GFX, and 1 Write-back Pipeline
 - HDMI Encoder: HDMI 1.4a, HDCP 1.4, and DVI 1.0 Compliant
- Dual-Core PowerVR® SGX544™ 3D GPU
- 2D-Graphics Accelerator (BB2D) Subsystem
 - Vivante™ GC320 Core
- Imaging Subsystem (ISS), Consisting of Image Signal Processor (ISP) and Still Image Coprocessor (SIMCOP) Block
- Face Detection Interface (FDIF)
- Power-Independent Audio Back-End (ABE) Subsystem
- Level 3 (L3) and Level 4 (L4) Interconnects
- DDR3/DDR3L Memory Interface (EMIF) Module
 - Up to 4 GiB of SDRAM per EMIF (2 GiB per Chip Select)
- General-Purpose Memory Controller (GPMC)
- System Direct Memory Access (DMA) Controller
- Five High-Speed Inter-Integrated Circuit (I²C) Ports
- HDQ™/1-Wire® Interface
- 5 Configurable UART/IrDA/CIR Modules
- 4 Multichannel Serial Peripheral Interfaces (MCSPIs)
- Multichannel Buffered Serial Port (MCBSP)
- Multichannel Pulse Density Modulation (MCPDM)
- Multichannel Audio Serial Port (MCASP)
- 6-Path Digital Microphone (DMIC) Module
- MIPI® High-Speed Synchronous Serial Interface (HSI)
- High-Speed (HS) Multiport USB Host Subsystem
- SATA Host Controller and Physical Layer (PHY)
- MMC/SDIO Host Controller
- SuperSpeed (SS) USB OTG Subsystem and USB3 PHY
- Up to 256 General-Purpose I/O (GPIO) Pins
- 11 General-Purpose Timers
- 2 Watchdog Timers
- 32-kHz Synchronized Timer
- Power, Reset, and Clock Management
 - Multiple Independent Core Power Domains
 - Multiple Independent Core Voltage Domains
 - Module-Level Clock Management for Dynamic Reduction of Consumption
 - Available TI Clock Tree Tool (CTT) for Interactive Clock Tree Configuration
- Package
 - 754 Device Pins
 - Ball Grid Array (BGA)
 - 0.5-mm Ball Pitch



1.2 Applications

- Industrial Automation
- Automotive Infotainment
- Cloud Computing
- Touchscreens

1.3 Description

OMAP5432 devices are known for their low power consumption in tandem with best-in-class performance, supporting high-level operating systems, such as Linux® and Android™. Based on the Cortex-A15 core, OMAP5432 includes graphics and display accelerators for multimedia images in several mediums and supports a diversity of application requirements.

OMAP5 smart multicore processors employ two ARM Cortex-M4 cores to offload real-time control processing from the two main ARM Cortex-A15 cores of the processor. The architecture also integrates unique programmable accelerators—an embedded DSP, imaging and vision IMX accelerator, and display controller—that provide greater flexibility and future-proofing compared to hardwired accelerators. Dual-channel DDR3 memory provides bandwidth to support high-definition multimedia and displays.

The device also combines programmable video processing with a highly integrated peripheral set.

Device Information

| PART NUMBER | PACKAGE | BODY SIZE |
|-------------|-------------|-------------------|
| OMAP5432 | FCBGA (754) | 17.0 mm x 17.0 mm |

1.4 Functional Block Diagram

[Figure 1-1](#) is a block diagram for the OMAP5432 device.

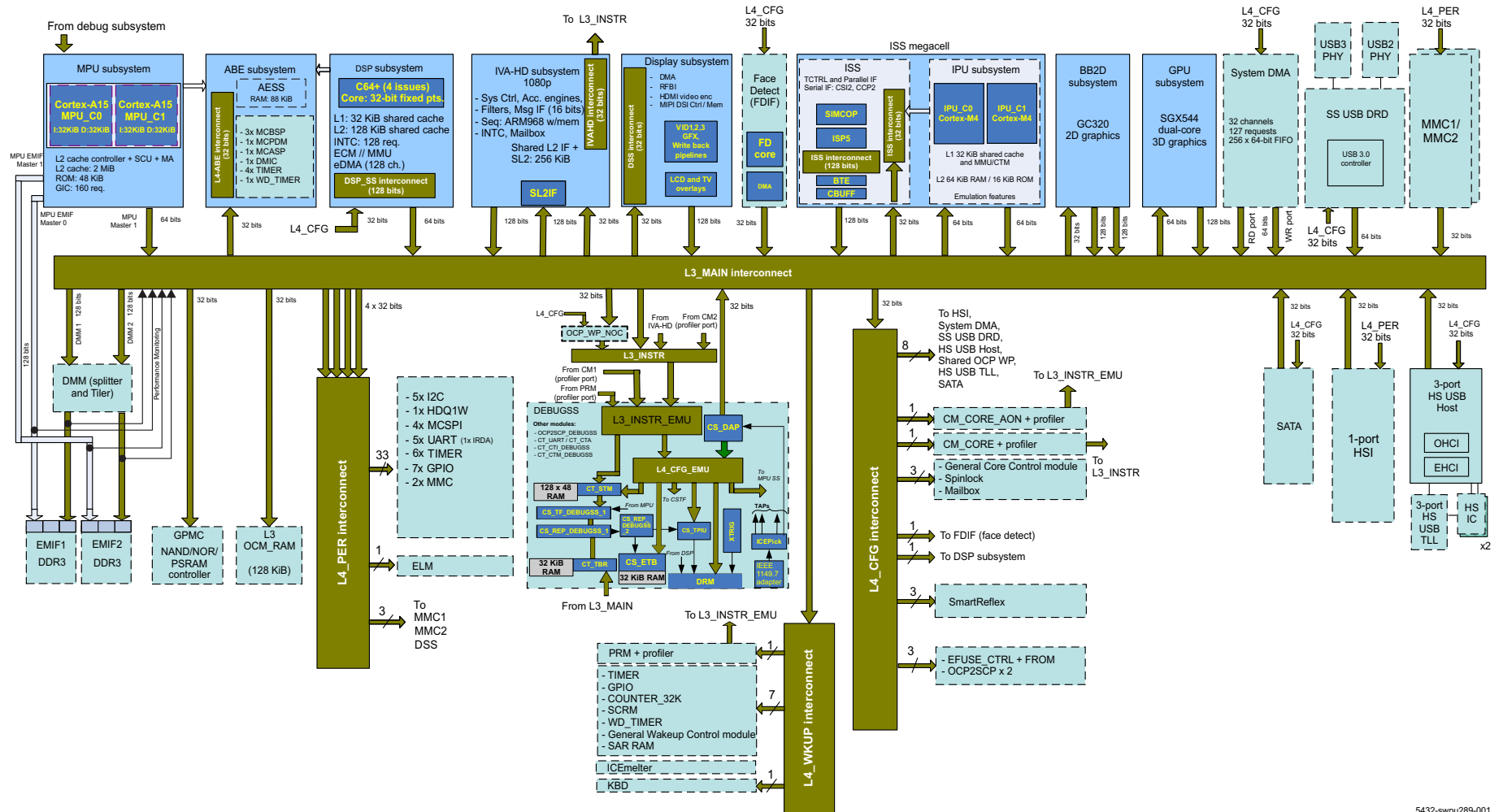


Figure 1-1. OMAP5432 Block Diagram

5432-swpu289-001

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

The following table summarizes the device Data Manual versions.

Revision History

| Version | Literature Number | Date | Notes |
|---------|-------------------|----------------|----------|
| A | SWPS051 | November 2012 | See (1) |
| B | SWPS051 | February 2013 | See (2) |
| C | SWPS051 | March 2013 | See (3) |
| D | SWPS051 | April 2013 | See (4) |
| E | SWPS051 | May 2013 | See (5) |
| F | SWPS051 | April 2014 | See (6) |
| G | SWPS051 | July 2014 | See (7) |
| H | SWPS051 | August 2014 | See (8) |
| I | SWPS051 | September 2014 | See (9) |
| J | SWPS051 | January 2015 | See (10) |
| K | SWPS051 | October 2015 | See (11) |

- (1) *OMAP5432 Multimedia Device Silicon Revision 2.0 Data Manual* - version A - DRAFT Book release.
- (2) *OMAP5432 Multimedia Device Silicon Revision 2.0 Data Manual* - version B - Early Preliminary Book release. In this version are updated the following chapters: Chapter 2 - Terminal Descriptions, Chapter 3 - Electrical Characteristics, Chapter 4 - Clock Specifications, Chapter 5 - Timing Requirements and Switching Characteristics and Chapter 8 - PCB Guidelines.
- (3) *OMAP5432 Multimedia Device Silicon Revision 2.0 Data Manual* - version C - Preliminary Book release. In this version are updated the following chapters : Chapter 8 - PCB Guidelines.
- (4) *OMAP5432 Multimedia Device Silicon Revision 2.0 Data Manual* - version D - Preliminary Book release. In this version are updated the following chapters : Chapter 8 - PCB Guidelines.
- (5) *OMAP5432 Multimedia Device Silicon Revision 2.0 Data Manual* - version E - Preliminary Book release. In this version are updated the following chapters : Chapter 7 - Package Characteristics.
- (6) *OMAP5432 Multimedia Device Silicon Revision 2.0 Data Manual* - version F - Preliminary Book release. In this version are updated the following chapters : Chapter 1 Introduction, Chapter 2 - Terminal Descriptions, Chapter 3 - Electrical Characteristics, Chapter 4 - Clock Specifications, Chapter 5 - Timing Requirements and Switching Characteristics, Chapter 6 - Thermal Management, Chapter 7 - Package Characteristics, and Chapter 8 - PCB Guidelines.
- (7) *OMAP5432 Multimedia Device Silicon Revision 2.0 Data Manual* - version G - Preliminary Book release. In this version are updated the following chapters : Chapter 3 - Terminal Configuration and Functions, Chapter 4 - Specifications and Chapter 6 - Timing Requirements and Switching Characteristics.
- (8) *OMAP5432 Multimedia Device Silicon Revision 2.0 Data Manual* - version H - Final Book release. In this version are updated the following chapters : Chapter 3 - Terminal Configuration and Functions, Chapter 4 - Specifications and Chapter 6 - Timing Requirements and Switching Characteristics, Chapter 7 - Applications, Implementation, and Layout
- (9) *OMAP5432 Multimedia Device Silicon Revision 2.0 Data Manual* - version I - Final Book release. In this version are updated the following chapters: Chapter 8: Device and Documentation support -[Section 8.1.2, Device Nomenclature](#).
- (10) *OMAP5432 Multimedia Device Silicon Revision 2.0 Data Manual* - version J - Final Book release. In this version are updated the following chapters: Chapter 4: Specifications -[Section 4.3, Operating Performance Points](#).
- (11) *OMAP5432 Multimedia Device Silicon Revision 2.0 Data Manual* - version K - Final Book release. In this version are updated the following chapters: Chapter 8 Device and Documentation Support and Chapter 9 Mechanical Packaging and Orderable Information

3 Terminal Configuration and Functions

3.1 Terminal Assignment

Figure 3-1 shows the ball locations for the 754-ball plastic ball grid array (PBGA) package and are used in conjunction with Table 3-1 through Table 3-39 to locate signal names and ball grid numbers.

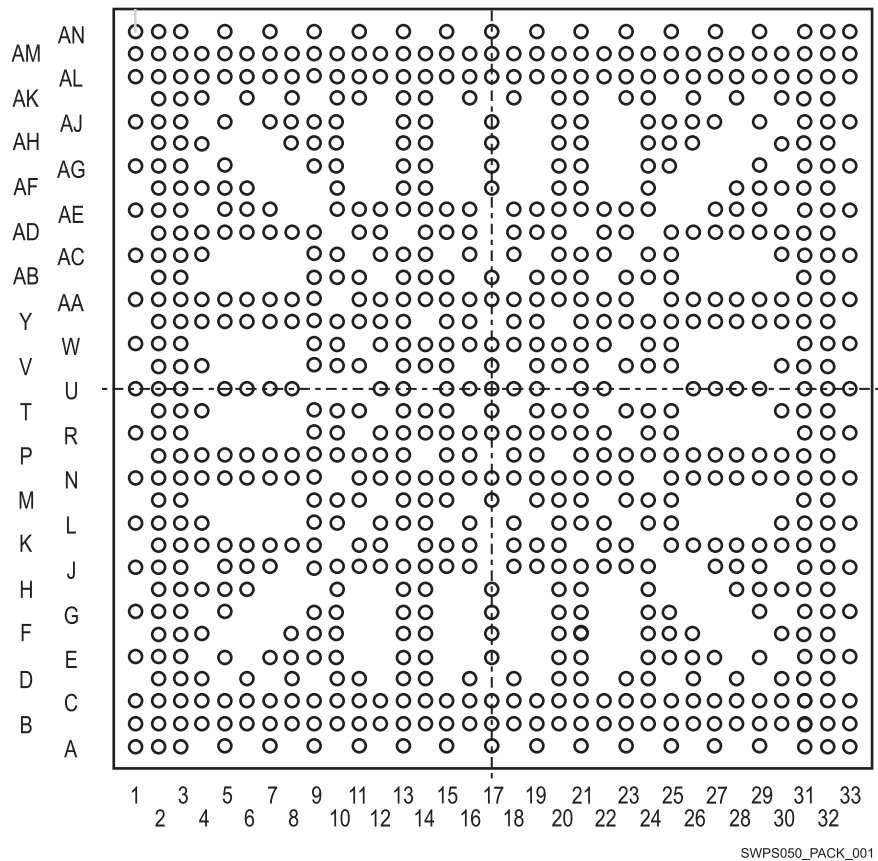


Figure 3-1. OMAP5432 AAN S-PBGA-N754 Package (Bottom View)

NOTE

The following bottom balls are not connected: A1 / A2 / AM33 / AN32 / AN33.

These balls can be connected to VSS if desired.

NOTE

The following bottom balls are reserved: AN2 / AD8 / K7 / AA8 / U7 / G10 / P27 / G17 / G25 / AN1 / B1 / AC33 / AG33 / AL22 / AM28 / AN27 / AM1 / AF14 / AG14 / AJ14 / AH14 / AG13 / AF13 / AH13 / AJ13.

These balls must be left unconnected.

NOTE

The following bottom balls are reserved: AJ17 / AK18 / AK16 / AF17 / H14.

These balls must be grounded.

3.2 Ball Characteristics

Table 3-1 describes the terminal characteristics and the signals multiplexed on each ball. The following list describes the table column headers:

1. **BALL BOTTOM:** Ball number(s) on the bottom side associated with each signal on the bottom.
2. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in mode 0).

NOTE

Table 3-1 does not take into account the subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 3.4, *Signal Descriptions*.

NOTE

In the safe_mode, the buffer is configured in high-impedance.

3. **MODE:** Multiplexing mode number:
 - (a) Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the ball corresponds to the name of the ball. There is always a function mapped on the primary mode. The primary mode is not necessarily the default mode.

NOTE

The default mode is the mode at the release of the reset; also see the RESET REL. MODE column.

- (b) Modes 1 through 7 are possible modes for alternate functions. On each ball, some modes are effectively used for alternate functions, while some modes are not used and correspond to a safe mode per design implementation.
4. **TYPE:** Signal type and direction:
 - I = Input
 - O = Output
 - IO = Input or Output
 - D = Open drain
 - DS = Differential
 - A = Analog
 - PWR = Power
 - GND = Ground
5. **BALL RESET STATE:** The state of the terminal at power-on reset:
 - 0: The buffer drives V_{OL} (pulldown or pullup resistor not activated).
 - 1: The buffer drives V_{OH} (pulldown or pullup resistor not activated).
 - Z: High-impedance
 - L: High-impedance with an active pulldown resistor
 - H: High-impedance with an active pullup resistor
6. **BALL RESET REL. STATE:** The state of the terminal at the release of the system control module reset (PRCM CORE_PWRON_RET_RST reset signal).
 - 0: The buffer drives V_{OL} (pulldown or pullup resistor not activated).
 - 1: The buffer drives V_{OH} (pulldown or pullup resistor not activated).
 - Z: High-impedance
 - L: High-impedance with an active pulldown resistor
 - H: High-impedance with an active pullup resistor

NOTE

For more information on the CORE_PWRON_RET_RST reset signal and its reset sources, see the Power Reset and Clock Management / PRCM Reset Management Functional Description section of the Device TRM.

7. **RESET REL. MODE:** This mode is automatically configured at the release of the system control module reset (PRCM CORE_PWRON_RET_RST reset signal).
8. **IO VOLTAGE VALUE:** This column describes the IO voltage value (VDDS supply).
9. **POWER NAME:** The voltage supply that powers the terminal IO buffers.
10. **SECOND POWER AVAIL.:** Some Device IOs have a second power supply signal (vdds_1p8) to ensure the VDDS ramping.
11. **HYS:** Indicates if the input buffer is with hysteresis:
 - Yes: With high hysteresis
 - No: Without low hysteresis

NOTE

For more information, see the hysteresis values in [Section 4.4, Electrical Characteristics](#).

12. **BUFFER STRENGTH:** Drive strength of the associated output buffer.

NOTE

For programmable buffer strength:

- The default value is given in [Table 3-1](#).
- A note describes all possible values according to the selected mode.

13. **PULLUP/DOWN – TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

NOTE

The pullup/pulldown drive strength is equal to: minimum = 50 μ A, typical = 100 μ A, maximum = 250 μ A, unless otherwise specified.

14. **IO CELL:** IO cell information:
 - LVCMOS: The IO buffer receives or drives a standard GPIO signal.
 - BK: This symbol underlines that this IO supports a bus keeper (or bus holder) function. It allows the output buffer to maintain the last state driven by using an internal pullup or pulldown resistor.
 - I²C Open Drain: The IO buffer outputs an open drain signal. This IO is designed for I²C function.
 - LVCMOS 3-State Open Drain: That indicates that the IO is a standard LVCMOS buffer that is used in the 3-state mode to have an open drain driver.
 - MPHY: This I/O supports MIPI M-PHY signals.
 - DPHY: This IO supports MIPI D-PHY signals.
 - Analog: For analog signals.
 - DDR: This IO can support DDR3 and DDR3L and HSUL_12 (HSIC) protocols.
 - SATAPHY: This IO supports SATA PHY signals.
 - USB3PHY: This IO supports USB3 PHY signals.
 - HDMIPHY: For IO buffer that supports HDMI PHY signals.

NOTE

Configuring two balls to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration. (safe_mode is not an input signal.)

NOTE

When a pad is set into a multiplexing mode which is not defined by ball multiplexing, this pad is actually set undriven (high impedance: Z) with potential pullup or pulldown resistors. Pulls need to be disabled to have a pure high impedance.

NOTE

All balls not described in [Table 3-1](#) are not connected.

Table 3-1. Ball Characteristics⁽¹⁾

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|--|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| H20 / J23 / J22 / J14 / J13 / J12 / L9 / M9 / P26 / P25 / R25 / U27 / U26 / W25 / Y25 / Y9 / AA25 / AA9 / AB25 / AC25 / AC9 / AD25 / AE24 / AE21 / AE15 / AE14 / AE13 / AF21 / U28 | vdds_1p8 | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| AB9 | vdds_emmc | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| AJ10 | emmc_clk | 0 | O | H | 0 | 0 | 1.8 V or 1.2 V | vdds_emmc | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpio2_46 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AH10 | emmc_cmd | 0 | IO | H | H | 0 | 1.8 V or 1.2 V | vdds_emmc | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpio2_47 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AG10 | emmc_data0 | 0 | IO | H | L | 0 | 1.8 V or 1.2 V | vdds_emmc | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpio2_48 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AF10 | emmc_data1 | 0 | IO | H | L | 0 | 1.8 V or 1.2 V | vdds_emmc | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpio2_49 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AH9 | emmc_data2 | 0 | IO | H | L | 0 | 1.8 V or 1.2 V | vdds_emmc | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpio2_50 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AJ9 | emmc_data3 | 0 | IO | H | L | 0 | 1.8 V or 1.2 V | vdds_emmc | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpio2_51 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AG9 | emmc_data4 | 0 | IO | H | L | 0 | 1.8 V or 1.2 V | vdds_emmc | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpio2_52 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AJ8 | emmc_data5 | 0 | IO | H | L | 0 | 1.8 V or 1.2 V | vdds_emmc | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpio2_53 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AH8 | emmc_data6 | 0 | IO | H | L | 0 | 1.8 V or 1.2 V | vdds_emmc | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpio2_54 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AJ7 | emmc_data7 | 0 | IO | H | L | 0 | 1.8 V or 1.2 V | vdds_emmc | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpio2_55 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| J21 / J20 | vdds_c2c | 0 | PWR | - | - | - | - | - | - | - | - | Power | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| J27 | Reserved | 0 | I | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | kbd_row0 | 3 | I | | | | | | | | | | |
| | gpmc_ad0 | 4 | IO | | | | | | | | | | |
| | gpio2_37 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| H28 | Reserved | 0 | I | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | kbd_row1 | 3 | I | | | | | | | | | | |
| | gpmc_ad1 | 4 | IO | | | | | | | | | | |
| | gpio2_38 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| H29 | Reserved | 0 | I | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | kbd_row2 | 3 | I | | | | | | | | | | |
| | gpmc_ad2 | 4 | IO | | | | | | | | | | |
| | gpio2_39 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| G29 | Reserved | 0 | I | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | kbd_row3 | 3 | I | | | | | | | | | | |
| | gpmc_ad3 | 4 | IO | | | | | | | | | | |
| | gpio2_40 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| E29 | Reserved | 0 | I | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | kbd_row4 | 3 | I | | | | | | | | | | |
| | gpmc_ad4 | 4 | IO | | | | | | | | | | |
| | gpio2_41 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| E27 | Reserved | 0 | I | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | kbd_row5 | 3 | I | | | | | | | | | | |
| | gpmc_ad5 | 4 | IO | | | | | | | | | | |
| | gpio2_42 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| F26 | Reserved | 0 | I | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | kbd_row6 | 3 | I | | | | | | | | | | |
| | gpmc_ad6 | 4 | IO | | | | | | | | | | |
| | gpio2_43 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| E26 | Reserved | 0 | I | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | kbd_row7 | 3 | I | | | | | | | | | | |
| | gpmc_ad7 | 4 | IO | | | | | | | | | | |
| | gpio2_44 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| J28 | Reserved | 0 | I | L | 0 | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | kbd_row8 | 3 | I | | | | | | | | | | |
| | gpmc_clk | 4 | O | | | | | | | | | | |
| | gpio2_36 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| J29 | Reserved | 0 | I | L | 0 | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | gpmc_nwp | 4 | O | | | | | | | | | | |
| | gpmc_nbe1 | 5 | O | | | | | | | | | | |
| | gpio2_35 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| E25 | Reserved | 0 | O | L | 0 | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | gpmc_NAdv_ale | 4 | O | | | | | | | | | | |
| | gpio2_33 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| F25 | Reserved | 0 | O | L | 0 | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | kbd_col8 | 3 | O | | | | | | | | | | |
| | gpmc_nbe0_cle | 4 | O | | | | | | | | | | |
| | gpio2_34 | 6 | IO | | | | | | | | | | |
| J32 | Reserved | 0 | O | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | kbd_col0 | 3 | O | | | | | | | | | | |
| | gpmc_ad8 | 4 | IO | | | | | | | | | | |
| | hw_dbg16 | 5 | O | | | | | | | | | | |
| | gpio2_56 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| J33 | Reserved | 0 | O | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | kbd_col1 | 3 | O | | | | | | | | | | |
| | gpmc_ad9 | 4 | IO | | | | | | | | | | |
| | hw_dbg17 | 5 | O | | | | | | | | | | |
| | gpio2_57 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| H32 | Reserved | 0 | O | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | kbd_col2 | 3 | O | | | | | | | | | | |
| | gpmc_ad10 | 4 | IO | | | | | | | | | | |
| | hw_dbg18 | 5 | O | | | | | | | | | | |
| | gpio2_58 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| J31 | Reserved | 0 | O | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | kbd_col3 | 3 | O | | | | | | | | | | |
| | gpmc_ad11 | 4 | IO | | | | | | | | | | |
| | hw_dbg19 | 5 | O | | | | | | | | | | |
| | gpio2_59 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| G31 | Reserved | 0 | O | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | kbd_col4 | 3 | O | | | | | | | | | | |
| | gpmc_ad12 | 4 | IO | | | | | | | | | | |
| | hw_dbg20 | 5 | O | | | | | | | | | | |
| | gpio2_60 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| H31 | Reserved | 0 | O | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | kbd_col5 | 3 | O | | | | | | | | | | |
| | gpmc_ad13 | 4 | IO | | | | | | | | | | |
| | hw_dbg21 | 5 | O | | | | | | | | | | |
| | gpio2_61 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| G32 | Reserved | 0 | O | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | kbd_col6 | 3 | O | | | | | | | | | | |
| | gpmc_ad14 | 4 | IO | | | | | | | | | | |
| | hw_dbg22 | 5 | O | | | | | | | | | | |
| | gpio2_62 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| G33 | Reserved | 0 | O | L | L | 4 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | kbd_col7 | 3 | O | | | | | | | | | | |
| | gpmc_ad15 | 4 | IO | | | | | | | | | | |
| | hw_dbg23 | 5 | O | | | | | | | | | | |
| | gpio2_63 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| G24 | Reserved | 0 | IO | L | L | 7 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpmc_a16 | 4 | O | | | | | | | | | | |
| | hw_dbg24 | 5 | O | | | | | | | | | | |
| | gpio4_113 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| H24 | Reserved | 0 | IO | L | L | 7 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpmc_a17 | 4 | O | | | | | | | | | | |
| | hw_dbg25 | 5 | O | | | | | | | | | | |
| | gpio4_114 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| E24 | Reserved | 0 | IO | L | L | 7 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpmc_a18 | 4 | O | | | | | | | | | | |
| | hw_dbg26 | 5 | O | | | | | | | | | | |
| | gpio4_115 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| F24 | Reserved | 0 | IO | L | L | 7 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpmc_a19 | 4 | O | | | | | | | | | | |
| | hw_dbg27 | 5 | O | | | | | | | | | | |
| | gpio4_116 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| G21 | Reserved | 0 | IO | L | L | 7 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpmc_a20 | 4 | O | | | | | | | | | | |
| | hw_dbg28 | 5 | O | | | | | | | | | | |
| | gpio4_117 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| H21 | Reserved | 0 | IO | L | L | 7 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpmc_a21 | 4 | O | | | | | | | | | | |
| | hw_dbg29 | 5 | O | | | | | | | | | | |
| | gpio4_118 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| E21 | Reserved | 0 | IO | L | L | 7 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpmc_a22 | 4 | O | | | | | | | | | | |
| | hw_dbg30 | 5 | O | | | | | | | | | | |
| | gpio4_119 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| F21 | Reserved | 0 | IO | L | L | 7 | 1.8 V or 1.2 V | vdds_c2c | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpmc_a23 | 4 | O | | | | | | | | | | |
| | hw_dbg31 | 5 | O | | | | | | | | | | |
| | gpio4_120 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| P32 | reserved | 0 | O | H | 1 | 4 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpmc_ncs0 | 4 | O | | | | | | | | | | |
| | gpio2_32 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|---------------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| N27 | Reserved | 0 | O | H | H | 4 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | gpmc_wait0 | 4 | I | | | | | | | | | | |
| | gpio2_45 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| N29 | Reserved | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | hw_wkdbg13 | 5 | O | | | | | | | | | | |
| | gpio1_wk15 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| N28 | Reserved | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | hw_wkdbg14 | 5 | O | | | | | | | | | | |
| | gpio1_wk14 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| G20 | hsi2_caready | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | usbb1_ulpiphy_clk | 3 | I | | | | | | | | | | |
| | gpmc_wait1 | 4 | I | | | | | | | | | | |
| | gpio3_76 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| F20 | hsi2_acready | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | usbb1_ulpiphy_nxt | 3 | I | | | | | | | | | | |
| | gpmc_ncs1 ⁽¹³⁾ | 4 | O | | | | | | | | | | |
| | gpio3_77 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| F17 | hsi2_cawake | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | usbb1_ulpiphy_dir | 3 | I | | | | | | | | | | |
| | gpmc_a24 | 4 | O | | | | | | | | | | |
| | gpio3_78 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| E20 | hsi2_acwake | 0 | O | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | usbb1_ulpiphy_stp | 3 | O | | | | | | | | | | |
| | gpmc_a25 | 4 | O | | | | | | | | | | |
| | gpio3_79 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| E14 | hsi2_cafflag | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | usbb1_ulpiphy_data0 | 3 | IO | | | | | | | | | | |
| | gpmc_wait2 | 4 | I | | | | | | | | | | |
| | gpio3_80 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| F14 | hsi2_cadata | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | usbb1_ulpiphy_data1 | 3 | IO | | | | | | | | | | |
| | gpmc_ncs2 ⁽¹³⁾ | 4 | O | | | | | | | | | | |
| | gpio3_81 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| G14 | hsi2_acflag | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | usbb1_ulpiphy_data2 | 3 | IO | | | | | | | | | | |
| | gpmc_ncs3 ⁽¹³⁾ | 4 | O | | | | | | | | | | |
| | gpio3_82 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| E17 | hsi2_acdata | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | usbb1_ulpiphy_data3 | 3 | IO | | | | | | | | | | |
| | gpmc_ncs4 ⁽¹³⁾ | 4 | O | | | | | | | | | | |
| | gpio3_83 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|----------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|--------------------------|----------------|
| F13 | uart2_rts | 0 | O | H | 1 | 4 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVC MOS |
| | mcspi3_somi | 1 | IO | | | | | | | | | | |
| | usbb1_ulpi phy_data4 | 3 | IO | | | | | | | | | | |
| | gpmc_nwe | 4 | O | | | | | | | | | | |
| | hw_dbg16 | 5 | O | | | | | | | | | | |
| | gpio3_84 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| N9 | uart2_cts | 0 | I | H | 1 | 4 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVC MOS |
| | mcspi3_cs0 | 1 | IO | | | | | | | | | | |
| | usbb1_ulpi phy_data5 | 3 | IO | | | | | | | | | | |
| | gpmc_noe_nre | 4 | O | | | | | | | | | | |
| | hw_dbg17 | 5 | O | | | | | | | | | | |
| | gpio3_85 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| G13 | uart2_rx | 0 | I | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVC MOS |
| | mcspi3_simo | 1 | IO | | | | | | | | | | |
| | usbb1_ulpi phy_data6 | 3 | IO | | | | | | | | | | |
| | gpmc_ncs5 | 4 | O | | | | | | | | | | |
| | hw_dbg18 | 5 | O | | | | | | | | | | |
| | gpio3_86 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| E13 | uart2_tx | 0 | O | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVC MOS |
| | mcspi3_clk | 1 | IO | | | | | | | | | | |
| | usbb1_ulpi phy_data7 | 3 | IO | | | | | | | | | | |
| | gpmc_ncs6 | 4 | O | | | | | | | | | | |
| | hw_dbg19 | 5 | O | | | | | | | | | | |
| | gpio3_87 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| N26 | vdds_hsic | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| K28 | usbb2_hsic_strobe | 0 | IO | L | L | 7 | 1.2 V | vdds_hsic | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| | gpio3_94 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| K29 | usbb2_hsic_data | 0 | IO | L | L | 7 | 1.2 V | vdds_hsic | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| | gpio3_95 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| W31 | timer10_pwm_evt | 0 | IO | L | L | 7 | 1.8 V or 1.2 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVC MOS |
| | gpio6_188 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| W33 | dsiporta_te0 | 0 | I | L | L | 7 | 1.8 V or 1.2 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVC MOS |
| | gpio6_189 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AA33 | vdda_dsiporta | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| Y30 | vssa_dsiporta | 0 | GND | - | - | - | - | - | - | - | - | - | - |
| AD31 | dsiporta_lane0x | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiporta | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AD32 | dsiporta_lane0y | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiporta | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AC31 | dsiporta_lane1x | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiporta | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AC32 | dsiporta_lane1y | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiporta | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AB32 | dsiporta_lane2x | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiporta | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AB31 | dsiporta_lane2y | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiporta | No | No | See ⁽¹⁵⁾ | No | DPHY |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|-------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| AA32 | dsiporta_lane3x | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiporta | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AA31 | dsiporta_lane3y | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiporta | No | No | See ⁽¹⁵⁾ | No | DPHY |
| Y32 | dsiporta_lane4x | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiporta | No | No | See ⁽¹⁵⁾ | No | DPHY |
| Y31 | dsiporta_lane4y | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiporta | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AJ33 | timer9_pwm_evt | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | sync_sof_clk | 1 | O | | | | | | | | | | |
| | sync_usof_itp_clk | 2 | O | | | | | | | | | | |
| | gpio6_190 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AK30 | dsiportc_te0 | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | gpio6_191 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AE33 | vdda_dsiportc | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| AD30 | vssa_dsiportc | 0 | GND | - | - | - | - | - | - | - | - | - | Power |
| AJ31 | dsiportc_lane0x | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiportc | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AJ32 | dsiportc_lane0y | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiportc | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AH32 | dsiportc_lane1x | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiportc | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AH31 | dsiportc_lane1y | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiportc | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AG32 | dsiportc_lane2x | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiportc | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AG31 | dsiportc_lane2y | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiportc | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AF32 | dsiportc_lane3x | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiportc | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AF31 | dsiportc_lane3y | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiportc | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AE32 | dsiportc_lane4x | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiportc | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AE31 | dsiportc_lane4y | 0 | ODS | 0 | L | 0 | 1.8 V or 1.5 V | vdda_dsiportc | No | No | See ⁽¹⁵⁾ | No | DPHY |
| AN13 | rfbi_hsync0 | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data17 | 3 | O | | | | | | | | | | |
| | kbd_col5 | 4 | O | | | | | | | | | | |
| | gpio6_160 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AM13 | rfbi_te_vsync0 | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data16 | 3 | O | | | | | | | | | | |
| | kbd_row5 | 4 | I | | | | | | | | | | |
| | jtag_sel | 5 | I | | | | | | | | | | |
| | gpio6_161 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AL18 | rfbi_re | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_pclk | 3 | O | | | | | | | | | | |
| | kbd_col4 | 4 | O | | | | | | | | | | |
| | gpio6_164 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AM18 | rfbi_a0 | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_de | 3 | O | | | | | | | | | | |
| | kbd_row4 | 4 | I | | | | | | | | | | |
| | gpio6_165 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| AL14 | rfbi_data8 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data8 | 3 | O | | | | | | | | | | |
| | kbd_col3 | 4 | O | | | | | | | | | | |
| | drm_emu12 | 5 | O | | | | | | | | | | |
| | gpio6_174 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| AM14 | rfbi_data9 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data9 | 3 | O | | | | | | | | | | |
| | kbd_row3 | 4 | I | | | | | | | | | | |
| | drm_emu13 | 5 | O | | | | | | | | | | |
| | gpio6_175 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| AM12 | rfbi_data10 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data10 | 3 | O | | | | | | | | | | |
| | kbd_row8 | 4 | I | | | | | | | | | | |
| | drm_emu14 | 5 | O | | | | | | | | | | |
| | gpio6_176 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| AL11 | rfbi_data11 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data11 | 3 | O | | | | | | | | | | |
| | kbd_row7 | 4 | I | | | | | | | | | | |
| | drm_emu15 | 5 | O | | | | | | | | | | |
| | gpio6_177 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| AM11 | rfbi_data12 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data12 | 3 | O | | | | | | | | | | |
| | kbd_row6 | 4 | I | | | | | | | | | | |
| | drm_emu16 | 5 | O | | | | | | | | | | |
| | gpio6_178 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| AN11 | rfbi_data13 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data13 | 3 | O | | | | | | | | | | |
| | kbd_col8 | 4 | O | | | | | | | | | | |
| | drm_emu17 | 5 | O | | | | | | | | | | |
| | gpio6_179 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| AL10 | rfbi_data14 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data14 | 3 | O | | | | | | | | | | |
| | kbd_col7 | 4 | O | | | | | | | | | | |
| | drm_emu18 | 5 | O | | | | | | | | | | |
| | gpio6_180 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| AM10 | rfbi_data15 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | mcspi2_cs1 | 1 | O | | | | | | | | | | |
| | dispc_data15 | 3 | O | | | | | | | | | | |
| | kbd_col6 | 4 | O | | | | | | | | | | |
| | drm_emu19 | 5 | O | | | | | | | | | | |
| | gpio6_181 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|---------------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| AN9 | gpio6_182 ⁽¹⁰⁾ | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data18 | 3 | O | | | | | | | | | | |
| | kbd_col0 | 4 | O | | | | | | | | | | |
| | gpio6_182 ⁽¹⁰⁾ | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AM9 | gpio6_183 ⁽¹⁰⁾ | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data19 | 3 | O | | | | | | | | | | |
| | kbd_col1 | 4 | O | | | | | | | | | | |
| | gpio6_183 ⁽¹⁰⁾ | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AL9 | gpio6_184 ⁽¹⁰⁾ | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data20 | 3 | O | | | | | | | | | | |
| | kbd_col2 | 4 | O | | | | | | | | | | |
| | hw_dbg22 | 5 | O | | | | | | | | | | |
| | gpio6_184 ⁽¹⁰⁾ | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AM8 | gpio6_185 ⁽¹⁰⁾ | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data21 | 3 | O | | | | | | | | | | |
| | kbd_row0 | 4 | I | | | | | | | | | | |
| | hw_dbg23 | 5 | O | | | | | | | | | | |
| | gpio6_185 ⁽¹⁰⁾ | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AL8 | gpio6_186 ⁽¹⁰⁾ | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data22 | 3 | O | | | | | | | | | | |
| | kbd_row1 | 4 | I | | | | | | | | | | |
| | hw_dbg24 | 5 | O | | | | | | | | | | |
| | gpio6_186 ⁽¹⁰⁾ | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AN7 | gpio6_187 ⁽¹⁰⁾ | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data23 | 3 | O | | | | | | | | | | |
| | kbd_row2 | 4 | I | | | | | | | | | | |
| | hw_dbg25 | 5 | O | | | | | | | | | | |
| | gpio6_187 ⁽¹⁰⁾ | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AL17 | rffi_data0 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data0 | 3 | O | | | | | | | | | | |
| | jtagtapext_rtck | 4 | I | | | | | | | | | | |
| | drm_emu4 | 5 | O | | | | | | | | | | |
| | gpio6_166 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AM17 | rffi_data1 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data1 | 3 | O | | | | | | | | | | |
| | uart3_rx_irrx | 4 | I | | | | | | | | | | |
| | drm_emu5 | 5 | O | | | | | | | | | | |
| | gpio6_167 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AN17 | rffi_data2 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data2 | 3 | O | | | | | | | | | | |
| | uart3_tx_irtx | 4 | O | | | | | | | | | | |
| | drm_emu6 | 5 | O | | | | | | | | | | |
| | gpio6_168 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| AL16 | rubi_data3 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data3 | 3 | O | | | | | | | | | | |
| | jtagtapext_nrst | 4 | O | | | | | | | | | | |
| | drm_emu7 | 5 | O | | | | | | | | | | |
| | gpio6_169 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AM16 | rubi_data4 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data4 | 3 | O | | | | | | | | | | |
| | jtagtapext_tck | 4 | O | | | | | | | | | | |
| | drm_emu8 | 5 | O | | | | | | | | | | |
| | gpio6_170 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AL15 | rubi_data5 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data5 | 3 | O | | | | | | | | | | |
| | jtagtapext_tmisc | 4 | O | | | | | | | | | | |
| | drm_emu9 | 5 | O | | | | | | | | | | |
| | gpio6_171 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AM15 | rubi_data6 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data6 | 3 | O | | | | | | | | | | |
| | jtagtapext_tdo | 4 | O | | | | | | | | | | |
| | drm_emu10 | 5 | O | | | | | | | | | | |
| | gpio6_172 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AN15 | rubi_data7 | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_data7 | 3 | O | | | | | | | | | | |
| | jtagtapext_tdi | 4 | I | | | | | | | | | | |
| | drm_emu11 | 5 | O | | | | | | | | | | |
| | gpio6_173 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AL13 | rubi_cs0 | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_hsync | 3 | O | | | | | | | | | | |
| | drm_emu3 | 5 | O | | | | | | | | | | |
| | gpio6_163 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AL12 | rubi_we | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | dispc_vsync | 3 | O | | | | | | | | | | |
| | drm_emu2 | 5 | O | | | | | | | | | | |
| | gpio6_162 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AF20 | mcspi2_cs0 | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | jtagtapext_nrst | 1 | O | | | | | | | | | | |
| | dispc_fid | 3 | O | | | | | | | | | | |
| | gpio7_196 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AH17 | mcspi2_clk | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | jtagtapext_tck | 1 | O | | | | | | | | | | |
| | gpio7_197 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-------------------------------|---------------------------------------|
| AG20 | mcspi2_simo | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | jtagtapext_tmisc | 1 | O | | | | | | | | | | |
| | hw_dbg20 | 5 | O | | | | | | | | | | |
| | gpio7_198 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AH20 | mcspi2_somi | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | jtagtapext_tdo | 1 | O | | | | | | | | | | |
| | hw_dbg21 | 5 | O | | | | | | | | | | |
| | gpio7_199 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AJ21 | i2c4_scl | 0 | IOD | H | H | 7 | 1.8 V | vdds_1p8 | Yes | No | 3 | PUx / PDy-GPIO ⁽⁴⁾ | LVCMOS I ² C Open Drain |
| | jtagtapext_tdi | 1 | I | | | | | | | | | | |
| | gpio7_200 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AJ20 | i2c4_sda | 0 | IOD | H | H | 7 | 1.8 V | vdds_1p8 | Yes | No | 3 | PUx / PDy-GPIO ⁽⁴⁾ | LVCMOS I ² C Open Drain |
| | jtagtapext_rtck | 1 | I | | | | | | | | | | |
| | gpio7_201 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AE23 | vdds_hdmi | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| AN23 | hdmi_cec | 0 | IOD | H | H | 7 | 1.8 V or 1.2 V | vdds_hdmi | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS Tri-State Open Drain |
| | gpio7_192 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AM23 | hdmi_hpd | 0 | I | L | L | 7 | 1.8 V or 1.2 V | vdds_hdmi | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | gpio7_193 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AM22 | hdmi_ddc_scl | 0 | IOD | H | H | 7 | 1.8 V or 1.2 V | vdds_hdmi | Yes | No | 3 | PUx / PDy-OD ⁽⁴⁾ | LVCMOS I ² C Open Drain |
| | gpio7_194 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AL23 | hdmi_ddc_sda | 0 | IOD | H | H | 7 | 1.8 V or 1.2 V | vdds_hdmi | Yes | No | 3 | PUx / PDy-OD ⁽⁴⁾ | LVCMOS I ² C Open Drain |
| | gpio7_195 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AN25 | vdda_hdmi | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| AK24 | vssa_hdmi | 0 | GND | - | - | - | - | - | - | - | - | - | Power |
| AL24 | hdmi_clkx | 0 | ODS | Z | Z | 0 | 1.8 V or 1.5 V | vdda_hdmi | No | No | 10 | PDy ⁽⁵⁾ | HDMIPHY |
| AM24 | hdmi_clkx | 0 | ODS | Z | Z | 0 | 1.8 V or 1.5 V | vdda_hdmi | No | No | 10 | PDy ⁽⁵⁾ | HDMIPHY |
| AL25 | hdmi_data0x | 0 | ODS | Z | Z | 0 | 1.8 V or 1.5 V | vdda_hdmi | No | No | 10 | PDy ⁽⁵⁾ | HDMIPHY |
| AM25 | hdmi_data0y | 0 | ODS | Z | Z | 0 | 1.8 V or 1.5 V | vdda_hdmi | No | No | 10 | PDy ⁽⁵⁾ | HDMIPHY |
| AL26 | hdmi_data1x | 0 | ODS | Z | Z | 0 | 1.8 V or 1.5 V | vdda_hdmi | No | No | 10 | PDy ⁽⁵⁾ | HDMIPHY |
| AM26 | hdmi_data1y | 0 | ODS | Z | Z | 0 | 1.8 V or 1.5 V | vdda_hdmi | No | No | 10 | PDy ⁽⁵⁾ | HDMIPHY |
| AL27 | hdmi_data2x | 0 | ODS | Z | Z | 0 | 1.8 V or 1.5 V | vdda_hdmi | No | No | 10 | PDy ⁽⁵⁾ | HDMIPHY |
| AM27 | hdmi_data2y | 0 | ODS | Z | Z | 0 | 1.8 V or 1.5 V | vdda_hdmi | No | No | 10 | PDy ⁽⁵⁾ | HDMIPHY |
| N3 | vdda_csiporta | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| P4 | vssa_csiporta | 0 | GND | - | - | - | - | - | - | - | - | - | Power |
| U6 | csiporta_lane0x | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiporta | Yes | No | NA | PU/PD | DPHY |
| | cpi_pclk | 3 | I | | | | | | | | | | |
| | gpio8_in236 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| U5 | csiporta_lane0y | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiporta | Yes | No | NA | PU/PD | DPHY |
| | cpi_wen | 3 | I | | | | | | | | | | |
| | gpio8_in237 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| P5 | csiporta_lane1y | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiporta | Yes | No | NA | PU/PD | DPHY |
| | cpi_data0 | 3 | I | | | | | | | | | | |
| | gpio8_in238 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| P6 | csiporta_lane1x | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiporta | Yes | No | NA | PU/PD | DPHY |
| | cpi_data1 | 3 | I | | | | | | | | | | |
| | gpio8_in239 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| P8 | csiporta_lane2y | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiporta | Yes | No | NA | PU/PD | DPHY |
| | cpi_data2 | 3 | I | | | | | | | | | | |
| | gpio8_in240 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| P7 | csiporta_lane2x | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiporta | Yes | No | NA | PU/PD | DPHY |
| | cpi_data3 | 3 | I | | | | | | | | | | |
| | gpio8_in241 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| N5 | csiporta_lane3x | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiporta | Yes | No | NA | PU/PD | DPHY |
| | cpi_data4 | 3 | I | | | | | | | | | | |
| | gpio8_in242 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| N6 | csiporta_lane3y | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiporta | Yes | No | NA | PU/PD | DPHY |
| | cpi_data5 | 3 | I | | | | | | | | | | |
| | gpio8_in243 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| N7 | csiporta_lane4x | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiporta | Yes | No | NA | PU/PD | DPHY |
| | cpi_data6 | 3 | I | | | | | | | | | | |
| | gpio8_in244 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| N8 | csiporta_lane4y | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiporta | Yes | No | NA | PU/PD | DPHY |
| | cpi_data7 | 3 | I | | | | | | | | | | |
| | gpio8_in245 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AA7 | vdda_csiportb | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| Y4 | vssa_csiportb | 0 | GND | - | - | - | - | - | - | - | - | - | Power |
| Y6 | csiportb_lane0x | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiportb | Yes | No | NA | PU/PD | DPHY |
| | cpi_data12 | 4 | I | | | | | | | | | | |
| | gpio8_in246 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| Y5 | csiportb_lane0y | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiportb | Yes | No | NA | PU/PD | DPHY |
| | cpi_data13 | 4 | I | | | | | | | | | | |
| | gpio8_in247 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| Y7 | csiportb_lane1y | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiportb | Yes | No | NA | PU/PD | DPHY |
| | cpi_data14 | 4 | I | | | | | | | | | | |
| | gpio8_in248 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| Y8 | csiportb_lane1x | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiportb | Yes | No | NA | PU/PD | DPHY |
| | cpi_data15 | 4 | I | | | | | | | | | | |
| | gpio8_in249 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AA5 | csiportb_lane2y | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiportb | Yes | No | NA | PU/PD | DPHY |
| | cpi_hsyncin | 4 | I | | | | | | | | | | |
| | gpio8_in250 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AA6 | csiportb_lane2x | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiportb | Yes | No | NA | PU/PD | DPHY |
| | cpi_vsyncin | 4 | I | | | | | | | | | | |
| | gpio8_in251 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| J5 | vdda_csiportc | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| K4 | vssa_csiportc | 0 | GND | - | - | - | - | - | - | - | - | - | Power |
| J6 | csiportc_lane0y | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiportc | Yes | No | NA | PU/PD | DPHY |
| | cpi_data8 | 3 | I | | | | | | | | | | |
| | gpio8_in252 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| J7 | csiportc_lane0x | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiportc | Yes | No | NA | PU/PD | DPHY |
| | cpi_data9 | 3 | I | | | | | | | | | | |
| | gpio8_in253 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| K6 | csiportc_lane1y | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiportc | Yes | No | NA | PU/PD | DPHY |
| | cpi_data10 | 3 | I | | | | | | | | | | |
| | gpio8_in254 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| K5 | csiportc_lane1x | 0 | IDS | L | L | 7 | 1.8 V or 1.5 V | vdda_csiportc | Yes | No | NA | PU/PD | DPHY |
| | cpi_data11 | 3 | I | | | | | | | | | | |
| | gpio8_in255 | 6 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AE6 | cam_shutter | 0 | O | Z | Z | 5 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | sys_nodeid0 | 5 | I | | | | | | | | | | |
| | gpio8_224 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AE5 | cam_strobe | 0 | O | Z | Z | 5 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | sys_nodeid1 | 5 | I | | | | | | | | | | |
| | gpio8_225 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AF6 | cam_globalreset | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | cam_shutter | 1 | O | | | | | | | | | | |
| | cpi_fid | 3 | I | | | | | | | | | | |
| | gpio8_226 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AE7 | timer11_pwm_evt | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | uart1_tx | 2 | O | | | | | | | | | | |
| | cpi_data12 | 3 | I | | | | | | | | | | |
| | hw_dbg26 | 5 | O | | | | | | | | | | |
| | gpio8_227 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|---------------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-------------------------------|---------------------------------------|
| AD5 | timer5_pwm_evt | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | sdcard_cd ⁽¹⁴⁾ | 1 | I | | | | | | | | | | |
| | uart1_cts | 2 | I | | | | | | | | | | |
| | cpi_data13 | 3 | I | | | | | | | | | | |
| | gpio8_228 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| AD6 | timer6_pwm_evt | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | sdcard_wp ⁽¹⁴⁾ | 1 | I | | | | | | | | | | |
| | uart1_rx | 2 | I | | | | | | | | | | |
| | cpi_data14 | 3 | I | | | | | | | | | | |
| | gpio8_229 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| AD7 | timer8_pwm_evt | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | sdcard_wp ⁽¹⁴⁾ | 1 | I | | | | | | | | | | |
| | uart1_rts | 2 | O | | | | | | | | | | |
| | cpi_data15 | 3 | I | | | | | | | | | | |
| | hw_dbg27 | 5 | O | | | | | | | | | | |
| | gpio8_230 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| AJ5 | i2c3_scl | 0 | IOD | H | H | 7 | 1.8 V | vdds_1p8 | Yes | No | 3 | PUx / PDy-GPIO ⁽⁴⁾ | LVCMOS I ² C Open Drain |
| | gpio8_231 | 6 | IO | | | | | | | | 4 | | |
| | safe_mode | 7 | | | | | | | | | 4 | | |
| AH4 | i2c3_sda | 0 | IOD | H | H | 7 | 1.8 V | vdds_1p8 | Yes | No | 3 | PUx / PDy-GPIO ⁽⁴⁾ | LVCMOS I ² C Open Drain |
| | gpio8_232 | 6 | IO | | | | | | | | 4 | | |
| | safe_mode | 7 | | | | | | | | | 4 | | |
| AG5 | gpio8_233 ⁽¹⁰⁾ | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | sys_secure_indicator | 1 | O | | | | | | | | | | |
| | timer8_pwm_evt | 2 | IO | | | | | | | | | | |
| | cpi_hsync | 3 | IO | | | | | | | | | | |
| | gpio8_233 ⁽¹⁰⁾ | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| AF5 | gpio8_234 ⁽¹⁰⁾ | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | sys_drm_msecure | 1 | O | | | | | | | | | | |
| | cpi_vsync | 3 | IO | | | | | | | | | | |
| | gpio8_234 ⁽¹⁰⁾ | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| W32 | abe_clks | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | abemcasp_axr | 3 | IO | | | | | | | | | | |
| | gpio4_96 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AF28 | abedmic_din1 | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | abemcasp_ahclr | 3 | IO | | | | | | | | | | |
| | abemcbasp3_fsx | 4 | IO | | | | | | | | | | |
| | gpio4_97 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AE29 | abedmic_din2 | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | abemcasp_axr | 3 | IO | | | | | | | | | | |
| | abemcbasp3_dx | 4 | O | | | | | | | | | | |
| | gpio4_98 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|-------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| AE28 | abedmic_din3 | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | abemcbasp3_dr | 4 | I | | | | | | | | | | |
| | gpio4_99 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AE27 | abedmic_clk1 | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | abemcbasp3_clkx | 4 | IO | | | | | | | | | | |
| | gpio4_100 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AD29 | abedmic_clk2 | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | abemcbasp1_fsx | 1 | IO | | | | | | | | | | |
| | abemcasp_amutein | 3 | I | | | | | | | | | | |
| | gpio4_101 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AD28 | abedmic_clk3 | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | abemcbasp1_dx | 1 | O | | | | | | | | | | |
| | abemcasp_aclkx | 3 | IO | | | | | | | | | | |
| | gpio4_102 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AF29 | reserved | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | abemcbasp1_clkx | 1 | IO | | | | | | | | | | |
| | abemcasp_afsr | 3 | IO | | | | | | | | | | |
| | gpio4_103 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AG29 | reserved | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS BK |
| | abemcbasp1_dr | 1 | I | | | | | | | | | | |
| | abemcasp_aclkr | 3 | IO | | | | | | | | | | |
| | gpio4_104 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AD26 | abemcbasp2_dr | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | abemcasp_axr | 3 | IO | | | | | | | | | | |
| | gpio4_105 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AD27 | abemcbasp2_dx | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | abemcasp_amuteout | 3 | O | | | | | | | | | | |
| | gpio4_106 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AA26 | abemcbasp2_fsx | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | abemcasp_afsx | 3 | IO | | | | | | | | | | |
| | gpio4_107 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AA27 | abemcbasp2_clkx | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | abemcasp_ahclkx | 3 | IO | | | | | | | | | | |
| | gpio4_108 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AA28 | abemcpdm_ul_data | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | abemcbasp3_dr | 1 | I | | | | | | | | | | |
| | abemcasp_axr3 | 3 | IO | | | | | | | | | | |
| | gpio4_109 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| AA29 | abemcpdm_dl_data | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | abemcbsp3_dx | 1 | O | | | | | | | | | | |
| | abemcasp_axr2 | 3 | IO | | | | | | | | | | |
| | gpio4_110 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| Y29 | abemcpdm_frame | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | abemcbsp3_clkx | 1 | IO | | | | | | | | | | |
| | abemcasp_axr1 | 3 | IO | | | | | | | | | | |
| | gpio4_111 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| Y28 | abemcpdm_lb_clk | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | abemcbsp3_fsx | 1 | IO | | | | | | | | | | |
| | gpio4_112 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AH25 | wlsdio_clk | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | mcspi4_clk | 1 | IO | | | | | | | | | | |
| | gpio5_128 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AG25 | wlsdio_cmd | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpio5_129 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AJ26 | wlsdio_data0 | 0 | IO | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | mcspi4_simo | 1 | IO | | | | | | | | | | |
| | gpio5_130 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AH26 | wlsdio_data1 | 0 | IO | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | mcspi4_somi | 1 | IO | | | | | | | | | | |
| | gpio5_131 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AK28 | wlsdio_data2 | 0 | IO | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | mcspi4_cs0 | 1 | IO | | | | | | | | | | |
| | gpio5_132 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AJ27 | wlsdio_data3 | 0 | IO | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | gpio5_133 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AL32 | uart5_rx | 0 | I | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | sdio4_data1 | 4 | IO | | | | | | | | | | |
| | hw_dbg28 | 5 | O | | | | | | | | | | |
| | gpio5_134 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AL31 | uart5_tx | 0 | O | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | sdio4_data2 | 4 | IO | | | | | | | | | | |
| | hw_dbg29 | 5 | O | | | | | | | | | | |
| | gpio5_135 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AK31 | uart5_cts | 0 | I | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | sdio4_data0 | 4 | IO | | | | | | | | | | |
| | hw_dbg30 | 5 | O | | | | | | | | | | |
| | gpio5_136 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] | |
|-----------------|--------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-------------------------------|---------------------------------------|---|
| AK32 | uart5_rts | 0 | O | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS | |
| | sdio4_data3 | 4 | IO | | | | | | | | | | | |
| | hw_dbg31 | 5 | O | | | | | | | | | | | |
| | gpio5_137 | 6 | IO | | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | | |
| AL33 | i2c2_scl | 0 | IOD | H | H | 7 | 1.8 V | vdds_1p8 | Yes | No | 3 | PUx / PDy-GPIO ⁽⁴⁾ | LVCMOS I ² C Open Drain | |
| | gpio5_138 | 6 | IO | | | | | | | | | | | 4 |
| | safe_mode | 7 | | | | | | | | | | | | 4 |
| AM32 | i2c2_sda | 0 | IOD | H | H | 7 | 1.8 V | vdds_1p8 | Yes | No | 3 | PUx / PDy-GPIO ⁽⁴⁾ | LVCMOS I ² C Open Drain | |
| | gpio5_139 | 6 | IO | | | | | | | | | | | 4 |
| | safe_mode | 7 | | | | | | | | | | | | 4 |
| AM30 | mcspi1_clk | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS | |
| | gpio5_140 | 6 | IO | | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | | |
| AL30 | mcspi1_somi | 0 | I | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS | |
| | usb0_ulpiphy_nxt | 5 | I | | | | | | | | | | | |
| | gpio5_141 | 6 | IO | | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | | |
| AL29 | mcspi1_simo | 0 | IO | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS | |
| | usb0_ulpiphy_dir | 5 | I | | | | | | | | | | | |
| | gpio5_142 | 6 | IO | | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | | |
| AN31 | mcspi1_cs0 | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS | |
| | usb0_ulpiphy_data0 | 5 | IO | | | | | | | | | | | |
| | gpio5_143 | 6 | IO | | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | | |
| AM31 | mcspi1_cs1 | 0 | O | L | L | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS | |
| | usb0_ulpiphy_data1 | 5 | IO | | | | | | | | | | | |
| | gpio5_144 | 6 | IO | | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | | |
| AL28 | i2c5_scl | 0 | IOD | H | H | 7 | 1.8 V | vdds_1p8 | Yes | No | 3 | PUx / PDy-GPIO ⁽⁴⁾ | LVCMOS I ² C Open Drain | |
| | uart4_rx | 2 | I | | | | | | | | | | | 4 |
| | gpio5_147 | 6 | IO | | | | | | | | | | | 4 |
| | safe_mode | 7 | | | | | | | | | | | | 4 |
| AM29 | i2c5_sda | 0 | IOD | H | H | 7 | 1.8 V | vdds_1p8 | Yes | No | 3 | PUx / PDy-GPIO ⁽⁴⁾ | LVCMOS I ² C Open Drain | |
| | uart4_tx | 2 | O | | | | | | | | | | | 4 |
| | gpio5_148 | 6 | IO | | | | | | | | | | | 4 |
| | safe_mode | 7 | | | | | | | | | | | | 4 |
| AN29 | uart6_rts | 0 | O | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS | |
| | sys_ndmareq0 | 1 | I | | | | | | | | | | | |
| | sdio5_data0 | 3 | IO | | | | | | | | | | | |
| | usbb2_mm_txse0 | 4 | IO | | | | | | | | | | | |
| | usb0_ulpiphy_stp | 5 | O | | | | | | | | | | | |
| | gpio5_152 | 6 | IO | | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | | |
| AJ25 | uart3_cts_rctx | 0 | IO | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS | |
| | sata_actled | 1 | O | | | | | | | | | | | |
| | sdio5_data7 | 3 | IO | | | | | | | | | | | |
| | usbb2_mm_txen | 4 | IO | | | | | | | | | | | |
| | usb0_ulpiphy_data4 | 5 | IO | | | | | | | | | | | |
| | gpio5_153 | 6 | IO | | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] ⁽²⁾ | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|------------------------------|----------|----------|----------------------|---------------------------|---------------------|-------------------------------------|----------------|--------------------------|--------------------|---------------------------|--------------------------|-----------------------------|
| AJ24 | uart3_rts_irsdc | 0 | O | H | H | 7 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS Tri-State Open Drain |
| | hdq_sio | 1 | IOD | | | | | | | | | | |
| | sdio5_data6 | 3 | IO | | | | | | | | | | |
| | usbb2_mm_txdat | 4 | IO | | | | | | | | | | |
| | usbd0_ulpiph_data5 | 5 | IO | | | | | | | | | | |
| | gpio5_154 | 6 | IO | | | | | | | | | | |
| safe_mode | 7 | | | | | | | | | | | | |
| AG24 | uart3_tx_irtx | 0 | O | H | H | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | sdio5_data5 | 3 | IO | | | | | | | | | | |
| | sdio4_clk | 4 | O | | | | | | | | | | |
| | usbd0_ulpiph_data6 | 5 | IO | | | | | | | | | | |
| | gpio5_155 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AH24 | uart3_rx_irtx | 0 | I | H | H | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | sdio5_data4 | 3 | IO | | | | | | | | | | |
| | sdio4_cmd | 4 | IO | | | | | | | | | | |
| | usbd0_ulpiph_data7 | 5 | IO | | | | | | | | | | |
| | gpio5_156 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| K26 | usbb3_hsic_strobe | 0 | IO | L | L | 7 | 1.2 V | vdds_hsic | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVCMOS DDR |
| | gpio5_158 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| K27 | usbb3_hsic_data | 0 | IO | L | L | 7 | 1.2 V | vdds_hsic | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVCMOS DDR |
| | gpio5_159 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| E9 | vdda_sata | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| D10 | vssa_sata | 0 | GND | - | - | - | - | - | - | - | - | - | Power |
| G9 | sata_tx | 0 | ODS | Z | Z | 0 | 1.8 V | vdda_sata | No | No | 3 | No | SATAPHY |
| F9 | sata_ty | 0 | ODS | Z | Z | 0 | 1.8 V | vdda_sata | No | No | 3 | No | SATAPHY |
| E10 | sata_rx | 0 | IDS | Z | Z | 0 | 1.8 V | vdda_sata | No | No | NA | NA | SATAPHY |
| F10 | sata_ry | 0 | IDS | Z | Z | 0 | 1.8 V | vdda_sata | No | No | NA | NA | SATAPHY |
| E5 | vdds_sdcard | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| F8 | sdcard_clk ⁽¹⁴⁾ | 0 | O | L | L | 0 | 3.0 V or 1.8 V | vdds_sdcard | Yes | See ⁽⁹⁾ | 2 ⁽⁹⁾ | PUx / PDy ⁽⁶⁾ | LVCMOS SDCARD |
| | jtag_rtck | 3 | O | | | | | | | | | | |
| | n_clk | 5 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| E8 | sdcard_cmd ⁽¹⁴⁾ | 0 | IO | L | L | 0 | 3.0 V or 1.8 V | vdds_sdcard | Yes | See ⁽⁹⁾ | 2 ⁽⁹⁾ | PUx / PDy ⁽⁶⁾ | LVCMOS SDCARD |
| | jtag_tdo | 3 | O | | | | | | | | | | |
| | uart6_rx | 4 | I | | | | | | | | | | |
| | n_d2 | 6 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| H6 | sdcard_data0 ⁽¹⁴⁾ | 0 | IO | L | 0 | 0 | 3.0 V or 1.8 V | vdds_sdcard | Yes | See ⁽⁹⁾ | 2 ⁽⁹⁾ | PUx / PDy ⁽⁶⁾ | LVCMOS SDCARD |
| | jtag_tdi | 3 | I | | | | | | | | | | |
| | n_d0 | 5 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| H5 | sdcard_data1 ⁽¹⁴⁾ | 0 | IO | L | 0 | 0 | 3.0 V or 1.8 V | vdds_sdcard | Yes | See ⁽⁹⁾ | 2 ⁽⁹⁾ | PUx / PDy ⁽⁶⁾ | LVCMOS SDCARD |
| | jtag_nrst | 3 | I | | | | | | | | | | |
| | n_d1 | 5 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| G5 | sdcard_data2 ⁽¹⁴⁾ | 0 | IO | L | 0 | 0 | 3.0 V or 1.8 V | vdds_sdcard | Yes | See ⁽⁹⁾ | 2 ⁽⁹⁾ | PUx / PDy ⁽⁶⁾ | LVCMOS SDCARD |
| | jtag_tmisc | 3 | IO | | | | | | | | | | |
| | n_d2 | 5 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|------------------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|--------------------|---------------------------|--------------------------|---------------|
| E7 | sdcard_data3 ⁽¹⁴⁾ | 0 | IO | L | 0 | 0 | 3.0 V or 1.8 V | vdds_sdcard | Yes | See ⁽⁹⁾ | 2 ⁽⁹⁾ | PUx / PDy ⁽⁶⁾ | LVCMOS SDCARD |
| | jtag_tck | 3 | I | | | | | | | | | | |
| | n_d3 | 5 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AE18 | vdds_usbhs18 | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| AN21 | vdda_usbhs33 | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| AK20 | vssa_usbhs | 0 | GND | - | - | - | - | - | - | - | - | - | Power |
| AL19 | usb0_hs_dp | 0 | IODS | H | H | 0 | 3.3 V | vdda_usbhs33 | No | No | See ⁽¹⁶⁾ | See ⁽¹⁷⁾ | USB2PHY |
| | uart3_rx_irrx | 4 | I | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AM19 | usb0_hs_dm | 0 | IODS | L | L | 0 | 3.3 V | vdda_usbhs33 | No | No | See ⁽¹⁶⁾ | See ⁽¹⁷⁾ | USB2PHY |
| | uart3_tx_irtx | 4 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| AN19 | usbphy_ce | 0 | O | 0 | Z | 0 | 3.3 V | vdda_usbhs33 | No | No | See ⁽¹⁶⁾ | NA | USB2PHY |
| AE19 | vdda_usbss18 | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| AK21 | vssa_usbss | 0 | GND | - | - | - | - | - | - | - | - | - | Power |
| AL20 | usb0_ss_tx | 0 | ODS | Z | Z | 0 | 1.8 V | vdda_usbss18 | No | No | 5 | No | USB3PHY |
| AM20 | usb0_ss_ty | 0 | ODS | Z | Z | 0 | 1.8 V | vdda_usbss18 | No | No | 5 | No | USB3PHY |
| AL21 | usb0_ss_rx | 0 | IDS | Z | Z | 0 | 1.8 V | vdda_usbss18 | No | No | NA | NA | USB3PHY |
| AM21 | usb0_ss_ry | 0 | IDS | Z | Z | 0 | 1.8 V | vdda_usbss18 | No | No | NA | NA | USB3PHY |
| K32 | drm_emu0 | 0 | IO | H | H | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | hw_wkdbg6 | 5 | O | | | | | | | | | | |
| | gpio1_wk6 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| K31 | drm_emu1 | 0 | IO | H | H | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | hw_wkdbg7 | 5 | O | | | | | | | | | | |
| | gpio1_wk7 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| B32 | jtag_nrst | 0 | I | L | L | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | safe_mode | 7 | | | | | | | | | | | |
| C31 | jtag_tck | 0 | I | L | L | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | safe_mode | 7 | | | | | | | | | | | |
| B33 | jtag_rtck | 0 | O | L | L | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | safe_mode | 7 | | | | | | | | | | | |
| B31 | jtag_tmisc | 0 | IO | H | H | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS BK |
| | safe_mode | 7 | | | | | | | | | | | |
| A32 | jtag_tdi | 0 | I | H | H | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | safe_mode | 7 | | | | | | | | | | | |
| A33 | jtag_tdo | 0 | O | H | H | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | safe_mode | 7 | | | | | | | | | | | |
| L31 | sys_32k | 0 | I | Z | Z | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| J24 | vdds_osc | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| L30 | vssa_xtal | 0 | GND | - | - | - | - | - | - | - | - | - | Power |
| L32 | fref_xtal_in | 0 | I-AI | Z | Z | 0 | 1.8 V | vdds_osc | Yes | No | NA | No | LVCMOS OSC |
| M32 | fref_xtal_out | 0 | AO | Z | NA | 0 | 1.8 V | vdds_osc | Yes | No | NA | No | OSC |
| L33 | fref_xtal_clk | 0 | O-AO | 0 | Z | 0 | 1.8 V | vdds_osc | Yes | No | NA | No | LVCMOS OSC |
| N31 | fref_clk_ireq | 0 | IO | L | L | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVCMOS |
| | gpio1_wk13 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] ⁽²⁾ | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-------------------------------------|----------------|--------------------------|----------|---------------------------|-----------------------------|-----------------------------|
| M31 | fref_clk0_out | 0 | O | L | 0 | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | hw_wkdbg9 | 5 | O | | | | | | | | | | |
| | gpio1_wk12 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| P31 | fref_clk1_out | 0 | O | L | L | 7 | 1.2 V or 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | hw_wkdbg5 | 5 | O | | | | | | | | | | |
| | gpio1_wk11 | 6 | IO | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| N33 | sys_nrespwron | 0 | I | Z | Z | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 | PUx / PDy ⁽⁷⁾ | LVCMOS |
| N32 | sys_nreswarm | 0 | IOD | 0 | H | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 | PUx / PDy ⁽⁷⁾ | LVCMOS Tri-State Open Drain |
| T31 | sys_pwr_req | 0 | O | H | 1 | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | hw_wkdbg15 | 5 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| R32 | sr_pmic_scl | 0 | IOD | H | H | 0 | 1.8 V | vdds_1p8 | Yes | No | 3 | PUx / PDy ⁽⁴⁾ | LVCMOS Open Drain |
| R31 | sr_pmic_sda | 0 | IOD | H | H | 0 | 1.8 V | vdds_1p8 | Yes | No | 3 | PUx / PDy ⁽⁴⁾ | LVCMOS Open Drain |
| R33 | sys_nirq1 | 0 | I | H | H | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PUx / PDy ⁽⁴⁾ | LVCMOS |
| | gpio1_wk16 | 6 | IO | | | | | | | | | | |
| T32 | sys_nirq2 | 0 | I | H | H | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PUx / PDy ⁽⁴⁾ | LVCMOS |
| | gpio1_wk17 | 6 | IO | | | | | | | | | | |
| P29 | i2c1_pmic_scl | 0 | OD | H | H | 0 | 1.8 V | vdds_1p8 | Yes | No | 3 | PUx / PDy-OD ⁽⁴⁾ | I ² C Open Drain |
| P28 | i2c1_pmic_sda | 0 | OD | H | H | 0 | 1.8 V | vdds_1p8 | Yes | No | 3 | PUx / PDy-OD ⁽⁴⁾ | I ² C Open Drain |
| U31 | sys_boot0 | 0 | I | Z | Z | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | drm_emu2 | 3 | O | | | | | | | | | | |
| | drm_emu15 | 4 | O | | | | | | | | | | |
| | hw_wkdbg0 | 5 | O | | | | | | | | | | |
| | gpio1_wkout0 | 6 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| U32 | sys_boot1 | 0 | I | Z | Z | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | drm_emu3 | 3 | O | | | | | | | | | | |
| | drm_emu16 | 4 | O | | | | | | | | | | |
| | hw_wkdbg1 | 5 | O | | | | | | | | | | |
| | gpio1_wkout1 | 6 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| U33 | sys_boot2 | 0 | I | Z | Z | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | drm_emu4 | 3 | O | | | | | | | | | | |
| | drm_emu17 | 4 | O | | | | | | | | | | |
| | hw_wkdbg2 | 5 | O | | | | | | | | | | |
| | gpio1_wkout2 | 6 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| V31 | sys_boot3 | 0 | I | Z | Z | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁸⁾ | PU/PD | LVCMOS |
| | drm_emu5 | 3 | O | | | | | | | | | | |
| | drm_emu18 | 4 | O | | | | | | | | | | |
| | hw_wkdbg3 | 5 | O | | | | | | | | | | |
| | gpio1_wkout3 | 6 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|--------------------------|--------------|
| V32 | sys_boot4 | 0 | I | Z | Z | 0 | 1.8 V | vdds_1p8 | Yes | Yes | 4 ⁽⁶⁾ | PU/PD | LVC MOS |
| | drm_emu6 | 3 | O | | | | | | | | | | |
| | drm_emu19 | 4 | O | | | | | | | | | | |
| | hw_wkdbg4 | 5 | O | | | | | | | | | | |
| | gpio1_wkout4 | 6 | O | | | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | | | |
| A29 | ddrch1_dm0 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| B24 | ddrch1_dm1 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| C30 | ddrch1_dm2 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| B6 | ddrch1_dm3 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| C28 | ddrch1_dq0 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| A31 | ddrch1_dq1 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| C29 | ddrch1_dq2 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| B30 | ddrch1_dq3 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| B29 | ddrch1_dq4 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| C26 | ddrch1_dq5 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| B28 | ddrch1_dq6 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| B26 | ddrch1_dq7 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| C23 | ddrch1_dq8 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| C22 | ddrch1_dq9 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| C21 | ddrch1_dq10 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| B22 | ddrch1_dq11 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| C24 | ddrch1_dq12 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| C25 | ddrch1_dq13 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| B25 | ddrch1_dq14 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| A25 | ddrch1_dq15 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| E31 | ddrch1_dq16 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| E33 | ddrch1_dq17 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| E32 | ddrch1_dq18 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| F32 | ddrch1_dq19 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| C33 | ddrch1_dq20 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| D30 | ddrch1_dq21 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| F31 | ddrch1_dq22 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| C32 | ddrch1_dq23 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |
| C6 | ddrch1_dq24 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddr_ch1 | Yes | No | See (3) | PuX / PDy ⁽³⁾ | LVC MOS DDR |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|--|------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|--------------------------|--------------|
| A5 | ddrch1_dq25 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| B5 | ddrch1_dq26 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| C5 | ddrch1_dq27 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| B2 | ddrch1_dq28 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| B3 | ddrch1_dq29 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| C3 | ddrch1_dq30 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| D4 | ddrch1_dq31 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| C27 | ddrch1_dqs0 | 0 | IODS | L | L | 0 | 1.5 V | vdds_ ddr_ch1 | NA | NA | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| B23 | ddrch1_dqs1 | 0 | IODS | L | L | 0 | 1.5 V | vdds_ ddr_ch1 | NA | NA | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| D31 | ddrch1_dqs2 | 0 | IODS | L | L | 0 | 1.5 V | vdds_ ddr_ch1 | NA | NA | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| C4 | ddrch1_dqs3 | 0 | IODS | L | L | 0 | 1.5 V | vdds_ ddr_ch1 | NA | NA | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| B27 | ddrch1_ndqs0 | 0 | IODS | H | H | 0 | 1.5 V | vdds_ ddr_ch1 | NA | NA | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| A23 | ddrch1_ndqs1 | 0 | IODS | H | H | 0 | 1.5 V | vdds_ ddr_ch1 | NA | NA | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| D32 | ddrch1_ndqs2 | 0 | IODS | H | H | 0 | 1.5 V | vdds_ ddr_ch1 | NA | NA | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| B4 | ddrch1_ndqs3 | 0 | IODS | H | H | 0 | 1.5 V | vdds_ ddr_ch1 | NA | NA | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| A19 | ddrch1_vref_dq | 0 | PWR | Z | NA | 0 | 0.5 x vdds_ ddr_ch1 | vdds_ ddr_ch1 | Yes | No | - | NA | Analog |
| J16 | vddq_vref_ddrch1 | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| A27 / A11 / A3 / H30 / H10 / J19 / J18 / J10 / K30 / K25 / K23 / K15 / K14 / L25 / M25 / A21 | vdds_ ddr_ch1 | 0 | PWR | - | - | - | - | - | - | - | - | - | Power |
| J1 | ddrch2_dm0 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| AJ3 | ddrch2_dm1 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| G1 | ddrch2_dm2 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| AL4 | ddrch2_dm3 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| K3 | ddrch2_dq0 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| H2 | ddrch2_dq1 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| H3 | ddrch2_dq2 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| J3 | ddrch2_dq3 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| J2 | ddrch2_dq4 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| M3 | ddrch2_dq5 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| L2 | ddrch2_dq6 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| L1 | ddrch2_dq7 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| AK3 | ddrch2_dq8 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |
| AG1 | ddrch2_dq9 | 0 | IO | L | L | 0 | 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| AH3 | ddrch2_dq10 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AJ2 | ddrch2_dq11 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AH2 | ddrch2_dq12 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AL1 | ddrch2_dq13 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AL3 | ddrch2_dq14 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AK4 | ddrch2_dq15 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| G3 | ddrch2_dq16 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| D3 | ddrch2_dq17 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| C2 | ddrch2_dq18 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| C1 | ddrch2_dq19 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| D2 | ddrch2_dq20 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| F2 | ddrch2_dq21 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| G2 | ddrch2_dq22 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| F3 | ddrch2_dq23 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AM3 | ddrch2_dq24 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AL5 | ddrch2_dq25 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AM4 | ddrch2_dq26 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AN3 | ddrch2_dq27 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AL7 | ddrch2_dq28 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AL6 | ddrch2_dq29 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AM7 | ddrch2_dq30 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AM6 | ddrch2_dq31 | 0 | IO | L | L | 0 | 1.5 V | vdds_ddrch2 | Yes | No | See (3) | PUx / PDy(3) | LVC MOS DDR |
| K2 | ddrch2_dqs0 | 0 | IODS | L | L | 0 | 1.5 V | vdds_ddrch2 | NA | NA | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AK2 | ddrch2_dqs1 | 0 | IODS | L | L | 0 | 1.5 V | vdds_ddrch2 | NA | NA | See (3) | PUx / PDy(3) | LVC MOS DDR |
| E2 | ddrch2_dqs2 | 0 | IODS | L | L | 0 | 1.5 V | vdds_ddrch2 | NA | NA | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AM5 | ddrch2_dqs3 | 0 | IODS | L | L | 0 | 1.5 V | vdds_ddrch2 | NA | NA | See (3) | PUx / PDy(3) | LVC MOS DDR |
| L3 | ddrch2_ndqs0 | 0 | IODS | H | H | 0 | 1.5 V | vdds_ddrch2 | NA | NA | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AL2 | ddrch2_ndqs1 | 0 | IODS | H | H | 0 | 1.5 V | vdds_ddrch2 | NA | NA | See (3) | PUx / PDy(3) | LVC MOS DDR |
| E3 | ddrch2_ndqs2 | 0 | IODS | H | H | 0 | 1.5 V | vdds_ddrch2 | NA | NA | See (3) | PUx / PDy(3) | LVC MOS DDR |
| AN5 | ddrch2_ndqs3 | 0 | IODS | H | H | 0 | 1.5 V | vdds_ddrch2 | NA | NA | See (3) | PUx / PDy(3) | LVC MOS DDR |
| U1 | ddrch2_vref_dq | 0 | PWR | Z | NA | 0 | 0.5 x vdds_ddrch2 | vdds_ddrch2 | Yes | No | - | NA | Analog |
| V10 | vddq_vref_ddrch2 | 0 | PWR | - | - | - | - | - | - | - | - | - | - |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] ⁽²⁾ | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|---|-----------------|----------|----------|----------------------|---------------------------|---------------------|-------------------------------------|----------------|--------------------------|----------|---------------------------|--------------------------|--------------------|
| E1 / J9 / K8 / N1 / R9 / T9 / V9 / W9 / AA1 / AC10 / AE12 / AE11 / AE10 / AJ1 / AM2 | vdds_ddr_ch2 | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| A7 | ddr3ch1_a0 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B7 | ddr3ch1_a1 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C7 | ddr3ch1_a2 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B8 | ddr3ch1_a3 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C8 | ddr3ch1_a4 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B9 | ddr3ch1_a5 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C10 | ddr3ch1_a6 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B12 | ddr3ch1_a7 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C12 | ddr3ch1_a8 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| A13 | ddr3ch1_a9 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B13 | ddr3ch1_a10_ap | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C13 | ddr3ch1_a11 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B14 | ddr3ch1_a12_nbc | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C14 | ddr3ch1_a13 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| A15 | ddr3ch1_a14 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B15 | ddr3ch1_a15 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C11 | ddr3ch1_cka | 0 | IODS | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C18 | ddr3ch1_ckb | 0 | IODS | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C9 | ddr3ch1_cke0 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| A17 | ddr3ch1_cke1 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B11 | ddr3ch1_ncka | 0 | IODS | H | H | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B18 | ddr3ch1_nckb | 0 | IODS | H | H | 0 | 1.35 V or 1.5 V | vdds_ddr_ch1 | Yes | No | See ⁽³⁾ | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] ⁽²⁾ | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-------------------------------------|----------------|--------------------------|----------|---------------------------|--------------------------|--------------------|
| B10 | ddr3ch1_ncs0 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B17 | ddr3ch1_ncs1 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C15 | ddr3ch1_ba0 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B16 | ddr3ch1_ba1 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C16 | ddr3ch1_ba2 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C17 | ddr3ch1_ncas | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B19 | ddr3ch1_nras | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C19 | ddr3ch1_nreset | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B20 | ddr3ch1_nwe | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| C20 | ddr3ch1_odt0 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| B21 | ddr3ch1_odt1 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch1 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| A9 | ddr3ch1_vref_ca | 0 | PWR | Z | NA | 0 | 0.5 x vdds_ ddr_ch1 | vdds_ ddr_ch1 | Yes | No | - | NA | Analog |
| AG2 | ddr3ch2_a0 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AG3 | ddr3ch2_a1 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AF2 | ddr3ch2_a2 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AF3 | ddr3ch2_a3 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AE2 | ddr3ch2_a4 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AE3 | ddr3ch2_a5 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AC3 | ddr3ch2_a6 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AB2 | ddr3ch2_a7 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AB3 | ddr3ch2_a8 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AA2 | ddr3ch2_a9 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AA3 | ddr3ch2_a10_ap | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| Y2 | ddr3ch2_a11 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] ⁽²⁾ | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-------------------------------------|----------------|--------------------------|----------|---------------------------|--------------------------|--------------------------|
| Y3 | ddr3ch2_a12_nbc | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| W1 | ddr3ch2_a13 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| W2 | ddr3ch2_a14 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| W3 | ddr3ch2_a15 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AC2 | ddr3ch2_cka | 0 | IODS | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| R2 | ddr3ch2_ckb | 0 | IODS | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AD2 | ddr3ch2_cke0 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| U3 | ddr3ch2_cke1 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AC1 | ddr3ch2_ncka | 0 | IODS | H | H | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| R1 | ddr3ch2_nckb | 0 | IODS | H | H | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AD3 | ddr3ch2_ncs0 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| T2 | ddr3ch2_ncs1 | 0 | IO | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| V2 | ddr3ch2_ba0 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| V3 | ddr3ch2_ba1 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| U2 | ddr3ch2_ba2 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| T3 | ddr3ch2_ncas | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| R3 | ddr3ch2_nras | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| P2 | ddr3ch2_nreset | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| P3 | ddr3ch2_nwe | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| N2 | ddr3ch2_odt0 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| M2 | ddr3ch2_odt1 | 0 | O | L | L | 0 | 1.35 V or 1.5 V | vdds_ddr_ch2 | Yes | No | See (3) | PUx / PDy ⁽³⁾ | LVC MOS DDR3 DDR3L |
| AE1 | ddr3ch2_vref_ca | 0 | AI | Z | NA | 0 | 0.5 x vdds_ddr_ch2 | vdds_ddr_ch2 | Yes | No | - | NA | Analog |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] (2) | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|---|------------------------|----------|----------|----------------------|---------------------------|---------------------|-----------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| J11 / K22 / K12 / K11 / K9 / L14 / L13 / L12 / L10 / M14 / M13 / M11 / M10 / N15 / N14 / N11 / P11 / W24 / W22 / Y24 / Y23 / AA23 / AB24 / AB23 / AC24 / AC22 / AC21 / AD23 / AD22 / AD20 / AD16 / AD15 / AD14 / AD12 | vdd_core | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| AH21 | vdd_core_sense | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| T14 / T13 / T11 / T10 / W13 / W12 / W10 / Y19 / Y15 / Y11 / Y10 / AA19 / AA16 / AA15 / AA11 / AB19 / AB15 / AB13 / AB11 / AB10 / AC20 / AC16 / AC14 / AC13 / AC12 / AD19 / AD11 | vdd_mm | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| AG21 | vdd_mm_sense | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| K20 / K19 / K18 / L24 / L22 / L21 / L20 / L18 / M24 / M23 / M20 / M19 / N23 / N18 / P24 / P23 / P22 / P18 / R24 / T24 / T23 / T21 / T20 | vdd_mpu | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| U29 | vdd_mpu_sense | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| AJ29 | vss_mpu_sense | 0 | GND | - | - | - | - | - | - | - | - | - | - |
| AD9 | vpp1 | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| D28 / D26 / D24 / D23 / D21 / D20 / D18 / D16 / D14 / D13 / D11 / D8 / D6 / F4 / H4 / L16 / L4 / M21 / M17 / M15 / N30 / N22 / N21 / N20 / N19 / N17 / N16 / N13 / N12 / N4 / P30 / P21 / P19 / P16 / P15 / P13 / P12 / P10 / P9 / R22 / R21 / R20 / R19 / R18 / R17 / R16 / R15 / R14 / R13 / R12 / R10 / T30 / T19 / T17 / T15 / T4 / U22 / U21 / U19 / U18 / U17 / U16 / U15 / U13 / U12 / V30 / V24 / V23 / V21 / V20 / V19 / V17 / V15 / V14 / V13 / V11 / V4 / W21 / W20 / W19 / W18 / W17 / W16 / W15 / W14 / Y22 / Y21 / Y18 / Y16 / Y13 / Y12 / AA30 / AA22 / AA21 / AA20 / AA18 / AA17 / AA14 / AA13 / AA12 / AA4 / AB21 / AB20 / AB17 / AB14 / AC30 / AC18 / AC4 / AD4 / AF30 / AF4 / AH30 / AK26 / AK23 / AK14 / AK13 / F30 / AK11 / AK10 / AK8 / AK6 | vss | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| Y26 | vdda_dpll_core_emu_abe | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| U8 | vdda_dpll_mm_l4per | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| AF24 | vdda_dpll_hdmi | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| Y27 | vdda_dpll_mpu | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| AE22 | vdda_ldo_core | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| AE20 | vdda_ldo_mm | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| J15 | vdda_ldo_mpu | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| N25 | vdda_ldo_emu_wkup | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| AE16 | vdda_vbgap_core | 0 | PWR | - | - | - | - | - | - | - | - | - | - |

Table 3-1. Ball Characteristics⁽¹⁾ (continued)

| BALL BOTTOM [1] | SIGNAL NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | IO VOLTAGE VALUE [8] ⁽²⁾ | POWER NAME [9] | SECOND POWER AVAIL. [10] | HYS [11] | BUFFER STRENGTH (mA) [12] | PULLUP/DOWN TYPE [13] | IO CELL [14] |
|-----------------|------------------------------|----------|----------|----------------------|---------------------------|---------------------|-------------------------------------|----------------|--------------------------|----------|---------------------------|-----------------------|--------------|
| T25 | cap_vdda_ldo_sram_core_array | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| AG17 | cap_vdda_ldo_sram_mm_array | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| H17 | cap_vdda_ldo_sram_mpu_array | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| V25 | cap_vddldo_emu_wkup | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| AD18 | cap_vbb_ldo_mm | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| H13 | cap_vbb_ldo_mpu | 0 | PWR | - | - | - | - | - | - | - | - | - | - |
| K16 | cap_vdda_ldo_sram_mpu_array2 | 0 | PWR | - | - | - | - | - | - | - | - | - | - |

(1) NA in this table stands for not applicable.

(2) For more information on recommended operating conditions, see [Section 4.2, Recommended Operating Conditions](#).

(3) In PUx / PDy, x and y = 60 to 200 μ A

The output impedance settings (or drive strengths) of this IO are programmable (34 Ω , 40 Ω , 48 Ω , 60 Ω , 80 Ω or 11.75 mA, 10 mA, 8.33 mA, 6.67 mA) depending on the values of the I2, I1, I0 registers. The default value is I[2:0] = 010.

(4) The pullup or pulldown can be either the standard LVCMOS 100- μ A drive strength or the configurable I²C internal pullup resistor. Naming convention:

- PUx / PDy-OD is specified: the default buffer configuration is high-speed (HS) I²C point-to-point mode using the internal pullup resistor.

NOTE

For balls P29 / P28, i2c1_pmic_scl and i2c1_pmic_sda functional modes are I²C only.

- PUx / PDy-GPIO is specified: the default buffer configuration is standard LVCMOS mode (non-I²C). The internal pullup resistance programming does not apply in this mode.

These IOs have a pullupresx register that configures the internal I²C pullup or pulldown resistor of the IO, plus two load register bits [LB1:0] that configure the I²C load.

By default, at the reset release time, the multiplexing mode is safe_mode (that means GPIO). The I²C function must be selected to enable this I²C function and by default:

- For HDMI DDC (balls AM22 / AL23):

HSMODE = fast-speed mode

PULLUPSPRESX = 0, this means that the internal I²C pullup resistor is enabled.

LB[1:0] = 00: this means a 4-k Ω pullup resistor, for a load = 5 pF to 15 pF, in fast-speed mode.

- For SR (balls R32/ R31):

HSMODE = fast-speed mode

PULLUPSPRESX = 0, this means that the internal I²C pullup resistor is enabled.

LB[1:0] = 01: this means a 4-k Ω pullup resistor, for a load = 5 pF to 15 pF, in fast-speed mode.

- For I2C1 (balls P29 / P28):

HSMODE = fast-speed mode

PULLUPSPRESX = 0, this means that the internal I²C pullup resistor is enabled.

LB[1:0] = 01: this means a 2.1-k Ω pullup resistor, for a load = 15 pF to 50 pF, in fast-speed mode.

- For I2C2, I2C3, I2C4, I2C5 (balls AL33 / AM32 / AJ5 / AH4 / AJ21 / AJ20 / AL28 / AM29):

HSMODE = full-speed mode

PULLUPSPRESX = 1, external PU expected on the board.

NOTE

For I2C[5:2]: external pullup or pulldown resistors can be avoided if the I2C[5:2] interfaces are activated by boot. If the interface is activated then the interface is configured in driver mode and in this case pullup or pulldown resistors are not needed. For more information on boot modes, see the Device TRM.

In I²C mode configuration, for a full description of the internal pullup resistance programming according to the load range, see the CONTROL_I2C_0 and the CONTROL_SMART3I/O_PADCONF_0 registers in the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the

Device TRM.

In standard LVC MOS mode configuration (non-I²C mode), for a full description of the pullup or pulldown programming, see the CONTROL_CORE_PADX registers in the Control Module / Control Module Functional Description / Pad Functional Multiplexing and Configuration section of the Device TRM.

- (5) In PDy, y = 200 k Ω
- (6) In PUx / PDy, x and y = 10 k Ω to 100 k Ω .
- (7) The pullup / pulldown block strength is equal to: minimum = 50 μ A, typical = 100 μ A, maximum = 250 μ A.
- (8) The output impedance settings of this IO cell are programmable; by default, the value is DS[1:0] = 10, this means 40 Ω . For more information on DS[1:0] register configuration, see the Device TRM.
- (9) The output impedance settings of this IO cell are programmable; by default, the register value is ic[1:0] = 00, this means 44 Ω . The hysteresis function is also programmable for this IO; by default, the register value is hyst_en = 1, this means hysteresis function is enabled. For more information see the Device TRM.
- (10) gpio6_182, gpio6_183, gpio6_184, gpio6_185, gpio6_186, gpio6_187, gpio8_233, gpio8_234 GPIOs (balls AN9 / AM9 / AL9 / AM8 / AL8 / AN7 / AG5 / AF5) can output the same GPIO in mode 0 or in mode 6.
- (11) For the following balls: AF14 / AG14 / AH13 / AJ13, pulldown resistor is 20 k Ω . No pullup resistor is available.
- (12) See the note below.

NOTE

For SATA and USB3 SS PHYs:

- If the serial PHY is enabled, the corresponding vdda_xxx voltage supply must be supplied by a dedicated, low-noise, voltage source.
- If the serial PHY is definitively disabled:
 - The PHY voltage supply (vdda_xxx and vssa_xxx) and the associated DPLL voltage supply (vdda_dppll_xxx) are grounded for power saving.
 - The associated interface balls are left unconnected.

For HDMI PHY:

- If the serial PHY is enabled, the corresponding vdda_hdmi voltage and vdda_dppll_hdmi supplies must be supplied by dedicated low-noise voltage sources.
- If the serial PHY is definitively disabled:
 - vdda_hdmi is supplied.
 - vdda_dppll_hdmi can be grounded only if the corresponding HDMI DPLL is never used to generate the functional clock to the DISPC.
 - The associated data/clock balls are left unconnected.
 - The PHY can be put in the off power state (even if the HDMI DPLL is used).

For HDMI control interface (CEC, HPD, DDC):

- If the HDMI control interface is enabled, vdds_hdmi must be supplied by a dedicated low-noise voltage source.
- If the HDMI is definitively disabled, the other multiplexed CMOS signals of the interface can be enabled, the interface can be supplied by the same voltage source as vdds_1p8v.
- If the HDMI and the multiplexed CMOS signals are definitively disabled:
 - The voltage supply (vdds_hdmi) is grounded for power saving.
 - The associated interface balls are left unconnected.

For DSI Port A and Port C PHYs:

- If the serial PHY is enabled, the corresponding vdda_dsiportx voltage supply must be supplied by a dedicated low-noise voltage source.
- If the PHY is definitively disabled:
 - The PHY voltage supply (vdda_dsiportx and vssa_dsiportx) is grounded for power saving only if the corresponding DSI DPLL is never used to generate the functional clock to the DISPC.
 - The associated interface balls are left unconnected.

For CSI-2 PHYs:

- If the CSI-2 serial PHY is enabled, vdda_csiportx must be supplied by a dedicated low-noise voltage source.
- If the CSI-2 serial PHY is definitively disabled, the other multiplexed CMOS signals of the interface can be enabled, the interface can be supplied by the same voltage source as vdds_1p8v.
- If the CSI-2 serial PHY and the multiplexed CMOS signals are definitively disabled:
 - The PHY voltage supply (vdda_csiportx and vssa_csiportx) is grounded for power saving.
 - The associated interface balls are left unconnected.

For USB2 HS PHY:

- If the USB2 HS PHY is enabled, vdda_usbhs33 and vdds_usbhs18 must be supplied by dedicated 3.3-V and 1.8-V low-noise voltage sources.
- If the USB2 HS PHY is definitively disabled, the other multiplexed 3.3-V CMOS signals (UART3) of the interface can be enabled, vdda_usbhs33 must be supplied by a dedicated 3.3-V voltage source and vdds_usbhs18 can be supplied by the same voltage source as vdds_1p8v.
- If the USB2 HS PHY and UART3 signals are definitively disabled:
 - vdda_usbhs33 and vdds_usbhs18 are supplied.
 - The power-down bit is set to 1 (USB2PHY_PWR_CNTL.MEM_PD bit) in order to put the USB2 PHY in power-down mode and lower the leakage current from other supplies.
 - The disable charger detect is set to 1 CONTROL_USB2PHYCORE.USB2PHY_DISCHGDET bit) to disable the charger detect.
 - There are forward-biased diodes from usbd0_hs_dp, usbd0_hs_dm, and usbphy_ce pins to the vdda_usbhs33 pin.

For SDCARD interface:

- If the SDCARD functional signals are enabled, vdds_sdcard must be supplied by a 1.8-V or 3.0-V voltage source.
- If the SDCARD functional signals are definitively disabled, the other multiplexed CMOS signals of the interface can be enabled, the interface can be supplied by the same voltage source as vdds_1p8v.
- If the SDCARD functional balls and the multiplexed CMOS signals are definitively disabled:
 - The interface balls are left unconnected.
 - The SDCARD_PWRDNZ bit is kept at 0.

There are two options for the associated power supply:

- vdds_sdcard is grounded.
- vdds_sdcard is supplied by a 1.8-V or 3.0-V voltage supply. In this case, it is also recommended to keep default value of SDCARD_BIAS_VMODE bit (that is, 1).

For the corresponding setting of the SDCARD_PWRDNZ and SDCARD_BIAS_VMODE bits, see the Control Module / Control Module Functional Description / Extended-Drain IO and PBIAS Cell section and the Control Module / Control Module Programming Guide section of the Device TRM.

(13) See the Caution below.

CAUTION

Some GPMC chip-select pins have a pulldown resistor enabled by default after reset and all chip-select signals gpmc_ncs[6:0] are active low.

In case of an application with several memories connected to the GPMC, for the memories connected to a chip-select whose internal pulldown resistor is enabled by default after reset (ncs1, ncs2, ncs3, or ncs4), it is necessary to disable this pulldown resistor before performing the first access to any memory. Otherwise, contention will happen because several memories will be selected at the same time.

In the particular case of memory booting via the GPMC interface (memory device must be connected to the gpmc_ncs0 pin), it is not possible to disable any pulldown resistor before the first access. As a consequence, no memory device should be connected to a chip-select whose internal pulldown resistor is enabled by default (ncs1, ncs2, ncs3, or ncs4). Otherwise, contention will prevent OMAP from booting.

For more information, see the Initialization / Preinitialization / Boot Configuration / Boot Peripheral Pin Multiplexing section of the Device TRM.

- (14) On the SDCARD IOs (supporting sdcard signals in muxmode0), the PU/PD range has been changed from [10 kΩ to 100 kΩ] for ES1.0 to [10 kΩ to 40 kΩ] for ES2.0.
- (15) The maximum capacitive load for the DSI low-power mode is equal to 70 pF. For more information, see Chapter 9 of the MIPI D-PHY standard v1.1. No specific capacitive load is needed in DSI high-speed mode.
- (16) IO drive strength for usbd0_hs_dp and usbd0_hs_dm: minimum 18.3 mA, maximum 89 mA (for a power supply vdda_usba0otg_3p3v = 3.46 V). IO drive strength for usbphy_ce: minimum 100 μA, maximum 20 mA.
- (17) Minimum PU = 900 Ω, maximum PU = 3.090 kΩ and minimum PD = 14.25 kΩ, maximum PD = 24.8 kΩ. For more information, see chapter 7 of the USB2 specification, in particular the Signaling / Device Speed Identification section.

3.3 Multiplexing Characteristics

Table 3-2 describes the device multiplexing (no characteristics are available in this table).

NOTE

This table does not take into account subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 3.4, *Signal Descriptions*.

NOTE

For more information, see the Control Module / Control Module Functional Description / PAD Functional Multiplexing and Configuration section of the Device TRM.

NOTE

Configuring two balls to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration. (safe_mode is not an input signal.)

NOTE

When a pad is set into a multiplexing mode which is not defined by ball multiplexing, this pad is actually set undriven (high impedance: Z) with a potential pullup or pulldown resistor. Pullup and pulldown resistors need to be disabled to have a pure high impedance.

NOTE

All balls not described in [Table 3-1](#) and [Table 3-2](#) are not connected.

Table 3-2. Multiplexing Characteristics⁽¹⁾

| BOTTOM BALLS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|--|------------|--------|--------|----------|---------------|-----------|----------|-----------|
| H20 / J23 / J22 / J14 / J13 / J12 / L9 / M9 / P26 / P25 / R25 / U27 / U26 / W25 / Y25 / Y9 / AA25 / AA9 / AB25 / AC25 / AC9 / AD25 / AE24 / AE21 / AE15 / AE14 / AE13 / AF21 / U28 | vdds_1p8 | - | - | - | - | - | - | - |
| AB9 | vdds_emmc | - | - | - | - | - | - | - |
| AJ10 | emmc_clk | - | - | - | - | - | gpio2_46 | safe_mode |
| AH10 | emmc_cmd | - | - | - | - | - | gpio2_47 | safe_mode |
| AG10 | emmc_data0 | - | - | - | - | - | gpio2_48 | safe_mode |
| AF10 | emmc_data1 | - | - | - | - | - | gpio2_49 | safe_mode |
| AH9 | emmc_data2 | - | - | - | - | - | gpio2_50 | safe_mode |
| AJ9 | emmc_data3 | - | - | - | - | - | gpio2_51 | safe_mode |
| AG9 | emmc_data4 | - | - | - | - | - | gpio2_52 | safe_mode |
| AJ8 | emmc_data5 | - | - | - | - | - | gpio2_53 | safe_mode |
| AH8 | emmc_data6 | - | - | - | - | - | gpio2_54 | safe_mode |
| AJ7 | emmc_data7 | - | - | - | - | - | gpio2_55 | safe_mode |
| J21 / J20 | vdds_c2c | - | - | - | - | - | - | - |
| J27 | Reserved | - | - | kbd_row0 | gpmc_ad0 | - | gpio2_37 | safe_mode |
| H28 | Reserved | - | - | kbd_row1 | gpmc_ad1 | - | gpio2_38 | safe_mode |
| H29 | Reserved | - | - | kbd_row2 | gpmc_ad2 | - | gpio2_39 | safe_mode |
| G29 | Reserved | - | - | kbd_row3 | gpmc_ad3 | - | gpio2_40 | safe_mode |
| E29 | Reserved | - | - | kbd_row4 | gpmc_ad4 | - | gpio2_41 | safe_mode |
| E27 | Reserved | - | - | kbd_row5 | gpmc_ad5 | - | gpio2_42 | safe_mode |
| F26 | Reserved | - | - | kbd_row6 | gpmc_ad6 | - | gpio2_43 | safe_mode |
| E26 | Reserved | - | - | kbd_row7 | gpmc_ad7 | - | gpio2_44 | safe_mode |
| J28 | Reserved | - | - | kbd_row8 | gpmc_clk | - | gpio2_36 | safe_mode |
| J29 | Reserved | - | - | - | gpmc_nwp | gpmc_nbe1 | gpio2_35 | safe_mode |
| E25 | Reserved | - | - | - | gpmc_nadv_ale | - | gpio2_33 | safe_mode |
| F25 | Reserved | - | - | kbd_col8 | gpmc_nbe0_cle | - | gpio2_34 | safe_mode |
| J32 | Reserved | - | - | kbd_col0 | gpmc_ad8 | hw_dbg16 | gpio2_56 | safe_mode |
| J33 | Reserved | - | - | kbd_col1 | gpmc_ad9 | hw_dbg17 | gpio2_57 | safe_mode |
| H32 | Reserved | - | - | kbd_col2 | gpmc_ad10 | hw_dbg18 | gpio2_58 | safe_mode |
| J31 | Reserved | - | - | kbd_col3 | gpmc_ad11 | hw_dbg19 | gpio2_59 | safe_mode |
| G31 | Reserved | - | - | kbd_col4 | gpmc_ad12 | hw_dbg20 | gpio2_60 | safe_mode |

Table 3-2. Multiplexing Characteristics⁽¹⁾ (continued)

| BOTTOM BALLS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|--------------|-------------------|--------------|-------------------|---------------------|--------------|------------|------------|-----------|
| H31 | Reserved | - | - | kbd_col5 | gpmc_ad13 | hw_dbg21 | gpio2_61 | safe_mode |
| G32 | Reserved | - | - | kbd_col6 | gpmc_ad14 | hw_dbg22 | gpio2_62 | safe_mode |
| G33 | Reserved | - | - | kbd_col7 | gpmc_ad15 | hw_dbg23 | gpio2_63 | safe_mode |
| G24 | Reserved | - | - | - | gpmc_a16 | hw_dbg24 | gpio4_113 | safe_mode |
| H24 | Reserved | - | - | - | gpmc_a17 | hw_dbg25 | gpio4_114 | safe_mode |
| E24 | Reserved | - | - | - | gpmc_a18 | hw_dbg26 | gpio4_115 | safe_mode |
| F24 | Reserved | - | - | - | gpmc_a19 | hw_dbg27 | gpio4_116 | safe_mode |
| G21 | Reserved | - | - | - | gpmc_a20 | hw_dbg28 | gpio4_117 | safe_mode |
| H21 | Reserved | - | - | - | gpmc_a21 | hw_dbg29 | gpio4_118 | safe_mode |
| E21 | Reserved | - | - | - | gpmc_a22 | hw_dbg30 | gpio4_119 | safe_mode |
| F21 | Reserved | - | - | - | gpmc_a23 | hw_dbg31 | gpio4_120 | safe_mode |
| P32 | Reserved | - | - | - | gpmc_ncs0 | - | gpio2_32 | safe_mode |
| N27 | Reserved | - | - | - | gpmc_wait0 | - | gpio2_45 | safe_mode |
| N29 | Reserved | - | - | - | - | hw_wkdbg13 | gpio1_wk15 | safe_mode |
| N28 | Reserved | - | - | - | - | hw_wkdbg14 | gpio1_wk14 | safe_mode |
| G20 | hsi2_caready | - | - | usbb1_ulpiphy_clk | gpmc_wait1 | - | gpio3_76 | safe_mode |
| F20 | hsi2_acready | - | - | usbb1_ulpiphy_nxt | gpmc_ncs1 | - | gpio3_77 | safe_mode |
| F17 | hsi2_cawake | - | - | usbb1_ulpiphy_dir | gpmc_a24 | - | gpio3_78 | safe_mode |
| E20 | hsi2_acwake | - | - | usbb1_ulpiphy_stp | gpmc_a25 | - | gpio3_79 | safe_mode |
| E14 | hsi2_caflag | - | - | usbb1_ulpiphy_data0 | gpmc_wait2 | - | gpio3_80 | safe_mode |
| F14 | hsi2_cadata | - | - | usbb1_ulpiphy_data1 | gpmc_ncs2 | - | gpio3_81 | safe_mode |
| G14 | hsi2_aclflag | - | - | usbb1_ulpiphy_data2 | gpmc_ncs3 | - | gpio3_82 | safe_mode |
| E17 | hsi2_acdata | - | - | usbb1_ulpiphy_data3 | gpmc_ncs4 | - | gpio3_83 | safe_mode |
| F13 | uart2_rts | mcspi3_somi | - | usbb1_ulpiphy_data4 | gpmc_nwe | hw_dbg16 | gpio3_84 | safe_mode |
| N9 | uart2_cts | mcspi3_cs0 | - | usbb1_ulpiphy_data5 | gpmc_noe_nre | hw_dbg17 | gpio3_85 | safe_mode |
| G13 | uart2_rx | mcspi3_simo | - | usbb1_ulpiphy_data6 | gpmc_ncs5 | hw_dbg18 | gpio3_86 | safe_mode |
| E13 | uart2_tx | mcspi3_clk | - | usbb1_ulpiphy_data7 | gpmc_ncs6 | hw_dbg19 | gpio3_87 | safe_mode |
| N26 | vdds_hsic | - | - | - | - | - | - | - |
| K28 | usbb2_hsic_strobe | - | - | - | - | - | gpio3_94 | safe_mode |
| K29 | usbb2_hsic_data | - | - | - | - | - | gpio3_95 | safe_mode |
| W31 | timer10_pwm_evt | - | - | - | - | - | gpio6_188 | safe_mode |
| W33 | dsiporta_te0 | - | - | - | - | - | gpio6_189 | safe_mode |
| AA33 | vdda_dsiporta | - | - | - | - | - | - | - |
| Y30 | vssa_dsiporta | - | - | - | - | - | - | - |
| AD31 | dsiporta_lane0x | - | - | - | - | - | - | - |
| AD32 | dsiporta_lane0y | - | - | - | - | - | - | - |
| AC31 | dsiporta_lane1x | - | - | - | - | - | - | - |
| AC32 | dsiporta_lane1y | - | - | - | - | - | - | - |
| AB32 | dsiporta_lane2x | - | - | - | - | - | - | - |
| AB31 | dsiporta_lane2y | - | - | - | - | - | - | - |
| AA32 | dsiporta_lane3x | - | - | - | - | - | - | - |
| AA31 | dsiporta_lane3y | - | - | - | - | - | - | - |
| Y32 | dsiporta_lane4x | - | - | - | - | - | - | - |
| Y31 | dsiporta_lane4y | - | - | - | - | - | - | - |
| AJ33 | timer9_pwm_evt | sync_sof_clk | sync_usof_itp_clk | - | - | - | gpio6_190 | safe_mode |
| AK30 | dsiportc_te0 | - | - | - | - | - | gpio6_191 | safe_mode |
| AE33 | vdda_dsiportc | - | - | - | - | - | - | - |
| AD30 | vssa_dsiportc | - | - | - | - | - | - | - |

Table 3-2. Multiplexing Characteristics⁽¹⁾ (continued)

| BOTTOM BALLS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|--------------|--------------------------|------------------|--------|--------------|------------------|-----------|--------------------------|-----------|
| AJ31 | dsportc_lane0x | - | - | - | - | - | - | - |
| AJ32 | dsportc_lane0y | - | - | - | - | - | - | - |
| AH32 | dsportc_lane1x | - | - | - | - | - | - | - |
| AH31 | dsportc_lane1y | - | - | - | - | - | - | - |
| AG32 | dsportc_lane2x | - | - | - | - | - | - | - |
| AG31 | dsportc_lane2y | - | - | - | - | - | - | - |
| AF32 | dsportc_lane3x | - | - | - | - | - | - | - |
| AF31 | dsportc_lane3y | - | - | - | - | - | - | - |
| AE32 | dsportc_lane4x | - | - | - | - | - | - | - |
| AE31 | dsportc_lane4y | - | - | - | - | - | - | - |
| AN13 | rffi_hsync0 | - | - | dispc_data17 | kbd_col5 | - | gpio6_160 | safe_mode |
| AM13 | rffi_te_vsync0 | - | - | dispc_data16 | kbd_row5 | jtag_sel | gpio6_161 | safe_mode |
| AL18 | rffi_re | - | - | dispc_pclk | kbd_col4 | - | gpio6_164 | safe_mode |
| AM18 | rffi_a0 | - | - | dispc_de | kbd_row4 | - | gpio6_165 | safe_mode |
| AL14 | rffi_data8 | - | - | dispc_data8 | kbd_col3 | drm_emu12 | gpio6_174 | safe_mode |
| AM14 | rffi_data9 | - | - | dispc_data9 | kbd_row3 | drm_emu13 | gpio6_175 | safe_mode |
| AM12 | rffi_data10 | - | - | dispc_data10 | kbd_row8 | drm_emu14 | gpio6_176 | safe_mode |
| AL11 | rffi_data11 | - | - | dispc_data11 | kbd_row7 | drm_emu15 | gpio6_177 | safe_mode |
| AM11 | rffi_data12 | - | - | dispc_data12 | kbd_row6 | drm_emu16 | gpio6_178 | safe_mode |
| AN11 | rffi_data13 | - | - | dispc_data13 | kbd_col8 | drm_emu17 | gpio6_179 | safe_mode |
| AL10 | rffi_data14 | - | - | dispc_data14 | kbd_col7 | drm_emu18 | gpio6_180 | safe_mode |
| AM10 | rffi_data15 | mcspi2_cs1 | - | dispc_data15 | kbd_col6 | drm_emu19 | gpio6_181 | safe_mode |
| AN9 | gpio6_182 ⁽²⁾ | - | - | dispc_data18 | kbd_col0 | - | gpio6_182 ⁽²⁾ | safe_mode |
| AM9 | gpio6_183 ⁽²⁾ | - | - | dispc_data19 | kbd_col1 | - | gpio6_183 ⁽²⁾ | safe_mode |
| AL9 | gpio6_184 ⁽²⁾ | - | - | dispc_data20 | kbd_col2 | hw_dbg22 | gpio6_184 ⁽²⁾ | safe_mode |
| AM8 | gpio6_185 ⁽²⁾ | - | - | dispc_data21 | kbd_row0 | hw_dbg23 | gpio6_185 ⁽²⁾ | safe_mode |
| AL8 | gpio6_186 ⁽²⁾ | - | - | dispc_data22 | kbd_row1 | hw_dbg24 | gpio6_186 ⁽²⁾ | safe_mode |
| AN7 | gpio6_187 ⁽²⁾ | - | - | dispc_data23 | kbd_row2 | hw_dbg25 | gpio6_187 ⁽²⁾ | safe_mode |
| AL17 | rffi_data0 | - | - | dispc_data0 | jtagtapext_rtck | drm_emu4 | gpio6_166 | safe_mode |
| AM17 | rffi_data1 | - | - | dispc_data1 | uart3_rx_irrx | drm_emu5 | gpio6_167 | safe_mode |
| AN17 | rffi_data2 | - | - | dispc_data2 | uart3_tx_irtx | drm_emu6 | gpio6_168 | safe_mode |
| AL16 | rffi_data3 | - | - | dispc_data3 | jtagtapext_nrst | drm_emu7 | gpio6_169 | safe_mode |
| AM16 | rffi_data4 | - | - | dispc_data4 | jtagtapext_tck | drm_emu8 | gpio6_170 | safe_mode |
| AL15 | rffi_data5 | - | - | dispc_data5 | jtagtapext_tmisc | drm_emu9 | gpio6_171 | safe_mode |
| AM15 | rffi_data6 | - | - | dispc_data6 | jtagtapext_tdo | drm_emu10 | gpio6_172 | safe_mode |
| AN15 | rffi_data7 | - | - | dispc_data7 | jtagtapext_tdi | drm_emu11 | gpio6_173 | safe_mode |
| AL13 | rffi_cs0 | - | - | dispc_hsync | - | drm_emu3 | gpio6_163 | safe_mode |
| AL12 | rffi_we | - | - | dispc_vsync | - | drm_emu2 | gpio6_162 | safe_mode |
| AF20 | mcspi2_cs0 | jtagtapext_nrst | - | dispc_fid | - | - | gpio7_196 | safe_mode |
| AH17 | mcspi2_clk | jtagtapext_tck | - | - | - | - | gpio7_197 | safe_mode |
| AG20 | mcspi2_simo | jtagtapext_tmisc | - | - | - | hw_dbg20 | gpio7_198 | safe_mode |
| AH20 | mcspi2_somi | jtagtapext_tdo | - | - | - | hw_dbg21 | gpio7_199 | safe_mode |
| AJ21 | i2c4_scl | jtagtapext_tdi | - | - | - | - | gpio7_200 | safe_mode |
| AJ20 | i2c4_sda | jtagtapext_rtck | - | - | - | - | gpio7_201 | safe_mode |
| AE23 | vdds_hdmi | - | - | - | - | - | - | - |
| AN23 | hdmi_cec | - | - | - | - | - | gpio7_192 | safe_mode |
| AM23 | hdmi_hpd | - | - | - | - | - | gpio7_193 | safe_mode |
| AM22 | hdmi_ddc_scl | - | - | - | - | - | gpio7_194 | safe_mode |
| AL23 | hdmi_ddc_sda | - | - | - | - | - | gpio7_195 | safe_mode |
| AN25 | vdda_hdmi | - | - | - | - | - | - | - |
| AK24 | vssa_hdmi | - | - | - | - | - | - | - |
| AL24 | hdmi_clkx | - | - | - | - | - | - | - |
| AM24 | hdmi_clkx | - | - | - | - | - | - | - |
| AL25 | hdmi_data0x | - | - | - | - | - | - | - |
| AM25 | hdmi_data0y | - | - | - | - | - | - | - |
| AL26 | hdmi_data1x | - | - | - | - | - | - | - |

Table 3-2. Multiplexing Characteristics⁽¹⁾ (continued)

| BOTTOM BALLS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|--------------|--------------------------|----------------------|----------------|-------------------|-----------------|-------------|--------------------------|-----------|
| AM26 | hdmi_data1y | - | - | - | - | - | - | - |
| AL27 | hdmi_data2x | - | - | - | - | - | - | - |
| AM27 | hdmi_data2y | - | - | - | - | - | - | - |
| N3 | vdda_csiporta | - | - | - | - | - | - | - |
| P4 | vssa_csiporta | - | - | - | - | - | - | - |
| U6 | csiporta_lane0x | - | - | cpi_pclk | - | - | gpio8_in236 | safe_mode |
| U5 | csiporta_lane0y | - | - | cpi_wen | - | - | gpio8_in237 | safe_mode |
| P5 | csiporta_lane1y | - | - | cpi_data0 | - | - | gpio8_in238 | safe_mode |
| P6 | csiporta_lane1x | - | - | cpi_data1 | - | - | gpio8_in239 | safe_mode |
| P8 | csiporta_lane2y | - | - | cpi_data2 | - | - | gpio8_in240 | safe_mode |
| P7 | csiporta_lane2x | - | - | cpi_data3 | - | - | gpio8_in241 | safe_mode |
| N5 | csiporta_lane3x | - | - | cpi_data4 | - | - | gpio8_in242 | safe_mode |
| N6 | csiporta_lane3y | - | - | cpi_data5 | - | - | gpio8_in243 | safe_mode |
| N7 | csiporta_lane4x | - | - | cpi_data6 | - | - | gpio8_in244 | safe_mode |
| N8 | csiporta_lane4y | - | - | cpi_data7 | - | - | gpio8_in245 | safe_mode |
| AA7 | vdda_csiportb | - | - | - | - | - | - | - |
| Y4 | vssa_csiportb | - | - | - | - | - | - | - |
| Y6 | csiportb_lane0x | - | - | - | cpi_data12 | - | gpio8_in246 | safe_mode |
| Y5 | csiportb_lane0y | - | - | - | cpi_data13 | - | gpio8_in247 | safe_mode |
| Y7 | csiportb_lane1y | - | - | - | cpi_data14 | - | gpio8_in248 | safe_mode |
| Y8 | csiportb_lane1x | - | - | - | cpi_data15 | - | gpio8_in249 | safe_mode |
| AA5 | csiportb_lane2y | - | - | - | cpi_hsyncin | - | gpio8_in250 | safe_mode |
| AA6 | csiportb_lane2x | - | - | - | cpi_vsyncin | - | gpio8_in251 | safe_mode |
| J5 | vdda_csiportc | - | - | - | - | - | - | - |
| K4 | vssa_csiportc | - | - | - | - | - | - | - |
| J6 | csiportc_lane0y | - | - | cpi_data8 | - | - | gpio8_in252 | safe_mode |
| J7 | csiportc_lane0x | - | - | cpi_data9 | - | - | gpio8_in253 | safe_mode |
| K6 | csiportc_lane1y | - | - | cpi_data10 | - | - | gpio8_in254 | safe_mode |
| K5 | csiportc_lane1x | - | - | cpi_data11 | - | - | gpio8_in255 | safe_mode |
| AE6 | cam_shutter | - | - | - | - | sys_nodeid0 | gpio8_224 | safe_mode |
| AE5 | cam_strobe | - | - | - | - | sys_nodeid1 | gpio8_225 | safe_mode |
| AF6 | cam_globalreset | cam_shutter | - | cpi_fid | - | - | gpio8_226 | safe_mode |
| AE7 | timer11_pwm_evt | - | uart_tx | cpi_data12 | - | hw_dbg26 | gpio8_227 | safe_mode |
| AD5 | timer5_pwm_evt | sdcard_cd | uart_cts | cpi_data13 | - | - | gpio8_228 | safe_mode |
| AD6 | timer6_pwm_evt | sdcard_wp | uart_rx | cpi_data14 | - | - | gpio8_229 | safe_mode |
| AD7 | timer8_pwm_evt | sdcard_wp | uart_rts | cpi_data15 | - | hw_dbg27 | gpio8_230 | safe_mode |
| AJ5 | i2c3_scl | - | - | - | - | - | gpio8_231 | safe_mode |
| AH4 | i2c3_sda | - | - | - | - | - | gpio8_232 | safe_mode |
| AG5 | gpio8_233 ⁽²⁾ | sys_secure_indicator | timer8_pwm_evt | cpi_hsync | - | - | gpio8_233 ⁽²⁾ | safe_mode |
| AF5 | gpio8_234 ⁽²⁾ | sys_drm_msecure | - | cpi_vsync | - | - | gpio8_234 ⁽²⁾ | safe_mode |
| W32 | abe_clks | - | - | abemcasp_axr | - | - | gpio4_96 | safe_mode |
| AF28 | abedmic_din1 | - | - | abemcasp_ahclk | abemcbasp3_fsx | - | gpio4_97 | safe_mode |
| AE29 | abedmic_din2 | - | - | abemcasp_axr | abemcbasp3_dx | - | gpio4_98 | safe_mode |
| AE28 | abedmic_din3 | - | - | - | abemcbasp3_dr | - | gpio4_99 | safe_mode |
| AE27 | abedmic_clk1 | - | - | - | abemcbasp3_clkx | - | gpio4_100 | safe_mode |
| AD29 | abedmic_clk2 | abemcbasp1_fsx | - | abemcasp_amutein | - | - | gpio4_101 | safe_mode |
| AD28 | abedmic_clk3 | abemcbasp1_dx | - | abemcasp_aclkx | - | - | gpio4_102 | safe_mode |
| AF29 | reserved | abemcbasp1_clkx | - | abemcasp_afsr | - | - | gpio4_103 | safe_mode |
| AG29 | reserved | abemcbasp1_dr | - | abemcasp_aclkr | - | - | gpio4_104 | safe_mode |
| AD26 | abemcbasp2_dr | - | - | abemcasp_axr | - | - | gpio4_105 | safe_mode |
| AD27 | abemcbasp2_dx | - | - | abemcasp_amuteout | - | - | gpio4_106 | safe_mode |
| AA26 | abemcbasp2_fsx | - | - | abemcasp_afsx | - | - | gpio4_107 | safe_mode |
| AA27 | abemcbasp2_clkx | - | - | abemcasp_ahclkx | - | - | gpio4_108 | safe_mode |
| AA28 | abemcpdm_ul_data | abemcbasp3_dr | - | abemcasp_axr3 | - | - | gpio4_109 | safe_mode |

Table 3-2. Multiplexing Characteristics⁽¹⁾ (continued)

| BOTTOM BALLS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|--------------|-------------------|-----------------|----------|---------------|----------------|--------------------|-----------|-----------|
| AA29 | abemcpdm_dl_data | abemcbasp3_dx | - | abemcasp_axr2 | - | - | gpio4_110 | safe_mode |
| Y29 | abemcpdm_frame | abemcbasp3_clkx | - | abemcasp_axr1 | - | - | gpio4_111 | safe_mode |
| Y28 | abemcpdm_lb_clk | abemcbasp3_fsx | - | - | - | - | gpio4_112 | safe_mode |
| AH25 | wlsdio_clk | mcspi4_clk | - | - | - | - | gpio5_128 | safe_mode |
| AG25 | wlsdio_cmd | - | - | - | - | - | gpio5_129 | safe_mode |
| AJ26 | wlsdio_data0 | mcspi4_simo | - | - | - | - | gpio5_130 | safe_mode |
| AH26 | wlsdio_data1 | mcspi4_somi | - | - | - | - | gpio5_131 | safe_mode |
| AK28 | wlsdio_data2 | mcspi4_cs0 | - | - | - | - | gpio5_132 | safe_mode |
| AJ27 | wlsdio_data3 | - | - | - | - | - | gpio5_133 | safe_mode |
| AL32 | uart5_rx | - | - | - | sdio4_data1 | hw_dbg28 | gpio5_134 | safe_mode |
| AL31 | uart5_tx | - | - | - | sdio4_data2 | hw_dbg29 | gpio5_135 | safe_mode |
| AK31 | uart5_cts | - | - | - | sdio4_data0 | hw_dbg30 | gpio5_136 | safe_mode |
| AK32 | uart5_rts | - | - | - | sdio4_data3 | hw_dbg31 | gpio5_137 | safe_mode |
| AL33 | i2c2_scl | - | - | - | - | - | gpio5_138 | safe_mode |
| AM32 | i2c2_sda | - | - | - | - | - | gpio5_139 | safe_mode |
| AM30 | mcspi1_clk | - | - | - | - | usb0_ulpiphy_clk | gpio5_140 | safe_mode |
| AL30 | mcspi1_somi | - | - | - | - | usb0_ulpiphy_nxt | gpio5_141 | safe_mode |
| AL29 | mcspi1_simo | - | - | - | - | usb0_ulpiphy_dir | gpio5_142 | safe_mode |
| AN31 | mcspi1_cs0 | - | - | - | - | usb0_ulpiphy_data0 | gpio5_143 | safe_mode |
| AM31 | mcspi1_cs1 | - | - | - | - | usb0_ulpiphy_data1 | gpio5_144 | safe_mode |
| AL28 | i2c5_scl | - | uart4_rx | - | - | - | gpio5_147 | safe_mode |
| AM29 | i2c5_sda | - | uart4_tx | - | - | - | gpio5_148 | safe_mode |
| AN29 | uart6_rts | sys_ndmareq0 | - | sdio5_data0 | usbb2_mm_txse0 | usb0_ulpiphy_stp | gpio5_152 | safe_mode |
| AJ25 | uart3_cts_rctx | sata_actled | - | sdio5_data7 | usbb2_mm_txen | usb0_ulpiphy_data4 | gpio5_153 | safe_mode |
| AJ24 | uart3_rts_irsd | hdq_sio | - | sdio5_data6 | usbb2_mm_txdat | usb0_ulpiphy_data5 | gpio5_154 | safe_mode |
| AG24 | uart3_tx_irtx | - | - | sdio5_data5 | sdio4_clk | usb0_ulpiphy_data6 | gpio5_155 | safe_mode |
| AH24 | uart3_rx_irrx | - | - | sdio5_data4 | sdio4_cmd | usb0_ulpiphy_data7 | gpio5_156 | safe_mode |
| K26 | usbb3_hsic_strobe | - | - | - | - | - | gpio5_158 | safe_mode |
| K27 | usbb3_hsic_data | - | - | - | - | - | gpio5_159 | safe_mode |
| E9 | vdda_sata | - | - | - | - | - | - | - |
| D10 | vssa_sata | - | - | - | - | - | - | - |
| G9 | sata_tx | - | - | - | - | - | - | - |
| F9 | sata_ty | - | - | - | - | - | - | - |
| E10 | sata_rx | - | - | - | - | - | - | - |
| F10 | sata_ry | - | - | - | - | - | - | - |
| E5 | vdds_sdcard | - | - | - | - | - | - | - |
| F8 | sdcard_clk | - | - | jtag_rtck | - | n_clk | - | safe_mode |
| E8 | sdcard_cmd | - | - | jtag_tdo | uart6_rx | - | n_d2 | safe_mode |
| H6 | sdcard_data0 | - | - | jtag_tdi | - | n_d0 | - | safe_mode |
| H5 | sdcard_data1 | - | - | jtag_nrst | - | n_d1 | - | safe_mode |
| G5 | sdcard_data2 | - | - | jtag_tmisc | - | n_d2 | - | safe_mode |
| E7 | sdcard_data3 | - | - | jtag_tck | - | n_d3 | - | safe_mode |
| AE18 | vdds_usbhs18 | - | - | - | - | - | - | - |
| AN21 | vdda_usbhs33 | - | - | - | - | - | - | - |
| AK20 | vssa_usbhs | - | - | - | - | - | - | - |
| AL19 | usb0_hs_dp | - | - | - | uart3_rx_irrx | - | - | safe_mode |
| AM19 | usb0_hs_dm | - | - | - | uart3_tx_irtx | - | - | safe_mode |
| AN19 | usbphy_ce | - | - | - | - | - | - | - |
| AE19 | vdda_usbss18 | - | - | - | - | - | - | - |
| AK21 | vssa_usbss | - | - | - | - | - | - | - |
| AL20 | usb0_ss_tx | - | - | - | - | - | - | - |
| AM20 | usb0_ss_ty | - | - | - | - | - | - | - |
| AL21 | usb0_ss_rx | - | - | - | - | - | - | - |
| AM21 | usb0_ss_ry | - | - | - | - | - | - | - |
| K32 | drm_emu0 | - | - | - | - | hw_wkdbg6 | gpio1_wk6 | safe_mode |
| K31 | drm_emu1 | - | - | - | - | hw_wkdbg7 | gpio1_wk7 | safe_mode |

Table 3-2. Multiplexing Characteristics⁽¹⁾ (continued)

| BOTTOM BALLS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|--------------|----------------|--------|--------|----------|-----------|------------|--------------|-----------|
| B32 | jtag_nrst | - | - | - | - | - | - | safe_mode |
| C31 | jtag_tck | - | - | - | - | - | - | safe_mode |
| B33 | jtag_rtck | - | - | - | - | - | - | safe_mode |
| B31 | jtag_tmssc | - | - | - | - | - | - | safe_mode |
| A32 | jtag_tdi | - | - | - | - | - | - | safe_mode |
| A33 | jtag_tdo | - | - | - | - | - | - | safe_mode |
| L31 | sys_32k | - | - | - | - | - | - | - |
| J24 | vdds_osc | - | - | - | - | - | - | - |
| L30 | vssa_xtal | - | - | - | - | - | - | - |
| L32 | fref_xtal_in | - | - | - | - | - | - | - |
| M32 | fref_xtal_out | - | - | - | - | - | - | - |
| L33 | fref_xtal_clk | - | - | - | - | - | - | - |
| N31 | fref_clk_ioreq | - | - | - | - | - | gpio1_wk13 | safe_mode |
| M31 | fref_clk0_out | - | - | - | - | hw_wkdbg9 | gpio1_wk12 | safe_mode |
| P31 | fref_clk1_out | - | - | - | - | hw_wkdbg5 | gpio1_wk11 | safe_mode |
| N33 | sys_nrespwrn | - | - | - | - | - | - | - |
| N32 | sys_nreswarm | - | - | - | - | - | - | - |
| T31 | sys_pwr_req | - | - | - | - | hw_wkdbg15 | - | safe_mode |
| R32 | sr_pmic_scl | - | - | - | - | - | - | - |
| R31 | sr_pmic_sda | - | - | - | - | - | - | - |
| R33 | sys_nirq1 | - | - | - | - | - | gpio1_wk16 | - |
| T32 | sys_nirq2 | - | - | - | - | - | gpio1_wk17 | - |
| P29 | i2c1_pmic_scl | - | - | - | - | - | - | - |
| P28 | i2c1_pmic_sda | - | - | - | - | - | - | - |
| U31 | sys_boot0 | - | - | drm_emu2 | drm_emu15 | hw_wkdbg0 | gpio1_wkout0 | safe_mode |
| U32 | sys_boot1 | - | - | drm_emu3 | drm_emu16 | hw_wkdbg1 | gpio1_wkout1 | safe_mode |
| U33 | sys_boot2 | - | - | drm_emu4 | drm_emu17 | hw_wkdbg2 | gpio1_wkout2 | safe_mode |
| V31 | sys_boot3 | - | - | drm_emu5 | drm_emu18 | hw_wkdbg3 | gpio1_wkout3 | safe_mode |
| V32 | sys_boot4 | - | - | drm_emu6 | drm_emu19 | hw_wkdbg4 | gpio1_wkout4 | safe_mode |
| A29 | ddrch1_dm0 | - | - | - | - | - | - | - |
| B24 | ddrch1_dm1 | - | - | - | - | - | - | - |
| C30 | ddrch1_dm2 | - | - | - | - | - | - | - |
| B6 | ddrch1_dm3 | - | - | - | - | - | - | - |
| C28 | ddrch1_dq0 | - | - | - | - | - | - | - |
| A31 | ddrch1_dq1 | - | - | - | - | - | - | - |
| C29 | ddrch1_dq2 | - | - | - | - | - | - | - |
| B30 | ddrch1_dq3 | - | - | - | - | - | - | - |
| B29 | ddrch1_dq4 | - | - | - | - | - | - | - |
| C26 | ddrch1_dq5 | - | - | - | - | - | - | - |
| B28 | ddrch1_dq6 | - | - | - | - | - | - | - |
| B26 | ddrch1_dq7 | - | - | - | - | - | - | - |
| C23 | ddrch1_dq8 | - | - | - | - | - | - | - |
| C22 | ddrch1_dq9 | - | - | - | - | - | - | - |
| C21 | ddrch1_dq10 | - | - | - | - | - | - | - |
| B22 | ddrch1_dq11 | - | - | - | - | - | - | - |
| C24 | ddrch1_dq12 | - | - | - | - | - | - | - |
| C25 | ddrch1_dq13 | - | - | - | - | - | - | - |
| B25 | ddrch1_dq14 | - | - | - | - | - | - | - |
| A25 | ddrch1_dq15 | - | - | - | - | - | - | - |
| E31 | ddrch1_dq16 | - | - | - | - | - | - | - |
| E33 | ddrch1_dq17 | - | - | - | - | - | - | - |
| E32 | ddrch1_dq18 | - | - | - | - | - | - | - |
| F32 | ddrch1_dq19 | - | - | - | - | - | - | - |
| C33 | ddrch1_dq20 | - | - | - | - | - | - | - |
| D30 | ddrch1_dq21 | - | - | - | - | - | - | - |
| F31 | ddrch1_dq22 | - | - | - | - | - | - | - |

Table 3-2. Multiplexing Characteristics⁽¹⁾ (continued)

| BOTTOM BALLS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|--|------------------|--------|--------|--------|--------|--------|--------|--------|
| C32 | ddrch1_dq23 | - | - | - | - | - | - | - |
| C6 | ddrch1_dq24 | - | - | - | - | - | - | - |
| A5 | ddrch1_dq25 | - | - | - | - | - | - | - |
| B5 | ddrch1_dq26 | - | - | - | - | - | - | - |
| C5 | ddrch1_dq27 | - | - | - | - | - | - | - |
| B2 | ddrch1_dq28 | - | - | - | - | - | - | - |
| B3 | ddrch1_dq29 | - | - | - | - | - | - | - |
| C3 | ddrch1_dq30 | - | - | - | - | - | - | - |
| D4 | ddrch1_dq31 | - | - | - | - | - | - | - |
| C27 | ddrch1_dqs0 | - | - | - | - | - | - | - |
| B23 | ddrch1_dqs1 | - | - | - | - | - | - | - |
| D31 | ddrch1_dqs2 | - | - | - | - | - | - | - |
| C4 | ddrch1_dqs3 | - | - | - | - | - | - | - |
| B27 | ddrch1_ndqs0 | - | - | - | - | - | - | - |
| A23 | ddrch1_ndqs1 | - | - | - | - | - | - | - |
| D32 | ddrch1_ndqs2 | - | - | - | - | - | - | - |
| B4 | ddrch1_ndqs3 | - | - | - | - | - | - | - |
| A19 | ddrch1_vref_dq | - | - | - | - | - | - | - |
| J16 | vddq_vref_ddrch1 | - | - | - | - | - | - | - |
| A27 / A11 / A3 / H30 / H10 / J19 / J18 / J10 / K30 / K25 / K23 / K15 / K14 / L25 / M25 / A21 | vdds_ddrch1 | - | - | - | - | - | - | - |
| J1 | ddrch2_dm0 | - | - | - | - | - | - | - |
| AJ3 | ddrch2_dm1 | - | - | - | - | - | - | - |
| G1 | ddrch2_dm2 | - | - | - | - | - | - | - |
| AL4 | ddrch2_dm3 | - | - | - | - | - | - | - |
| K3 | ddrch2_dq0 | - | - | - | - | - | - | - |
| H2 | ddrch2_dq1 | - | - | - | - | - | - | - |
| H3 | ddrch2_dq2 | - | - | - | - | - | - | - |
| J3 | ddrch2_dq3 | - | - | - | - | - | - | - |
| J2 | ddrch2_dq4 | - | - | - | - | - | - | - |
| M3 | ddrch2_dq5 | - | - | - | - | - | - | - |
| L2 | ddrch2_dq6 | - | - | - | - | - | - | - |
| L1 | ddrch2_dq7 | - | - | - | - | - | - | - |
| AK3 | ddrch2_dq8 | - | - | - | - | - | - | - |
| AG1 | ddrch2_dq9 | - | - | - | - | - | - | - |
| AH3 | ddrch2_dq10 | - | - | - | - | - | - | - |
| AJ2 | ddrch2_dq11 | - | - | - | - | - | - | - |
| AH2 | ddrch2_dq12 | - | - | - | - | - | - | - |
| AL1 | ddrch2_dq13 | - | - | - | - | - | - | - |
| AL3 | ddrch2_dq14 | - | - | - | - | - | - | - |
| AK4 | ddrch2_dq15 | - | - | - | - | - | - | - |
| G3 | ddrch2_dq16 | - | - | - | - | - | - | - |
| D3 | ddrch2_dq17 | - | - | - | - | - | - | - |
| C2 | ddrch2_dq18 | - | - | - | - | - | - | - |
| C1 | ddrch2_dq19 | - | - | - | - | - | - | - |
| D2 | ddrch2_dq20 | - | - | - | - | - | - | - |
| F2 | ddrch2_dq21 | - | - | - | - | - | - | - |
| G2 | ddrch2_dq22 | - | - | - | - | - | - | - |
| F3 | ddrch2_dq23 | - | - | - | - | - | - | - |
| AM3 | ddrch2_dq24 | - | - | - | - | - | - | - |
| AL5 | ddrch2_dq25 | - | - | - | - | - | - | - |
| AM4 | ddrch2_dq26 | - | - | - | - | - | - | - |
| AN3 | ddrch2_dq27 | - | - | - | - | - | - | - |
| AL7 | ddrch2_dq28 | - | - | - | - | - | - | - |
| AL6 | ddrch2_dq29 | - | - | - | - | - | - | - |
| AM7 | ddrch2_dq30 | - | - | - | - | - | - | - |

Table 3-2. Multiplexing Characteristics⁽¹⁾ (continued)

| BOTTOM BALLS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---|------------------|--------|--------|--------|--------|--------|--------|--------|
| AM6 | ddrch2_dq31 | - | - | - | - | - | - | - |
| K2 | ddrch2_dqs0 | - | - | - | - | - | - | - |
| AK2 | ddrch2_dqs1 | - | - | - | - | - | - | - |
| E2 | ddrch2_dqs2 | - | - | - | - | - | - | - |
| AM5 | ddrch2_dqs3 | - | - | - | - | - | - | - |
| L3 | ddrch2_ndqs0 | - | - | - | - | - | - | - |
| AL2 | ddrch2_ndqs1 | - | - | - | - | - | - | - |
| E3 | ddrch2_ndqs2 | - | - | - | - | - | - | - |
| AN5 | ddrch2_ndqs3 | - | - | - | - | - | - | - |
| U1 | ddrch2_vref_dq | - | - | - | - | - | - | - |
| V10 | vddq_vref_ddrch2 | - | - | - | - | - | - | - |
| E1 / J9 / K8 / N1 / R9 / T9 / V9 / W9 / AA1 / AC10 / AE12 / AE11 / AE10 / AJ1 / AM2 | vdds_ddr_ch2 | - | - | - | - | - | - | - |
| A7 | ddr3ch1_a0 | - | - | - | - | - | - | - |
| B7 | ddr3ch1_a1 | - | - | - | - | - | - | - |
| C7 | ddr3ch1_a2 | - | - | - | - | - | - | - |
| B8 | ddr3ch1_a3 | - | - | - | - | - | - | - |
| C8 | ddr3ch1_a4 | - | - | - | - | - | - | - |
| B9 | ddr3ch1_a5 | - | - | - | - | - | - | - |
| C10 | ddr3ch1_a6 | - | - | - | - | - | - | - |
| B12 | ddr3ch1_a7 | - | - | - | - | - | - | - |
| C12 | ddr3ch1_a8 | - | - | - | - | - | - | - |
| A13 | ddr3ch1_a9 | - | - | - | - | - | - | - |
| B13 | ddr3ch1_a10_ap | - | - | - | - | - | - | - |
| C13 | ddr3ch1_a11 | - | - | - | - | - | - | - |
| B14 | ddr3ch1_a12_nbc | - | - | - | - | - | - | - |
| C14 | ddr3ch1_a13 | - | - | - | - | - | - | - |
| A15 | ddr3ch1_a14 | - | - | - | - | - | - | - |
| B15 | ddr3ch1_a15 | - | - | - | - | - | - | - |
| C11 | ddr3ch1_cka | - | - | - | - | - | - | - |
| C18 | ddr3ch1_ckb | - | - | - | - | - | - | - |
| C9 | ddr3ch1_cke0 | - | - | - | - | - | - | - |
| A17 | ddr3ch1_cke1 | - | - | - | - | - | - | - |
| B11 | ddr3ch1_ncka | - | - | - | - | - | - | - |
| B18 | ddr3ch1_nckb | - | - | - | - | - | - | - |
| B10 | ddr3ch1_ncs0 | - | - | - | - | - | - | - |
| B17 | ddr3ch1_ncs1 | - | - | - | - | - | - | - |
| C15 | ddr3ch1_ba0 | - | - | - | - | - | - | - |
| B16 | ddr3ch1_ba1 | - | - | - | - | - | - | - |
| C16 | ddr3ch1_ba2 | - | - | - | - | - | - | - |
| C17 | ddr3ch1_ncas | - | - | - | - | - | - | - |
| B19 | ddr3ch1_nras | - | - | - | - | - | - | - |
| C19 | ddr3ch1_nreset | - | - | - | - | - | - | - |
| B20 | ddr3ch1_nwe | - | - | - | - | - | - | - |
| C20 | ddr3ch1_odt0 | - | - | - | - | - | - | - |
| B21 | ddr3ch1_odt1 | - | - | - | - | - | - | - |
| A9 | ddr3ch1_vref_ca | - | - | - | - | - | - | - |
| AG2 | ddr3ch2_a0 | - | - | - | - | - | - | - |
| AG3 | ddr3ch2_a1 | - | - | - | - | - | - | - |
| AF2 | ddr3ch2_a2 | - | - | - | - | - | - | - |
| AF3 | ddr3ch2_a3 | - | - | - | - | - | - | - |
| AE2 | ddr3ch2_a4 | - | - | - | - | - | - | - |
| AE3 | ddr3ch2_a5 | - | - | - | - | - | - | - |
| AC3 | ddr3ch2_a6 | - | - | - | - | - | - | - |
| AB2 | ddr3ch2_a7 | - | - | - | - | - | - | - |
| AB3 | ddr3ch2_a8 | - | - | - | - | - | - | - |

Table 3-2. Multiplexing Characteristics⁽¹⁾ (continued)

| BOTTOM BALLS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---|-------------------------|--------|--------|--------|--------|--------|--------|--------|
| AA2 | ddr3ch2_a9 | - | - | - | - | - | - | - |
| AA3 | ddr3ch2_a10_ap | - | - | - | - | - | - | - |
| Y2 | ddr3ch2_a11 | - | - | - | - | - | - | - |
| Y3 | ddr3ch2_a12_nbc | - | - | - | - | - | - | - |
| W1 | ddr3ch2_a13 | - | - | - | - | - | - | - |
| W2 | ddr3ch2_a14 | - | - | - | - | - | - | - |
| W3 | ddr3ch2_a15 | - | - | - | - | - | - | - |
| AC2 | ddr3ch2_cka | - | - | - | - | - | - | - |
| R2 | ddr3ch2_ckb | - | - | - | - | - | - | - |
| AD2 | ddr3ch2_cke0 | - | - | - | - | - | - | - |
| U3 | ddr3ch2_cke1 | - | - | - | - | - | - | - |
| AC1 | ddr3ch2_ncka | - | - | - | - | - | - | - |
| R1 | ddr3ch2_nckb | - | - | - | - | - | - | - |
| AD3 | ddr3ch2_ncs0 | - | - | - | - | - | - | - |
| T2 | ddr3ch2_ncs1 | - | - | - | - | - | - | - |
| V2 | ddr3ch2_ba0 | - | - | - | - | - | - | - |
| V3 | ddr3ch2_ba1 | - | - | - | - | - | - | - |
| U2 | ddr3ch2_ba2 | - | - | - | - | - | - | - |
| T3 | ddr3ch2_ncas | - | - | - | - | - | - | - |
| R3 | ddr3ch2_nras | - | - | - | - | - | - | - |
| P2 | ddr3ch2_nreset | - | - | - | - | - | - | - |
| P3 | ddr3ch2_nwe | - | - | - | - | - | - | - |
| N2 | ddr3ch2_odt0 | - | - | - | - | - | - | - |
| M2 | ddr3ch2_odt1 | - | - | - | - | - | - | - |
| AE1 | ddr3ch2_vref_ca | - | - | - | - | - | - | - |
| J11 / K22 / K12 / K11 / K9 / L14 / L13 / L12 / L10 / M14 / M13 / M11 / M10 / N15 / N14 / N11 / P11 / W24 / W22 / Y24 / Y23 / AA23 / AB24 / AB23 / AC24 / AC22 / AC21 / AD23 / AD22 / AD20 / AD16 / AD15 / AD14 / AD12 | vdd_core | - | - | - | - | - | - | - |
| AH21 | vdd_core_sense | - | - | - | - | - | - | - |
| T14 / T13 / T11 / T10 / W13 / W12 / W10 / Y19 / Y15 / Y11 / Y10 / AA19 / AA16 / AA15 / AA11 / AB19 / AB15 / AB13 / AB11 / AB10 / AC20 / AC16 / AC14 / AC13 / AC12 / AD19 / AD11 | vdd_mm | - | - | - | - | - | - | - |
| AG21 | vdd_mm_sense | - | - | - | - | - | - | - |
| K20 / K19 / K18 / L24 / L22 / L21 / L20 / L18 / M24 / M23 / M20 / M19 / N23 / N18 / P24 / P23 / P22 / P18 / R24 / T24 / T23 / T21 / T20 | vdd_mpu | - | - | - | - | - | - | - |
| U29 | vdd_mpu_sense | - | - | - | - | - | - | - |
| AJ29 | vss_mpu_sense | - | - | - | - | - | - | - |
| AD9 | vpp1 | - | - | - | - | - | - | - |
| D28 / D26 / D24 / D23 / D21 / D20 / D18 / D16 / D14 / D13 / D11 / D8 / D6 / F4 / H4 / L16 / L4 / M21 / M17 / M15 / N30 / N22 / N21 / N20 / N19 / N17 / N16 / N13 / N12 / N4 / P30 / P21 / P19 / P16 / P15 / P13 / P12 / P10 / P9 / R22 / R21 / R20 / R19 / R18 / R17 / R16 / R15 / R14 / R13 / R12 / R10 / T30 / T19 / T17 / T15 / T4 / U22 / U21 / U19 / U18 / U17 / U16 / U15 / U13 / U12 / V30 / V24 / V23 / V21 / V20 / V19 / V17 / V15 / V14 / V13 / V11 / V4 / W21 / W20 / W19 / W18 / W17 / W16 / W15 / W14 / Y22 / Y21 / Y18 / Y16 / Y13 / Y12 / AA30 / AA22 / AA21 / AA20 / AA18 / AA17 / AA14 / AA13 / AA12 / AA4 / AB21 / AB20 / AB17 / AB14 / AC30 / AC18 / AC4 / AD4 / AF30 / AF4 / AH30 / AK26 / AK23 / AK14 / AK13 / F30 / AK11 / AK10 / AK8 / AK6 | vss | - | - | - | - | - | - | - |
| Y26 | vdda_dppll_core_emu_abe | - | - | - | - | - | - | - |

Table 3-2. Multiplexing Characteristics⁽¹⁾ (continued)

| BOTTOM BALLS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|--------------|------------------------------|--------|--------|--------|--------|--------|--------|--------|
| U8 | vdda_dpll_mm_l4per | - | - | - | - | - | - | - |
| AF24 | vdda_dpll_hdmi | - | - | - | - | - | - | - |
| Y27 | vdda_dpll_mpu | - | - | - | - | - | - | - |
| AE22 | vdda_ldo_core | - | - | - | - | - | - | - |
| AE20 | vdda_ldo_mm | - | - | - | - | - | - | - |
| J15 | vdda_ldo_mpu | - | - | - | - | - | - | - |
| N25 | vdda_ldo_emu_wkup | - | - | - | - | - | - | - |
| AE16 | vdda_vbgap_core | - | - | - | - | - | - | - |
| T25 | cap_vdda_ldo_sram_core_array | - | - | - | - | - | - | - |
| AG17 | cap_vdda_ldo_sram_mm_array | - | - | - | - | - | - | - |
| H17 | cap_vdda_ldo_sram_mpu_array | - | - | - | - | - | - | - |
| V25 | cap_vddldo_emu_wkup | - | - | - | - | - | - | - |
| AD18 | cap_vbb_ldo_mm | - | - | - | - | - | - | - |
| H13 | cap_vbb_ldo_mpu | - | - | - | - | - | - | - |
| K16 | cap_vdda_ldo_sram_mpu_array2 | - | - | - | - | - | - | - |

(1) NA in table stands for not applicable.

(2) gpio6_182, gpio6_183, gpio6_184, gpio6_185, gpio6_186, gpio6_187, gpio8_233, gpio8_234 GPIOs (balls AJ10 / AK10 / AJ11 / AK11 / AJ12 / AK12 / AC2 / AC3) can output the same GPIO in mode 0 or in mode 6.

3.4 Signal Descriptions

Many signals are available on multiple balls, according to the software configuration of the ball multiplexing options.

1. **SIGNAL NAME:** The name of the signal passing through the ball.

NOTE

The subsystem multiplexing signals are not described in [Table 3-1](#) and [Table 3-2](#).

2. **DESCRIPTION:** Description of the signal
3. **TYPE:** Signal direction and type:
 - I = Input
 - O = Output
 - IO = Input or output
 - D = Open Drain
 - DS = Differential
 - A = Analog
 - PWR = Power
 - GND = Ground
4. **BALL BOTTOM:** Associated ball(s) bottom
5. **PIN NAME:** This is the name of the ball the signal is passing through.

3.4.1 External Memory Interfaces

3.4.1.1 GPMC

NOTE

For more information, see the Memory Subsystem / General-Purpose Memory Controller section of the Device TRM.

Table 3-3. GPMC Signal Descriptions

| SIGNAL NAME [1] | PIN NAME [5] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|---------------------------------|--------------|-----------------------------------|----------|-----------------|
| Multiplexed GPMC Mode | | | | |
| gpmc_a1 / gpmc_d0 | gpmc_ad0 | GPMC address bit 1 / data bit 0 | IO | J27 |
| gpmc_a2 / gpmc_d1 | gpmc_ad1 | GPMC address bit 2 / data bit 1 | IO | H28 |
| gpmc_a3 / gpmc_d2 | gpmc_ad2 | GPMC address bit 3 / data bit 2 | IO | H29 |
| gpmc_a4 / gpmc_d3 | gpmc_ad3 | GPMC address bit 4 / data bit 3 | IO | G29 |
| gpmc_a5 / gpmc_d4 | gpmc_ad4 | GPMC address bit 5 / data bit 4 | IO | E29 |
| gpmc_a6 / gpmc_d5 | gpmc_ad5 | GPMC address bit 6 / data bit 5 | IO | E27 |
| gpmc_a7 / gpmc_d6 | gpmc_ad6 | GPMC address bit 7 / data bit 6 | IO | F26 |
| gpmc_a8 / gpmc_d7 | gpmc_ad7 | GPMC address bit 8 / data bit 7 | IO | E26 |
| gpmc_a9 / gpmc_d8 | gpmc_ad8 | GPMC address bit 9 / data bit 8 | IO | J32 |
| gpmc_a10 / gpmc_d9 | gpmc_ad9 | GPMC address bit 10 / data bit 9 | IO | J33 |
| gpmc_a11 / gpmc_d10 | gpmc_ad10 | GPMC address bit 11 / data bit 10 | IO | H32 |
| gpmc_a12 / gpmc_d11 | gpmc_ad11 | GPMC address bit 12 / data bit 11 | IO | J31 |
| gpmc_a13 / gpmc_d12 | gpmc_ad12 | GPMC address bit 13 / data bit 12 | IO | G31 |
| gpmc_a14 / gpmc_d13 | gpmc_ad13 | GPMC address bit 14 / data bit 13 | IO | H31 |
| gpmc_a15 / gpmc_d14 | gpmc_ad14 | GPMC address bit 15 / data bit 14 | IO | G32 |
| gpmc_a16 / gpmc_d15 | gpmc_ad15 | GPMC address bit 16 / data bit 15 | IO | G33 |
| gpmc_a17 | gpmc_a16 | GPMC address bit 17 | O | G24 |
| gpmc_a18 | gpmc_a17 | GPMC address bit 18 | O | H24 |
| gpmc_a19 | gpmc_a18 | GPMC address bit 19 | O | E24 |
| gpmc_a20 | gpmc_a19 | GPMC address bit 20 | O | F24 |
| gpmc_a21 | gpmc_a20 | GPMC address bit 21 | O | G21 |
| gpmc_a22 | gpmc_a21 | GPMC address bit 22 | O | H21 |
| gpmc_a23 | gpmc_a22 | GPMC address bit 23 | O | E21 |
| gpmc_a24 | gpmc_a23 | GPMC address bit 24 | O | F21 |
| gpmc_a25 | gpmc_a24 | GPMC address bit 25 | O | F17 |
| gpmc_a26 | gpmc_a25 | GPMC address bit 26 | O | E20 |
| Nonmultiplexed GPMC Mode | | | | |
| gpmc_d0 | gpmc_ad0 | GPMC data bit 0 | IO | J27 |
| gpmc_d1 | gpmc_ad1 | GPMC data bit 1 | IO | H28 |
| gpmc_d2 | gpmc_ad2 | GPMC data bit 2 | IO | H29 |
| gpmc_d3 | gpmc_ad3 | GPMC data bit 3 | IO | G29 |
| gpmc_d4 | gpmc_ad4 | GPMC data bit 4 | IO | E29 |
| gpmc_d5 | gpmc_ad5 | GPMC data bit 5 | IO | E27 |
| gpmc_d6 | gpmc_ad6 | GPMC data bit 6 | IO | F26 |
| gpmc_d7 | gpmc_ad7 | GPMC data bit 7 | IO | E26 |
| gpmc_d8 | gpmc_ad8 | GPMC data bit 8 | IO | J32 |
| gpmc_d9 | gpmc_ad9 | GPMC data bit 9 | IO | J33 |
| gpmc_d10 | gpmc_ad10 | GPMC data bit 10 | IO | H32 |
| gpmc_d11 | gpmc_ad11 | GPMC data bit 11 | IO | J31 |
| gpmc_d12 | gpmc_ad12 | GPMC data bit 12 | IO | G31 |
| gpmc_d13 | gpmc_ad13 | GPMC data bit 13 | IO | H31 |
| gpmc_d14 | gpmc_ad14 | GPMC data bit 14 | IO | G32 |
| gpmc_d15 | gpmc_ad15 | GPMC data bit 15 | IO | G33 |
| gpmc_a1 | gpmc_a16 | GPMC address bit 1 | O | G24 |
| gpmc_a2 | gpmc_a17 | GPMC address bit 2 | O | H24 |
| gpmc_a3 | gpmc_a18 | GPMC address bit 3 | O | E24 |

Table 3-3. GPMC Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN NAME [5] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|----------------------------|---------------|---|----------|-------------------|
| gpmc_a4 | gpmc_a19 | GPMC address bit 4 | O | F24 |
| gpmc_a5 | gpmc_a20 | GPMC address bit 5 | O | G21 |
| gpmc_a6 | gpmc_a21 | GPMC address bit 6 | O | H21 |
| gpmc_a7 | gpmc_a22 | GPMC address bit 7 | O | E21 |
| gpmc_a8 | gpmc_a23 | GPMC address bit 8 | O | F21 |
| gpmc_a9 | gpmc_a24 | GPMC address bit 9 | O | F17 |
| gpmc_a10 | gpmc_a25 | GPMC address bit 10 | O | E20 |
| Common GPMC Signals | | | | |
| gpmc_ncs0 | gpmc_ncs0 | GPMC chip select 0 invert | O | P32 |
| gpmc_ncs1 | gpmc_ncs1 | GPMC chip select 1 invert | O | F20 |
| gpmc_ncs2 | gpmc_ncs2 | GPMC chip select 2 invert | O | F14 |
| gpmc_ncs3 | gpmc_ncs3 | GPMC chip select 3 invert | O | G14 |
| gpmc_ncs4 | gpmc_ncs4 | GPMC chip select 4 invert | O | E17 |
| gpmc_ncs5 | gpmc_ncs5 | GPMC chip select 5 invert | O | G13 |
| gpmc_ncs6 | gpmc_ncs6 | GPMC chip select 6 invert | O | E13 |
| gpmc_ncs7 | gpmc_ncs7 | GPMC chip select 7 invert | O | NA ⁽¹⁾ |
| gpmc_nwp | gpmc_nwp | GPMC flash write protect invert | O | J29 |
| gpmc_clk | gpmc_clk | GPMC clock | O | J28 |
| gpmc_nadv_ale | gpmc_nadv_ale | GPMC address valid invert or address latch enable | O | E25 |
| gpmc_noe_nre | gpmc_noe | GPMC output enable invert or read enable | O | N9 |
| gpmc_nwe | gpmc_nwe | GPMC write enable invert | O | F13 |
| gpmc_nbe0_cle | gpmc_nbe0_cle | GPMC lower-byte enable invert | O | F25 |
| gpmc_nbe1 | gpmc_nbe1 | GPMC upper-byte enable invert | O | J29 |
| gpmc_wait0 | gpmc_wait0 | GPMC external indication of wait 0 | I | N27 |
| gpmc_wait1 | gpmc_wait1 | GPMC external indication of wait 1 | I | G20 |
| gpmc_wait2 | gpmc_wait2 | GPMC external indication of wait 2 | I | E14 |
| gpmc_wait3 | gpmc_wait3 | GPMC external indication of wait 3 | I | NA ⁽¹⁾ |

(1) NA in this table stands for not applicable for the device.

3.4.1.2 DDR3 and DDR3L

NOTE

For more information, see the Memory Subsystem / EMIF Controller section of the Device TRM.

Table 3-4. DDR3 and DDR3L Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|---------------------------------|--|----------|-----------------|
| DDR3 and DDR3L Channel 1 | | | |
| ddrch1_dm0 | DDR3 and DDR3L channel 1 data mask 0 | IO | A29 |
| ddrch1_dm1 | DDR3 and DDR3L channel 1 data mask 1 | IO | B24 |
| ddrch1_dm2 | DDR3 and DDR3L channel 1 data mask 2 | IO | C30 |
| ddrch1_dm3 | DDR3 and DDR3L channel 1 data mask 3 | IO | B6 |
| ddrch1_dq0 | DDR3 and DDR3L channel 1 data bit 0 | IO | C28 |
| ddrch1_dq1 | DDR3 and DDR3L channel 1 data bit 1 | IO | A31 |
| ddrch1_dq2 | DDR3 and DDR3L channel 1 data bit 2 | IO | C29 |
| ddrch1_dq3 | DDR3 and DDR3L channel 1 data bit 3 | IO | B30 |
| ddrch1_dq4 | DDR3 and DDR3L channel 1 data bit 4 | IO | B29 |
| ddrch1_dq5 | DDR3 and DDR3L channel 1 data bit 5 | IO | C26 |
| ddrch1_dq6 | DDR3 and DDR3L channel 1 data bit 6 | IO | B28 |
| ddrch1_dq7 | DDR3 and DDR3L channel 1 data bit 7 | IO | B26 |
| ddrch1_dq8 | DDR3 and DDR3L channel 1 data bit 8 | IO | C23 |
| ddrch1_dq9 | DDR3 and DDR3L channel 1 data bit 9 | IO | C22 |
| ddrch1_dq10 | DDR3 and DDR3L channel 1 data bit 10 | IO | C21 |
| ddrch1_dq11 | DDR3 and DDR3L channel 1 data bit 11 | IO | B22 |
| ddrch1_dq12 | DDR3 and DDR3L channel 1 data bit 12 | IO | C24 |
| ddrch1_dq13 | DDR3 and DDR3L channel 1 data bit 13 | IO | C25 |
| ddrch1_dq14 | DDR3 and DDR3L channel 1 data bit 14 | IO | B25 |
| ddrch1_dq15 | DDR3 and DDR3L channel 1 data bit 15 | IO | A25 |
| ddrch1_dq16 | DDR3 and DDR3L channel 1 data bit 16 | IO | E31 |
| ddrch1_dq17 | DDR3 and DDR3L channel 1 data bit 17 | IO | E33 |
| ddrch1_dq18 | DDR3 and DDR3L channel 1 data bit 18 | IO | E32 |
| ddrch1_dq19 | DDR3 and DDR3L channel 1 data bit 19 | IO | F32 |
| ddrch1_dq20 | DDR3 and DDR3L channel 1 data bit 20 | IO | C33 |
| ddrch1_dq21 | DDR3 and DDR3L channel 1 data bit 21 | IO | D30 |
| ddrch1_dq22 | DDR3 and DDR3L channel 1 data bit 22 | IO | F31 |
| ddrch1_dq23 | DDR3 and DDR3L channel 1 data bit 23 | IO | C32 |
| ddrch1_dq24 | DDR3 and DDR3L channel 1 data bit 24 | IO | C6 |
| ddrch1_dq25 | DDR3 and DDR3L channel 1 data bit 25 | IO | A5 |
| ddrch1_dq26 | DDR3 and DDR3L channel 1 data bit 26 | IO | B5 |
| ddrch1_dq27 | DDR3 and DDR3L channel 1 data bit 27 | IO | C5 |
| ddrch1_dq28 | DDR3 and DDR3L channel 1 data bit 28 | IO | B2 |
| ddrch1_dq29 | DDR3 and DDR3L channel 1 data bit 29 | IO | B3 |
| ddrch1_dq30 | DDR3 and DDR3L channel 1 data bit 30 | IO | C3 |
| ddrch1_dq31 | DDR3 and DDR3L channel 1 data bit 31 | IO | D4 |
| ddrch1_dqs0 | DDR3 and DDR3L channel 1 data strobe 0 | IO | C27 |
| ddrch1_dqs1 | DDR3 and DDR3L channel 1 data strobe 1 | IO | B23 |
| ddrch1_dqs2 | DDR3 and DDR3L channel 1 data strobe 2 | IO | D31 |
| ddrch1_dqs3 | DDR3 and DDR3L channel 1 data strobe 3 | IO | C4 |

Table 3-4. DDR3 and DDR3L Signal Descriptions (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|---------------------------------|---|----------|-----------------|
| ddrch1_ndqs0 | DDR3 and DDR3L channel 1 negative data strobe 0 | IO | B27 |
| ddrch1_ndqs1 | DDR3 and DDR3L channel 1 negative data strobe 1 | IO | A23 |
| ddrch1_ndqs2 | DDR3 and DDR3L channel 1 negative data strobe 2 | IO | D32 |
| ddrch1_ndqs3 | DDR3 and DDR3L channel 1 negative data strobe 3 | IO | B4 |
| ddr3ch1_a0 | DDR3 and DDR3L row, column address bit 0 | O | A7 |
| ddr3ch1_a1 | DDR3 and DDR3L row, column address bit 1 | O | B7 |
| ddr3ch1_a2 | DDR3 and DDR3L row, column address bit 2 | O | C7 |
| ddr3ch1_a3 | DDR3 and DDR3L row, column address bit 3 | O | B8 |
| ddr3ch1_a4 | DDR3 and DDR3L row, column address bit 4 | O | C8 |
| ddr3ch1_a5 | DDR3 and DDR3L row, column address bit 5 | O | B9 |
| ddr3ch1_a6 | DDR3 and DDR3L row, column address bit 6 | O | C10 |
| ddr3ch1_a7 | DDR3 and DDR3L row, column address bit 7 | O | B12 |
| ddr3ch1_a8 | DDR3 and DDR3L row, column address bit 8 | O | C12 |
| ddr3ch1_a9 | DDR3 and DDR3L row, column address bit 9 | O | A13 |
| ddr3ch1_a10_ap | DDR3 and DDR3L row, column address bit 10 or DDR3 auto precharge sampling | O | B13 |
| ddr3ch1_a11 | DDR3 and DDR3L row, column address bit 11 | O | C13 |
| ddr3ch1_a12_nbc | DDR3 and DDR3L row, column address bit 12 or DDR3 bust chop on-the-fly sampling | O | B14 |
| ddr3ch1_a13 | DDR3 and DDR3L row, column address bit 13 | O | C14 |
| ddr3ch1_a14 | DDR3 and DDR3L row, column address bit 14 | O | A15 |
| ddr3ch1_a15 | DDR3 and DDR3L row, column address bit 15 | O | B15 |
| ddr3ch1_cka | DDR3 and DDR3L differential clock, set A | O | C11 |
| ddr3ch1_ckb | DDR3 and DDR3L differential clock, set B | O | C18 |
| ddr3ch1_cke0 | DDR3 and DDR3L clock enable for rank 0 | O | C9 |
| ddr3ch1_cke1 | DDR3 and DDR3L clock enable for rank 1 | O | A17 |
| ddr3ch1_ncka | DDR3 and DDR3L differential negative clock, set A | O | B11 |
| ddr3ch1_nckb | DDR3 and DDR3L differential negative clock, set B | O | B18 |
| ddr3ch1_ncs0 | DDR3 and DDR3L rank select 0 | O | B10 |
| ddr3ch1_ncs1 | DDR3 and DDR3L rank select 1 | O | B17 |
| ddr3ch1_ba0 | DDR3 and DDR3L bank select bit 0 | O | C15 |
| ddr3ch1_ba1 | DDR3 and DDR3L bank select bit 1 | O | B16 |
| ddr3ch1_ba2 | DDR3 and DDR3L bank select bit 2 | O | C16 |
| ddr3ch1_ncas | DDR3 and DDR3L command | O | C17 |
| ddr3ch1_nras | DDR3 and DDR3L command | O | B19 |
| ddr3ch1_nreset | DDR3 and DDR3L command | O | C19 |
| ddr3ch1_nwe | DDR3 and DDR3L asynchronous reset | O | B20 |
| ddr3ch1_odt0 | DDR3 and DDR3L on-die termination for rank 0 | O | C20 |
| ddr3ch1_odt1 | DDR3 and DDR3L on-die termination for rank 1 | O | B21 |
| DDR3 and DDR3L Channel 2 | | | |
| ddrch2_dm0 | DDR3 and DDR3L channel 2 data mask 0 | IO | J1 |
| ddrch2_dm1 | DDR3 and DDR3L channel 2 data mask 1 | IO | AJ3 |
| ddrch2_dm2 | DDR3 and DDR3L channel 2 data mask 2 | IO | G1 |
| ddrch2_dm3 | DDR3 and DDR3L channel 2 data mask 3 | IO | AL4 |
| ddrch2_dq0 | DDR3 and DDR3L channel 2 data bit 0 | IO | K3 |
| ddrch2_dq1 | DDR3 and DDR3L channel 2 data bit 1 | IO | H2 |
| ddrch2_dq2 | DDR3 and DDR3L channel 2 data bit 2 | IO | H3 |
| ddrch2_dq3 | DDR3 and DDR3L channel 2 data bit 3 | IO | J3 |

Table 3-4. DDR3 and DDR3L Signal Descriptions (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|---|----------|-----------------|
| ddrch2_dq4 | DDR3 and DDR3L channel 2 data bit 4 | IO | J2 |
| ddrch2_dq5 | DDR3 and DDR3L channel 2 data bit 5 | IO | M3 |
| ddrch2_dq6 | DDR3 and DDR3L channel 2 data bit 6 | IO | L2 |
| ddrch2_dq7 | DDR3 and DDR3L channel 2 data bit 7 | IO | L1 |
| ddrch2_dq8 | DDR3 and DDR3L channel 2 data bit 8 | IO | AK3 |
| ddrch2_dq9 | DDR3 and DDR3L channel 2 data bit 9 | IO | AG1 |
| ddrch2_dq10 | DDR3 and DDR3L channel 2 data bit 10 | IO | AH3 |
| ddrch2_dq11 | DDR3 and DDR3L channel 2 data bit 11 | IO | AJ2 |
| ddrch2_dq12 | DDR3 and DDR3L channel 2 data bit 12 | IO | AH2 |
| ddrch2_dq13 | DDR3 and DDR3L channel 2 data bit 13 | IO | AL1 |
| ddrch2_dq14 | DDR3 and DDR3L channel 2 data bit 14 | IO | AL3 |
| ddrch2_dq15 | DDR3 and DDR3L channel 2 data bit 15 | IO | AK4 |
| ddrch2_dq16 | DDR3 and DDR3L channel 2 data bit 16 | IO | G3 |
| ddrch2_dq17 | DDR3 and DDR3L channel 2 data bit 17 | IO | D3 |
| ddrch2_dq18 | DDR3 and DDR3L channel 2 data bit 18 | IO | C2 |
| ddrch2_dq19 | DDR3 and DDR3L channel 2 data bit 19 | IO | C1 |
| ddrch2_dq20 | DDR3 and DDR3L channel 2 data bit 20 | IO | D2 |
| ddrch2_dq21 | DDR3 and DDR3L channel 2 data bit 21 | IO | F2 |
| ddrch2_dq22 | DDR3 and DDR3L channel 2 data bit 22 | IO | G2 |
| ddrch2_dq23 | DDR3 and DDR3L channel 2 data bit 23 | IO | F3 |
| ddrch2_dq24 | DDR3 and DDR3L channel 2 data bit 24 | IO | AM3 |
| ddrch2_dq25 | DDR3 and DDR3L channel 2 data bit 25 | IO | AL5 |
| ddrch2_dq26 | DDR3 and DDR3L channel 2 data bit 26 | IO | AM4 |
| ddrch2_dq27 | DDR3 and DDR3L channel 2 data bit 27 | IO | AN3 |
| ddrch2_dq28 | DDR3 and DDR3L channel 2 data bit 28 | IO | AL7 |
| ddrch2_dq29 | DDR3 and DDR3L channel 2 data bit 29 | IO | AL6 |
| ddrch2_dq30 | DDR3 and DDR3L channel 2 data bit 30 | IO | AM7 |
| ddrch2_dq31 | DDR3 and DDR3L channel 2 data bit 31 | IO | AM6 |
| ddrch2_dqs0 | DDR3 and DDR3L channel 2 data strobe 0 | IO | K2 |
| ddrch2_dqs1 | DDR3 and DDR3L channel 2 data strobe 1 | IO | AK2 |
| ddrch2_dqs2 | DDR3 and DDR3L channel 2 data strobe 2 | IO | E2 |
| ddrch2_dqs3 | DDR3 and DDR3L channel 2 data strobe 3 | IO | AM5 |
| ddrch2_ndqs0 | DDR3 and DDR3L channel 2 negative data strobe 0 | IO | L3 |
| ddrch2_ndqs1 | DDR3 and DDR3L channel 2 negative data strobe 1 | IO | AL2 |
| ddrch2_ndqs2 | DDR3 and DDR3L channel 2 negative data strobe 2 | IO | E3 |
| ddrch2_ndqs3 | DDR3 and DDR3L channel 2 negative data strobe 3 | IO | AN5 |
| ddr3ch2_a0 | DDR3 and DDR3L row, column address bit 0 | O | AG2 |
| ddr3ch2_a1 | DDR3 and DDR3L row, column address bit 1 | O | AG3 |
| ddr3ch2_a2 | DDR3 and DDR3L row, column address bit 2 | O | AF2 |
| ddr3ch2_a3 | DDR3 and DDR3L row, column address bit 3 | O | AF3 |
| ddr3ch2_a4 | DDR3 and DDR3L row, column address bit 4 | O | AE2 |
| ddr3ch2_a5 | DDR3 and DDR3L row, column address bit 5 | O | AE3 |
| ddr3ch2_a6 | DDR3 and DDR3L row, column address bit 6 | O | AC3 |
| ddr3ch2_a7 | DDR3 and DDR3L row, column address bit 7 | O | AB2 |
| ddr3ch2_a8 | DDR3 and DDR3L row, column address bit 8 | O | AB3 |
| ddr3ch2_a9 | DDR3 and DDR3L row, column address bit 9 | O | AA2 |
| ddr3ch2_a10_ap | DDR3 and DDR3L row, column address bit 10 or DDR3 auto precharge sampling | O | AA3 |

Table 3-4. DDR3 and DDR3L Signal Descriptions (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|---|----------|-----------------|
| ddr3ch2_a11 | DDR3 and DDR3L row, column address bit 11 | O | Y2 |
| ddr3ch2_a12_nbc | DDR3 and DDR3L row, column address bit 12 or DDR3 bust chop on-the-fly sampling | O | Y3 |
| ddr3ch2_a13 | DDR3 and DDR3L row, column address bit 13 | O | W1 |
| ddr3ch2_a14 | DDR3 and DDR3L row, column address bit 14 | O | W2 |
| ddr3ch2_a15 | DDR3 and DDR3L row, column address bit 15 | O | W3 |
| ddr3ch2_cka | DDR3 and DDR3L differential clock, set A | O | AC2 |
| ddr3ch2_ckb | DDR3 and DDR3L differential clock, set B | O | R2 |
| ddr3ch2_cke0 | DDR3 and DDR3L clock enable for rank 0 | O | AD2 |
| ddr3ch2_cke1 | DDR3 and DDR3L clock enable for rank 1 | O | U3 |
| ddr3ch2_ncka | DDR3 and DDR3L differential negative clock, set A | O | AC1 |
| ddr3ch2_nckb | DDR3 and DDR3L differential negative clock, set B | O | R1 |
| ddr3ch2_ncs0 | DDR3 and DDR3L rank select 0 | O | AD3 |
| ddr3ch2_ncs1 | DDR3 and DDR3L rank select 1 | O | T2 |
| ddr3ch2_ba0 | DDR3 and DDR3L bank select bit 0 | O | V2 |
| ddr3ch2_ba1 | DDR3 and DDR3L bank select bit 1 | O | V3 |
| ddr3ch2_ba2 | DDR3 and DDR3L bank select bit 2 | O | U2 |
| ddr3ch2_ncas | DDR3 and DDR3L command | O | T3 |
| ddr3ch2_nras | DDR3 and DDR3L command | O | R3 |
| ddr3ch2_nreset | DDR3 and DDR3L command | O | P2 |
| ddr3ch2_nwe | DDR3 and DDR3L asynchronous reset | O | P3 |
| ddr3ch2_odt0 | DDR3 and DDR3L on-die termination for rank 0 | O | N2 |
| ddr3ch2_odt1 | DDR3 and DDR3L on-die termination for rank 1 | O | M2 |

3.4.2 Camera Interfaces

NOTE

For more information, see the Imaging Subsystem / ISS Interfaces section of the Device TRM.

3.4.2.1 Camera Control

Table 3-5. CAM Control Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|--------------------|----------|-----------------|
| cam_shutter | Mechanical shutter | O | AE6 / AF6 |
| cam_strobe | Flash trigger | O | AE5 |
| cam_globalreset | Sensor reset | IO | AF6 |

3.4.2.2 CSI-2 MIPI D-PHY

Table 3-6. CSI-2 MIPI D-PHY Signal Descriptions

| PIN NAME [5] | SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|---------------------------------|-----------------|---|----------|-----------------|
| Main Camera—CSI-2 Port A | | | | |
| csiporta_lane0x | CSI-2_lane0x | CSI-2 (Port A) camera lane 0 differential x | IDS | U6 |
| csiporta_lane0y | CSI-2_lane0y | CSI-2 (Port A) camera lane 0 differential y | IDS | U5 |
| csiporta_lane1x | CSI-2_lane1x | CSI-2 (Port A) camera lane 1 differential x | IDS | P6 |
| csiporta_lane1y | CSI-2_lane1y | CSI-2 (Port A) camera lane 1 differential y | IDS | P5 |

Table 3-6. CSI-2 MIPI D-PHY Signal Descriptions (continued)

| PIN NAME [5] | SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--------------------------------------|-----------------|---|----------|-----------------|
| csiporta_lane2x | CSI-2_lane2x | CSI-2 (Port A) camera lane 2 differential x | IDS | P7 |
| csiporta_lane2y | CSI-2_lane2y | CSI-2 (Port A) camera lane 2 differential y | IDS | P8 |
| csiporta_lane3x | CSI-2_lane3x | CSI-2 (Port A) camera lane 3 differential x | IDS | N5 |
| csiporta_lane3y | CSI-2_lane3y | CSI-2 (Port A) camera lane 3 differential y | IDS | N6 |
| csiporta_lane4x | CSI-2_lane4x | CSI-2 (Port A) camera lane 4 differential x | IDS | N7 |
| csiporta_lane4y | CSI-2_lane4y | CSI-2 (Port A) camera lane 4 differential y | IDS | N8 |
| Auxiliary Camera—CSI-2 Port B | | | | |
| csiportb_lane0x | CSI-2_lane0x | CSI-2 (Port B) camera lane 0 differential x | IDS | Y6 |
| csiportb_lane0y | CSI-2_lane0y | CSI-2 (Port B) camera lane 0 differential y | IDS | Y5 |
| csiportb_lane1x | CSI-2_lane1x | CSI-2 (Port B) camera lane 1 differential x | IDS | Y8 |
| csiportb_lane1y | CSI-2_lane1y | CSI-2 (Port B) camera lane 1 differential y | IDS | Y7 |
| csiportb_lane2x | CSI-2_lane2x | CSI-2 (Port B) camera lane 2 differential x | IDS | AA6 |
| csiportb_lane2y | CSI-2_lane2y | CSI-2 (Port B) camera lane 2 differential y | IDS | AA5 |
| Second Camera—CSI-2 Port C | | | | |
| csiportc_lane0x | CSI-2_lane0x | CSI-2 (Port C) camera lane 1 differential x | IDS | J7 |
| csiportc_lane0y | CSI-2_lane0y | CSI-2 (Port C) camera lane 1 differential y | IDS | J6 |
| csiportc_lane1x | CSI-2_lane1x | CSI-2 (Port C) camera lane 0 differential x | IDS | K5 |
| csiportc_lane1y | CSI-2_lane1y | CSI-2 (Port C) camera lane 0 differential y | IDS | K6 |

3.4.2.3 CCP2 PHY**Table 3-7. CCP2 PHY Signal Descriptions**

| PIN NAME [5] | SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--------------------------------------|-----------------|---|----------|-----------------|
| Auxiliary Camera—CCPV2 Port B | | | | |
| csiportb_lane0x | ccpv2_lane0x | CCPV2 (Port B) camera lane 0 differential x | IDS | Y6 |
| csiportb_lane0y | ccpv2_lane0y | CCPV2 (Port B) camera lane 0 differential y | IDS | Y5 |
| csiportb_lane1x | ccpv2_lane1x | CCPV2 (Port B) camera lane 1 differential x | IDS | Y8 |
| csiportb_lane1y | ccpv2_lane1y | CCPV2 (Port B) camera lane 1 differential y | IDS | Y7 |
| csiportb_lane2x | ccpv2_lane2x | CCPV2 (Port B) camera lane 2 differential x | IDS | AA6 |
| csiportb_lane2y | ccpv2_lane2y | CCPV2 (Port B) camera lane 2 differential y | IDS | AA5 |
| Second Camera—CCPV2 Port C | | | | |
| csiportc_lane1x | ccpv2_lane1x | CCPV2 (Port C) camera lane 0 differential x | IDS | J7 |
| csiportc_lane1y | ccpv2_lane1y | CCPV2 (Port C) camera lane 0 differential y | IDS | J6 |
| csiportc_lane0x | ccpv2_lane0x | CCPV2 (Port C) camera lane 1 differential x | IDS | K5 |
| csiportc_lane0y | ccpv2_lane0y | CCPV2 (Port C) camera lane 1 differential y | IDS | K6 |

3.4.2.4 CPI**Table 3-8. CPI Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|--|----------|-----------------|
| cp_i_pclk | CPI pixel clock | I | U6 |
| cp_i_hsync | CPI horizontal synchronization: line trigger | IO | AG5 |
| cp_i_vsync | CPI vertical synchronization: frame trigger | IO | AF5 |
| cp_i_hsyncin | CPI input-only version of cp_i_hsyncnck | I | AA5 |
| cp_i_vsyncin | CPI input-only version of cp_i_vsyncnck | I | AA6 |
| cp_i_data0 | CPI data bit 0 | I | P5 |
| cp_i_data1 | CPI data bit 1 | I | P6 |

Table 3-8. CPI Signal Descriptions (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|--|----------|-----------------|
| cpi_data2 | CPI data bit 2 | I | P8 |
| cpi_data3 | CPI data bit 3 | I | P7 |
| cpi_data4 | CPI data bit 4 | I | N5 |
| cpi_data5 | CPI data bit 5 | I | N6 |
| cpi_data6 | CPI data bit 6 | I | N7 |
| cpi_data7 | CPI data bit 7 | I | N8 |
| cpi_data8 | CPI data bit 8 | I | J6 |
| cpi_data9 | CPI data bit 9 | I | J7 |
| cpi_data10 | CPI data bit 10 | I | K6 |
| cpi_data11 | CPI data bit 11 | I | K5 |
| cpi_data12 | CPI data bit 12 | I | Y6 / AE7 |
| cpi_data13 | CPI data bit 13 | I | Y5 / AD5 |
| cpi_data14 | CPI data bit 14 | I | Y7 / AD6 |
| cpi_data15 | CPI data bit 15 | I | Y8 / AD7 |
| cpi_wen | CPI external write enable | I | U5 |
| cpi_fid | CPI field identification for interlaced sensors (I mode) | I | AF6 |

3.4.3 Display

NOTE

For more information, see the Display Subsystem / Display Subsystem Overview / DSS Environment section of the Device TRM.

3.4.3.1 DSI-1 MIPI D-PHY

Table 3-9. DSI-1 MIPI D-PHY Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-------------------|---|----------|-----------------|
| DSI Port A | | | |
| dsiporta_lane0x | DSI (Port A) lane 0 differential positive or negative | ODS | AD31 |
| dsiporta_lane0y | DSI (Port A) lane 0 differential positive or negative | ODS | AD32 |
| dsiporta_lane1x | DSI (Port A) lane 1 differential positive or negative | ODS | AC31 |
| dsiporta_lane1y | DSI (Port A) lane 1 differential positive or negative | ODS | AC32 |
| dsiporta_lane2x | DSI (Port A) lane 2 differential positive or negative | ODS | AB32 |
| dsiporta_lane2y | DSI (Port A) lane 2 differential positive or negative | ODS | AB31 |
| dsiporta_lane3x | DSI (Port A) lane 3 differential positive or negative | ODS | AA32 |
| dsiporta_lane3y | DSI (Port A) lane 3 differential positive or negative | ODS | AA31 |
| dsiporta_lane4x | DSI (Port A) lane 4 differential positive or negative | ODS | Y32 |
| dsiporta_lane4y | DSI (Port A) lane 4 differential positive or negative | ODS | Y31 |
| dsiporta_te0 | DSI (Port A) tearing effect control input | I | W33 |
| DSI Port C | | | |
| dsiportc_lane0x | DSI (Port C) lane 0 differential positive or negative | ODS | AJ31 |
| dsiportc_lane0y | DSI (Port C) lane 0 differential positive or negative | ODS | AJ32 |
| dsiportc_lane1x | DSI (Port C) lane 1 differential positive or negative | ODS | AH32 |
| dsiportc_lane1y | DSI (Port C) lane 1 differential positive or negative | ODS | AH31 |
| dsiportc_lane2x | DSI (Port C) lane 2 differential positive or negative | ODS | AG32 |
| dsiportc_lane2y | DSI (Port C) lane 2 differential positive or negative | ODS | AG31 |
| dsiportc_lane3x | DSI (Port C) lane 3 differential positive or negative | ODS | AF32 |
| dsiportc_lane3y | DSI (Port C) lane 3 differential positive or negative | ODS | AF31 |
| dsiportc_lane4x | DSI (Port A) lane 4 differential positive or negative | ODS | AE32 |
| dsiportc_lane4y | DSI (Port A) lane 4 differential positive or negative | ODS | AE31 |
| dsiportc_te0 | DSI (Port C) tearing effect control input | I | AK30 |

3.4.3.2 HDMI PHY

Table 3-10. HDMI PHY Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|---|----------|-----------------|
| hdmi_cec | HDMI consumer electronic control | IOD | AN23 |
| hdmi_hpd | HDMI display hot plug detect | I | AM23 |
| hdmi_ddc_scl | HDMI display data channel clock | IOD | AM22 |
| hdmi_ddc_sda | HDMI display data channel data | IOD | AL23 |
| hdmi_clkx | HDMI clock differential positive or negative | ODS | AL24 |
| hdmi_clky | HDMI clock differential positive or negative | ODS | AM24 |
| hdmi_data0x | HDMI data 0 differential positive or negative | ODS | AL25 |
| hdmi_data0y | HDMI data 0 differential positive or negative | ODS | AM25 |
| hdmi_data1x | HDMI data 1 differential positive or negative | ODS | AL26 |
| hdmi_data1y | HDMI data 1 differential positive or negative | ODS | AM26 |
| hdmi_data2x | HDMI data 2 differential positive or negative | ODS | AL27 |
| hdmi_data2y | HDMI data 2 differential positive or negative | ODS | AM27 |

3.4.3.3 RFBI

Table 3-11. RFBI Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|---|----------|-----------------|
| rfbi_data0 | RFBI data bit 0 | IO | AL17 |
| rfbi_data1 | RFBI data bit 1 | IO | AM17 |
| rfbi_data2 | RFBI data bit 2 | IO | AN17 |
| rfbi_data3 | RFBI data bit 3 | IO | AL16 |
| rfbi_data4 | RFBI data bit 4 | IO | AM16 |
| rfbi_data5 | RFBI data bit 5 | IO | AL15 |
| rfbi_data6 | RFBI data bit 6 | IO | AM15 |
| rfbi_data7 | RFBI data bit 7 | IO | AN15 |
| rfbi_data8 | RFBI data bit 8 | IO | AL14 |
| rfbi_data9 | RFBI data bit 9 | IO | AM14 |
| rfbi_data10 | RFBI data bit 10 | IO | AM12 |
| rfbi_data11 | RFBI data bit 11 | IO | AL11 |
| rfbi_data12 | RFBI data bit 12 | IO | AM11 |
| rfbi_data13 | RFBI data bit 13 | IO | AN11 |
| rfbi_data14 | RFBI data bit 14 | IO | AL10 |
| rfbi_data15 | RFBI data bit 15 | IO | AM10 |
| rfbi_a0 | RFBI data / control selection | O | AM18 |
| rfbi_we | RFBI write enable | O | AL12 |
| rfbi_re | RFBI read enable | O | AL18 |
| rfbi_cs0 | RFBI chip select | O | AL13 |
| rfbi_te_vsync0 | RFBI vertical synchronization / tearing effect control signal | I | AM13 |
| rfbi_hsync0 | RFBI horizontal synchronization / tearing effect control signal | I | AN13 |

3.4.3.4 DISPC

Table 3-12. DISPC Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|--------------------------------------|----------|-----------------|
| dispc_data0 | DISPC data to LCD2 panel—data bit 0 | O | AL17 |
| dispc_data1 | DISPC data to LCD2 panel—data bit 1 | O | AM17 |
| dispc_data2 | DISPC data to LCD2 panel—data bit 2 | O | AN17 |
| dispc_data3 | DISPC data to LCD2 panel—data bit 3 | O | AL16 |
| dispc_data4 | DISPC data to LCD2 panel—data bit 4 | O | AM16 |
| dispc_data5 | DISPC data to LCD2 panel—data bit 5 | O | AL15 |
| dispc_data6 | DISPC data to LCD2 panel—data bit 6 | O | AM15 |
| dispc_data7 | DISPC data to LCD2 panel—data bit 7 | O | AN15 |
| dispc_data8 | DISPC data to LCD2 panel—data bit 8 | O | AL14 |
| dispc_data9 | DISPC data to LCD2 panel—data bit 9 | O | AM14 |
| dispc_data10 | DISPC data to LCD2 panel—data bit 10 | O | AM12 |
| dispc_data11 | DISPC data to LCD2 panel—data bit 11 | O | AL11 |
| dispc_data12 | DISPC data to LCD2 panel—data bit 12 | O | AM11 |
| dispc_data13 | DISPC data to LCD2 panel—data bit 13 | O | AN11 |
| dispc_data14 | DISPC data to LCD2 panel—data bit 14 | O | AL10 |
| dispc_data15 | DISPC data to LCD2 panel—data bit 15 | O | AM10 |
| dispc_data16 | DISPC data to LCD2 panel—data bit 16 | O | AN9 |
| dispc_data17 | DISPC data to LCD2 panel—data bit 17 | O | AM9 |

Table 3-12. DISPC Signal Descriptions (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|---|----------|-----------------|
| dispc_data18 | DISPC data to LCD2 panel—data bit 18 | O | AL9 |
| dispc_data19 | DISPC data to LCD2 panel—data bit 19 | O | AM8 |
| dispc_data20 | DISPC data to LCD2 panel—data bit 20 | O | AL8 |
| dispc_data21 | DISPC data to LCD2 panel—data bit 21 | O | AN7 |
| dispc_data22 | DISPC data to LCD2 panel—data bit 22 | O | AL14 |
| dispc_data23 | DISPC data to LCD2 panel—data bit 23 | O | AM14 |
| dispc_hsync | DISPC horizontal synchronization from dispc to LCD2 | O | AL13 |
| dispc_vsync | DISPC vertical synchronization from dispc to LCD2 | O | AL12 |
| dispc_de | DISPC ac bias output enable or data enable to LCD2 | O | AM18 |
| dispc_pclk | DISPC LCD pixel clock to LCD2 | O | AL18 |
| dispc_fid | DISPC field ID to LCD2 | O | AF20 |

3.4.4 Serial and Parallel Communication Interfaces

3.4.4.1 HDQ / 1-Wire

NOTE

For more information, see the Serial Communication Interface / HDQ/1-Wire section of the Device TRM.

Table 3-13. HDQ / 1-Wire Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|-----------------|----------|-----------------|
| hdq_sio | HDQ 1-wire | IOD | AJ24 |

3.4.4.2 I²C

NOTE

For more information, see the Serial Communication Interface / Multimaster High-Speed I²C Controller / HS I²C Environment / HS I²C in I²C Mode section of the Device TRM.

NOTE

For more information on SmartReflex™ AVS, see:

- The Power, Reset and Clock Management / Device Power Management Introduction / Device Power-Management Architecture Building Blocks / Voltage Management / AVS Overview section
 - The Power, Reset and Clock Management / PRCM Subsystem Environment / External Power Control Signals section of the Device TRM.
-

Table 3-14. I²C Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|---|---------------------------------|----------|-----------------|
| Inter-Integrated Circuit Interface (I2C1)—Platform | | | |
| i2c1_pmic_scl | I2C1 master platform clock | IOD | P29 |
| i2c1_pmic_sda | I2C1 master platform data | IOD | P28 |
| Inter-Integrated Circuit Interface (I2C2)—Generic | | | |
| i2c2_scl | I2C2 OMAP master or slave clock | IOD | AL33 |

Table 3-14. I²C Signal Descriptions (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|---|---------------------------------|----------|-----------------|
| i2c2_sda | I2C2 data | IOD | AM32 |
| Inter-Integrated Circuit Interface (I2C3)—Generic | | | |
| i2c3_scl | I2C3 OMAP master clock | IOD | AJ5 |
| i2c3_sda | I2C3 data | IOD | AH4 |
| Inter-Integrated Circuit Interface (I2C4)—Generic | | | |
| i2c4_scl | I2C4 OMAP master clock | IOD | AJ21 |
| i2c4_sda | I2C4 data | IOD | AJ20 |
| Inter-Integrated Circuit Interface (I2C5)—Generic | | | |
| i2c5_scl | I2C5 OMAP master or slave clock | IOD | AL28 |
| i2c5_sda | I2C5 data | IOD | AM29 |
| Inter-Integrated Circuit Interface (SmartReflex™ AVS)—PMIC | | | |
| sr_pmic_scl | SmartReflex™ AVS clock | IOD | R32 |
| sr_pmic_sda | SmartReflex™ AVS data | IOD | R31 |

3.4.4.3 McBSP

NOTE

For more information, see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) section of the Device TRM.

Table 3-15. McBSP Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--|---|----------|-----------------|
| abe_clks | ABE synchronization input clock | I | W32 |
| Audio Back-end Multichannel Buffered Serial Port (ABE McBSP1) | | | |
| abemcbasp1_dr | ABE McBSP1 received serial data | I | AG29 |
| abemcbasp1_dx | ABE McBSP1 transmitted serial data | O | AD28 |
| abemcbasp1_fsx | ABE McBSP1 combined frame synchronization | IO | AD29 |
| abemcbasp1_clkx | ABE McBSP1 combined serial clock | IO | AF29 |
| Audio Back-end Multichannel Buffered Serial Port (ABE McBSP2) | | | |
| abemcbasp2_dr | ABE McBSP2 received serial data | I | AD26 |
| abemcbasp2_dx | ABE McBSP2 transmitted serial data | O | AD27 |
| abemcbasp2_fsx | ABE McBSP2 combined frame synchronization | IO | AA26 |
| abemcbasp2_clkx | ABE McBSP2 combined serial clock | IO | AA27 |
| Audio Back-end Multichannel Buffered Serial Port (ABE McBSP3) | | | |
| abemcbasp3_dr | ABE McBSP3 received serial data | I | AE28 / AA28 |
| abemcbasp3_dx | ABE McBSP3 transmitted serial data | O | AE29 / AA29 |
| abemcbasp3_fsx | ABE McBSP3 combined frame synchronization | IO | AF28 / Y28 |
| abemcbasp3_clkx | ABE McBSP3 combined serial clock | IO | AE27 / Y29 |

3.4.4.4 McPDM

NOTE

For more information, see the Serial Communication Interface / Multichannel PDM Controller section of the Device TRM.

Table 3-16. McPDM Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--|---|----------|-----------------|
| abe_clks | ABE synchronization input clock | I | W32 |
| Audio Back-end Multichannel PDM | | | |
| abemcpdm_ul_data | ABE PDM data stream from PMIC to Device | I | AA28 |
| abemcpdm_dl_data | ABE PDM data stream from Device to PMIC | O | AA29 |
| abemcpdm_frame | ABE PDM frame synchronization | IO | Y29 |
| abemcpdm_lb_clk | ABE PDM loop back clock | O | Y28 |

3.4.4.5 DMIC**NOTE**

For more information, see the Serial Communication Interface / Digital Microphone Module section of the Device TRM.

Table 3-17. DMIC Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|---|---------------------------------------|----------|-----------------|
| abe_clks | ABE synchronization input clock | I | W32 |
| Audio Back-end Digital Microphone Module | | | |
| abedmic_clk1 | ABE digital microphone clock output 1 | O | AE27 |
| abedmic_din1 | ABE digital microphone data input 1 | I | AF28 |
| abedmic_clk2 | ABE digital microphone clock output 2 | O | AD29 |
| abedmic_din2 | ABE digital microphone data input 2 | I | AE29 |
| abedmic_clk3 | ABE digital microphone clock output 3 | O | AD28 |
| abedmic_din3 | ABE digital microphone data input 3 | I | AE28 |

3.4.4.6 McASP**NOTE**

For more information, see the Serial Communication Interface / Multichannel Audio Serial Port section of the Device TRM.

Table 3-18. McASP Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--|--|----------|-------------------|
| abe_clks | ABE synchronization input clock | I | W32 |
| Audio Back-end Multichannel Audio Serial Port | | | |
| abemcasp_axr | ABE McASP serial data IO | IO | AD26 / W32 / AE29 |
| abemcasp_axr1 | ABE McASP serial data 1 IO | IO | Y29 |
| abemcasp_axr2 | ABE McASP serial data 2 IO | IO | AA29 |
| abemcasp_axr3 | ABE McASP serial data 3 IO | IO | AA28 |
| abemcasp_aclkx | ABE McASP clock transmit | IO | AD28 |
| abemcasp_afsx | ABE McASP frame synchronization transmit | IO | AA26 |
| abemcasp_afsr | ABE McASP frame synchronization receive | IO | AF29 |
| abemcasp_ahclkx | ABE McASP high frequency clock output | IO | AA27 |
| abemcasp_aclkr | ABE McASP low frequency clock input | IO | AG29 |
| abemcasp_amutein | ABE McASP auto mute input | I | AD29 |
| abemcasp_amuteout | ABE McASP auto mute output | O | AD27 |

3.4.4.7 HSI

NOTE

For more information, see the Serial Communication Interface / MIPI-HSI section of the Device TRM.

NOTE

The HSI1 interface is not available in the device. For more information, see the Device TRM.

Table 3-19. HSI2 Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|---|---|----------|-----------------|
| High-speed Synchronous Serial Interface (HSI2) | | | |
| hsi2_cawake | HSI2 cellular modem to APE wake signal | I | F17 |
| hsi2_acready | HSI2 APE to cellular modem ready signal | O | F20 |
| hsi2_cadata | HSI2 cellular modem to APE signal | I | F14 |
| hsi2_caflag | HSI2 cellular modem to APE flag signal | I | E14 |
| hsi2_acwake | HS2 APE to cellular modem wake signal | O | E20 |
| hsi2_caready | HSI2 cellular modem to APE ready signal | I | G20 |
| hsi2_acdata | HSI2 APE to cellular modem data signal | O | E17 |
| hsi2_acflag | HSI2 APE to cellular modem ready signal | O | G14 |

3.4.4.8 McSPI

NOTE

For more information, see the Serial Communication Interface / Multichannel Serial Port Interface (McSPI) section of the Device TRM.

Table 3-20. McSPI Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--|---|----------|-------------------|
| Multichannel Serial Port Interface (McSPI1) | | | |
| mcspi1_simo | McSPI1 data (slave input, master output, Z when not shifting) | IO | AL29 |
| mcspi1_somi | McSPI1 data (slave output, master input, Z when not shifting) | I | AL30 |
| mcspi1_clk | McSPI1 clock | IO | AM30 |
| mcspi1_cs0 | McSPI1 chip select 0 | O | AN31 |
| mcspi1_cs1 | McSPI1 chip select 1 | O | AM31 |
| mcspi1_cs2 | McSPI1 chip select 2 | O | NA ⁽¹⁾ |
| mcspi1_cs3 | McSPI1 chip select 3 | O | NA ⁽¹⁾ |
| Multichannel Serial Port Interface (McSPI2) | | | |
| mcspi2_simo | McSPI2 data (slave input, master output, Z when not shifting) | IO | AG20 |
| mcspi2_somi | McSPI2 data (slave output, master input, Z when not shifting) | I | AH20 |
| mcspi2_clk | McSPI2 clock | IO | AH17 |
| mcspi2_cs0 | McSPI2 chip select 0 | O | AF20 |
| mcspi2_cs1 | McSPI2 chip select 1 | O | AM10 |
| Multichannel Serial Port Interface (McSPI3) | | | |
| mcspi3_simo | McSPI3 data (slave input, master output, Z when not shifting) | IO | G13 |
| mcspi3_somi | McSPI3 data (slave output, master input, Z when not shifting) | IO | F13 |
| mcspi3_clk | McSPI3 clock | IO | E13 |
| mcspi3_cs0 | McSPI3 chip select 0 | IO | N9 |

Table 3-20. McSPI Signal Descriptions (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--|---|----------|-----------------|
| Multichannel Serial Port Interface (McSPI4) | | | |
| mcspi4_simo | McSPI4 data (slave input, master output, Z when not shifting) | IO | AJ26 |
| mcspi4_somi | McSPI4 data (slave output, master input, Z when not shifting) | IO | AH26 |
| mcspi4_clk | McSPI4 clock | IO | AH25 |
| mcspi4_cs0 | McSPI4 chip select 0 | IO | AK28 |

(1) NA in this table stands for not applicable for the device.

3.4.4.9 UART

NOTE

For more information, see the Serial Communication Interface / UART/IrDA/CIR section of the Device TRM.

NOTE

The UART4 and UART6 interfaces are not available in the device. For more information, see the Device TRM.

Table 3-21. UART1, UART2, UART3, and UART5 Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--|--|----------|--------------------|
| Universal Asynchronous Receiver/Transmitter (UART1) | | | |
| uart1_tx | UART1 transmit data | O | AE7 |
| uart1_rx | UART1 receive data | I | AD6 |
| uart1_cts | UART1 clear to send | I | AD5 |
| uart1_rts | UART1 request to send | O | AD7 |
| Universal Asynchronous Receiver/Transmitter (UART2) | | | |
| uart2_tx | UART2 transmit data | O | E13 |
| uart2_rx | UART2 receive data | I | G13 |
| uart2_cts | UART2 clear to send | I | N9 |
| uart2_rts | UART2 request to send | O | F13 |
| Universal Asynchronous Receiver/Transmitter (UART3) | | | |
| uart3_tx_irtx | UART3 transmit data output or infrared data output | O | AN17 / AG24 / AM19 |
| uart3_rx_irrx | UART3 receive data input or infrared data input | I | AM17 / AH24 / AL19 |
| uart3_cts_rctx | UART3 clear to send or remote control data output | IO | AJ25 |
| uart3_rts_irsds | UART3 request to send or infrared transceiver shutdown | O | AJ24 |
| Universal Asynchronous Receiver/Transmitter (UART5) | | | |
| uart5_tx | UART5 transmit data | O | AL31 |
| uart5_rx | UART5 receive data | I | AL32 |
| uart5_cts | UART5 clear to send | I | AK31 |
| uart5_rts | UART5 request to send | O | AK32 |

3.4.4.10 USB

NOTE

For more information, see:

- Serial Communication Interface / High-Speed Multiport USB Host Subsystem section, or
- Serial Communication Interface / High-Speed USB OTG Controller section, or
- Serial Communication Interface / Full-Speed USB Host Controller section, or
- Serial Communication Interface / Super-Speed USB OTG Subsystem section of the Device TRM.

NOTE

The following interfaces are not available in the device:

- USB (Port D0)—ULPI 8-bit
- USB (Port B1)—HSIC1
- USB (Port B2)—ULPI 8-bit
- USB (Port B2)—Full Speed / Low Speed

For more information, see the Device TRM.

Table 3-22. USB Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--|---|----------|-----------------|
| Universal Serial Bus (Port D0)—USB2PHY | | | |
| usbd0_hs_dp | USB2PHY (Port D0)—half-duplex positive lane | IODS | AL19 |
| usbd0_hs_dm | USB2PHY (Port D0)—half-duplex negative lane | IODS | AM19 |
| usbphy_ce | USB2PHY (Port D0)—charge enable | O | AN19 |
| Universal Serial Bus (Port D0)—USB3PHY | | | |
| usbd0_ss_tx | USB3PHY (Port D0)—transmitter positive lane | ODS | AL20 |
| usbd0_ss_ty | USB3PHY (Port D0)—transmitter negative lane | ODS | AM20 |
| usbd0_ss_rx | USB3PHY (Port D0)—receiver positive lane | IDS | AL21 |
| usbd0_ss_ry | USB3PHY (Port D0)—receiver negative lane | IDS | AM21 |
| Universal Serial Bus (Port B1)—ULPI 8-bit | | | |
| usbb1_ulpihy_clk | USB (Port B1)—ULPI functional clock | I | G20 |
| usbb1_ulpihy_stp | USB (Port B1)—ULPI stop | O | E20 |
| usbb1_ulpihy_dir | USB (Port B1)—ULPI bus direction | I | F17 |
| usbb1_ulpihy_nxt | USB (Port B1)—ULPI next | I | F20 |
| usbb1_ulpihy_data0 | USB (Port B1)—ULPI 8-bit data bus | IO | E14 |
| usbb1_ulpihy_data1 | USB (Port B1)—ULPI 8-bit data bus | IO | F14 |
| usbb1_ulpihy_data2 | USB (Port B1)—ULPI 8-bit data bus | IO | G14 |
| usbb1_ulpihy_data3 | USB (Port B1)—ULPI 8-bit data bus | IO | E17 |
| usbb1_ulpihy_data4 | USB (Port B1)—ULPI 8-bit data bus | IO | F13 |
| usbb1_ulpihy_data5 | USB (Port B1)—ULPI 8-bit data bus | IO | N9 |
| usbb1_ulpihy_data6 | USB (Port B1)—ULPI 8-bit data bus | IO | G13 |
| usbb1_ulpihy_data7 | USB (Port B1)—ULPI 8-bit data bus | IO | E13 |
| Universal Serial Bus (Port B2)—HSIC | | | |
| usbb2_hsic_data | USB (Port B2)—interchip data | IO | K29 |
| usbb2_hsic_strobe | USB (Port B2)—interchip strobe | IO | K28 |
| Universal Serial Bus (Port B3)—HSIC | | | |
| usbb3_hsic_data | USB (Port B3)—interchip data | IO | K27 |
| usbb3_hsic_strobe | USB (Port B3)—interchip strobe | IO | K26 |

3.4.4.11 SATA

NOTE

For more information, see the SATA section of the Device TRM.

Table 3-23. SATA Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|---|----------|-----------------|
| sata_tx | SATA differential positive or negative transmitter lane x | ODS | G9 |
| sata_ty | SATA differential positive or negative transmitter lane y | ODS | F9 |
| sata_rx | SATA differential positive or negative receiver lane x | IDS | E10 |
| sata_ry | SATA differential positive or negative receiver lane y | IDS | F10 |
| sata_actled | SATA channel activity indicator | O | AJ25 |

3.4.4.12 eMMC

NOTE

For more information, see the MMC / SD / SDIO section of the Device TRM.

Table 3-24. eMMC Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|-----------------|----------|-----------------|
| emmc_clk | eMMC clock | O | AJ10 |
| emmc_cmd | eMMC command | IO | AH10 |
| emmc_data0 | eMMC data bit 0 | IO | AG10 |
| emmc_data1 | eMMC data bit 1 | IO | AF10 |
| emmc_data2 | eMMC data bit 2 | IO | AH9 |
| emmc_data3 | eMMC data bit 3 | IO | AJ9 |
| emmc_data4 | eMMC data bit 4 | IO | AG9 |
| emmc_data5 | eMMC data bit 5 | IO | AJ8 |
| emmc_data6 | eMMC data bit 6 | IO | AH8 |
| emmc_data7 | eMMC data bit 7 | IO | AJ7 |

3.4.4.13 WLSdio3

Table 3-25. WLSdio Signal Descriptions⁽¹⁾

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|---|-------------------|----------|-----------------|
| Wireless LAN SDIO (OMAP to Wireless LAN) | | | |
| wlsdio_clk | WLSdio clock | O | AH25 |
| wlsdio_cmd | WLSdio command | IO | AG25 |
| wlsdio_data0 | WLSdio data bit 0 | IO | AJ26 |
| wlsdio_data1 | WLSdio data bit 1 | IO | AH26 |
| wlsdio_data2 | WLSdio data bit 2 | IO | AK28 |
| wlsdio_data3 | WLSdio data bit 3 | IO | AJ27 |

(1) This interface supports WLAN SDIO with inband interrupt.

3.4.4.14 SDIO4

Table 3-26. SDIO4 Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|---------------------|------------------|----------|-----------------|
| Generic SDIO | | | |
| sdio4_clk | SDIO4 clock | O | AG24 |
| sdio4_cmd | SDIO4 command | IO | AH24 |
| sdio4_data0 | SDIO4 data bit 0 | IO | AK31 |
| sdio4_data1 | SDIO4 data bit 1 | IO | AL32 |
| sdio4_data2 | SDIO4 data bit 2 | IO | AL31 |
| sdio4_data3 | SDIO4 data bit 3 | IO | AK32 |

NOTE

The SDIO5 interface is not available in the Device device. For more information, see the Device TRM.

3.4.5 Removable Cards

Table 3-27. SD Card Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|------------------|----------|-----------------|
| sdcard_clk | SD clock | O | F8 |
| sdcard_cmd | SD command | IO | E8 |
| sdcard_data0 | SD data bit 0 | IO | H6 |
| sdcard_data1 | SD data bit 1 | IO | H5 |
| sdcard_data2 | SD data bit 2 | IO | G5 |
| sdcard_data3 | SD data bit 3 | IO | E7 |
| sdcard_cd | SD card detect | I | AD5 |
| sdcard_wp | SD write protect | I | AD6 / AD7 |

3.4.6 Debug and Trace Interfaces

NOTE

For more information, see the On-Chip Debug Support / Debug Ports section of the Device TRM.

3.4.6.1 JTAG®

Table 3-28. JTAG Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|--|----------|-----------------|
| jtag_nrst | JTAG test reset | I | H5 / B32 |
| jtag_tck | JTAG test clock | I | E7 / C31 |
| jtag_tmselect | JTAG test mode select (I for JTAG) | IO | B31 / G5 |
| jtag_rtck | JTAG ARM @ clock emulation | O | F8 / B33 |
| jtag_tdi | JTAG test data In | I | H6 / A32 |
| jtag_tdo | JTAG test data out | O | E8 / A33 |
| jtag_sel | JTAG override HW control for JTAG on SD card interface | I | AM13 |

3.4.6.2 cJTAG

Table 3-29. cJTAG Signal Descriptions

| PIN NAME [5] | SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|------------------------------|-----------------|---------------------------------------|----------|-----------------|
| cJTAG Muxed with JTAG | | | | |
| jtag_tck | cjtag_tck | cJTAG test clock | I | E7 / C31 |
| jtag_tmisc | cjtag_tmisc | cJTAG test mode control and data scan | IO | B31 / G5 |

3.4.6.3 JTAG Expansion Port

Table 3-30. JTAG Expansion Port Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--|--|----------|-----------------|
| Inverted JTAG interface to chain a modem (or other IC) with the OMAP JTAG | | | |
| jtagtapext_nrst | Test reset for external modem or other IC | O | AL16 / AF20 |
| jtagtapext_tck | Test clock for external modem or other IC | O | AM16 / AH17 |
| jtagtapext_tmisc | Test mode select (0 for modem JTAG) for external modem or other IC | O | AL15 / AJ18 |
| jtagtapext_rtck | ARM clock emulation for external modem or other IC | O | AL17 / AJ20 |
| jtagtapext_tdi | Test data in for external modem or other IC | I | AN15 / AJ21 |
| jtagtapext_tdo | Test data out for external modem or other IC | O | AM15 / AH20 |

3.4.6.4 Debug Resource Manager (DRM)

NOTE

For more information, see the On-Chip Debug Support / Debug Ports section of the Device TRM.

Table 3-31 provides the DRM signal descriptions plus the debug modes available on the DRM signals.

Table 3-31. DRM Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] | DEBUG MODE | | |
|-----------------|-------------------------------|----------|-----------------|------------|-----------------|--------------------------|
| | | | | TRIGGER | TPIU PTM 16-BIT | TPIU STM 4-BIT |
| drm_emu19 | Debug resource manager bit 19 | O | AM10 / V32 | | atpiu_data15 | stm_data[3:0] or stm_clk |
| drm_emu18 | Debug resource manager bit 18 | O | AL10 / V31 | | atpiu_data14 | stm_data[3:0] or stm_clk |
| drm_emu17 | Debug resource manager bit 17 | O | AN11 / U33 | | atpiu_data13 | stm_data[3:0] or stm_clk |
| drm_emu16 | Debug resource manager bit 16 | O | AM11 / U32 | | atpiu_data12 | stm_data[3:0] or stm_clk |
| drm_emu15 | Debug resource manager bit 15 | O | AL11 / U31 | | atpiu_data11 | stm_data[3:0] or stm_clk |
| drm_emu14 | Debug resource manager bit 14 | O | AM12 | | atpiu_data10 | stm_data[3:0] or stm_clk |
| drm_emu13 | Debug resource manager bit 13 | O | AM14 | | atpiu_data9 | stm_data[3:0] or stm_clk |
| drm_emu12 | Debug resource manager bit 12 | O | AL14 | | atpiu_data8 | stm_data[3:0] or stm_clk |
| drm_emu11 | Debug resource manager bit 11 | O | AN15 | | atpiu_data7 | stm_data[3:0] or stm_clk |
| drm_emu10 | Debug resource manager bit 10 | O | AM15 | | atpiu_data6 | stm_data[3:0] or stm_clk |
| drm_emu9 | Debug resource manager bit 9 | O | AL15 | | atpiu_data5 | stm_data[3:0] or stm_clk |

Table 3-31. DRM Signal Descriptions (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] | DEBUG MODE | | |
|-----------------|------------------------------|----------|-----------------|------------------|-----------------|--------------------------|
| | | | | TRIGGER | TPIU PTM 16-BIT | TPIU STM 4-BIT |
| drm_emu8 | Debug resource manager bit 8 | O | AM16 | | atpiu_data4 | stm_data[3:0] or stm_clk |
| drm_emu7 | Debug resource manager bit 7 | O | AL16 | | atpiu_data3 | stm_data[3:0] or stm_clk |
| drm_emu6 | Debug resource manager bit 6 | O | AN17 / V32 | | atpiu_data2 | stm_data[3:0] or stm_clk |
| drm_emu5 | Debug resource manager bit 5 | O | AM17 / V31 | | atpiu_data1 | stm_data[3:0] or stm_clk |
| drm_emu4 | Debug resource manager bit 4 | O | AL17 / U33 | | atpiu_data0 | stm_data[3:0] or stm_clk |
| drm_emu3 | Debug resource manager bit 3 | O | AL13 / U32 | | atpiu_ctl | stm_data[3:0] or stm_clk |
| drm_emu2 | Debug resource manager bit 2 | O | AL12 / U31 | | atpiu_clk | stm_data[3:0] or stm_clk |
| drm_emu1 | Debug resource manager bit 1 | IO | K31 | trigger_channel1 | | stm_data[3:0] or stm_clk |
| drm_emu0 | Debug resource manager bit 0 | IO | K32 | trigger_channel0 | | stm_data[3:0] or stm_clk |

The DRM interface supports:

- PTM: Processor Trace Module, specific to MPU trace.
- STM: System Trace Module, for HW and SW system events.

STM via the DRM interface is always supported while MPU trace (PTM) is not always possible. This limitation is induced by the DRM: while any drm_emu signals can be configured as the STM clock or one of the data lanes, the drm_emu signals have a fixed PTM assignment.

The concurrent debug use cases are:

- UC1: Either uses trigger channel 2 pins plus the TPIU PTM 16-bit data.
- UC2: Either the TPIU PTM 16-bit data plus the TPIU STM 1-bit data.
- UC3: Either the trigger channel 2 pins plus TPIU PTM 8-bit data plus TPIU STM 4-bit data.
- UC4: Or uses the trigger channel 2 pins plus TPIU PTM 11-bit data plus TPIU STM 4-bit data.

An STM 4-bit data always-on interface is available via the DRM interface on the sys_boot pins in order to use debug function in OFF mode (especially for PRCM or audio backend debug).

Table 3-32. Always-On STM 4-Bit Debug Port Configuration

| DEBUG MODE STM 4-BIT | SIGNAL NAME (DEBUG PORT) [1] | PIN NAME [5] | TYPE [3] | BALL BOTTOM [4] |
|--------------------------|------------------------------|--------------|----------|-----------------|
| stm_data[3:0] or stm_clk | drm_emu15 | sys_boot0 | IO | U31 |
| stm_data[3:0] or stm_clk | drm_emu16 | sys_boot1 | IO | U32 |
| stm_data[3:0] or stm_clk | drm_emu17 | sys_boot2 | IO | U33 |
| stm_data[3:0] or stm_clk | drm_emu18 | sys_boot3 | IO | V31 |
| stm_data[3:0] or stm_clk | drm_emu19 | sys_boot4 | IO | V32 |

3.4.6.5 MIPI NiDnT (Narrow Interface for Debug and Test)

Typically, the device wide debug port is not available on a packaged end product phone due to connectivity and footprint constraints.

The Device provides a narrow debug interface on SD Card connector compliant to the MIPI NiDnT specification. The MIPI NiDnT functionality is supported with full software control.

Table 3-33 provides the NiDnT signal descriptions.

Table 3-33. NiDnT Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|---|-----------------|----------|-----------------|
| Narrow Interface for Debug and Trace | | | |
| n_clk | NiDnT debug bus | O | F8 |
| n_d0 | NiDnT debug bus | O | H6 |
| n_d1 | NiDnT debug bus | O | H5 |
| n_d2 | NiDnT debug bus | O | E8 / G5 |
| n_d3 | NiDnT debug bus | O | E7 |

The NiDnT standard supports several overlay modes by software. For more information, see the On-Chip Debug Support / Debug Interfaces / NiDnT section of the Device TRM.

3.4.6.6 Hardware Debug

NOTE

For more information, see the On-Chip Debug Support / Debug Ports section of the Device TRM.

Table 3-34. Hardware Debug Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--|-----------------------|----------|-------------------|
| Observability Hardware Debug Bus: Wakeup Domain | | | |
| hw_wkdbg0 | Hardware debug pin 0 | O | U31 |
| hw_wkdbg1 | Hardware debug pin 1 | O | U32 |
| hw_wkdbg2 | Hardware debug pin 2 | O | U33 |
| hw_wkdbg3 | Hardware debug pin 3 | O | V31 |
| hw_wkdbg4 | Hardware debug pin 4 | O | V32 |
| hw_wkdbg5 | Hardware debug pin 5 | O | P31 |
| hw_wkdbg6 | Hardware debug pin 6 | O | K32 |
| hw_wkdbg7 | Hardware debug pin 7 | O | K31 |
| hw_wkdbg8 | Hardware debug pin 8 | O | NA ⁽¹⁾ |
| hw_wkdbg9 | Hardware debug pin 9 | O | M31 |
| hw_wkdbg10 | Hardware debug pin 10 | O | NA ⁽¹⁾ |
| hw_wkdbg11 | Hardware debug pin 11 | O | NA ⁽¹⁾ |
| hw_wkdbg12 | Hardware debug pin 12 | O | NA ⁽¹⁾ |
| hw_wkdbg13 | Hardware debug pin 13 | O | N29 |
| hw_wkdbg14 | Hardware debug pin 14 | O | N28 |
| Observability Hardware Debug Bus: Core Domain | | | |
| hw_wkdbg15 | Hardware debug pin 15 | O | T31 |
| hw_dbg16 | Hardware debug pin 16 | O | J32 / F13 |
| hw_dbg17 | Hardware debug pin 17 | O | J33 / N9 |
| hw_dbg18 | Hardware debug pin 18 | O | H32 / G13 |
| hw_dbg19 | Hardware debug pin 19 | O | J31 / E31 |

Table 3-34. Hardware Debug Signal Descriptions (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|-----------------------|----------|-----------------|
| hw_dbg20 | Hardware debug pin 20 | O | G31 / AG20 |
| hw_dbg21 | Hardware debug pin 21 | O | H31 / AH20 |
| hw_dbg22 | Hardware debug pin 22 | O | G32 / AL9 |
| hw_dbg23 | Hardware debug pin 23 | O | G33 / AM8 |
| hw_dbg24 | Hardware debug pin 24 | O | G24 / AL8 |
| hw_dbg25 | Hardware debug pin 25 | O | H24 / AN7 |
| hw_dbg26 | Hardware debug pin 26 | O | E24 / AE7 |
| hw_dbg27 | Hardware debug pin 27 | O | F24 / AD7 |
| hw_dbg28 | Hardware debug pin 28 | O | G21 / AL32 |
| hw_dbg29 | Hardware debug pin 29 | O | H21 / AL31 |
| hw_dbg30 | Hardware debug pin 30 | O | E21 / AK31 |
| hw_dbg31 | Hardware debug pin 31 | O | F21 / AK32 |

(1) NA in this table stands for not applicable for the device.

3.4.7 General-Purpose IOs (GPIOs)

NOTE

For more information, see the General-Purpose Interface section of the Device TRM.

NOTE

Note that the following naming convention is used for the GPIO: gpio(N)_(wk)(In / Out)(Number)

With:

- N: bank name
 - wk (for wakeable): the always-on GPIOs that have the capability to wake-up domains. If not specified, this means that the GPIO is not wakeable.
 - In: Input only general-purpose signal
 - Out: Output only general-purpose signal
-

Table 3-35. GPIO Signal Descriptions⁽²⁾

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|---|----------|-------------------|
| gpio1_wk10 | General-purpose IO, always on, wakeable | IO | NA ⁽³⁾ |
| gpio1_wk11 | General-purpose IO, always on, wakeable | IO | P31 |
| gpio1_wk12 | General-purpose IO, always on, wakeable | IO | M31 |
| gpio1_wk13 | General-purpose IO, always on, wakeable | IO | N31 |
| gpio1_wk14 | General-purpose IO, always on, wakeable | IO | N28 |
| gpio1_wk15 | General-purpose IO, always on, wakeable | IO | N29 |
| gpio1_wk16 | General-purpose IO, always on, wakeable | IO | R33 |
| gpio1_wk17 | General-purpose IO, always on, wakeable | IO | T32 |
| gpio1_wk6 | General-purpose IO, always on, wakeable | IO | K32 |
| gpio1_wk7 | General-purpose IO, always on, wakeable | IO | K31 |
| gpio1_wk8 | General-purpose IO, always on, wakeable | IO | NA ⁽³⁾ |
| gpio1_wk9 | General-purpose IO, always on, wakeable | IO | NA ⁽³⁾ |
| gpio1_wkout0 | General-purpose output, always on, wakeable | O | U31 |
| gpio1_wkout1 | General-purpose output, always on, wakeable | O | U32 |
| gpio1_wkout2 | General-purpose output, always on, wakeable | O | U33 |
| gpio1_wkout3 | General-purpose output, always on, wakeable | O | V31 |
| gpio1_wkout4 | General-purpose output, always on, wakeable | O | V32 |
| gpio1_wkout5 | General-purpose output, always on, wakeable | O | NA ⁽³⁾ |
| gpio2_32 | General-purpose IO | IO | P32 |
| gpio2_33 | General-purpose IO | IO | E25 |
| gpio2_34 | General-purpose IO | IO | F25 |
| gpio2_35 | General-purpose IO | IO | J29 |
| gpio2_36 | General-purpose IO | IO | J28 |
| gpio2_37 | General-purpose IO | IO | J27 |
| gpio2_38 | General-purpose IO | IO | H28 |
| gpio2_39 | General-purpose IO | IO | H29 |
| gpio2_40 | General-purpose IO | IO | G29 |
| gpio2_41 | General-purpose IO | IO | E29 |
| gpio2_42 | General-purpose IO | IO | E27 |
| gpio2_43 | General-purpose IO | IO | F26 |
| gpio2_44 | General-purpose IO | IO | E26 |

Table 3-35. GPIO Signal Descriptions⁽²⁾ (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|--------------------|----------|-------------------|
| gpio2_45 | General-purpose IO | IO | N27 |
| gpio2_46 | General-purpose IO | IO | AJ10 |
| gpio2_47 | General-purpose IO | IO | AH10 |
| gpio2_48 | General-purpose IO | IO | AG10 |
| gpio2_49 | General-purpose IO | IO | AF10 |
| gpio2_50 | General-purpose IO | IO | AH9 |
| gpio2_51 | General-purpose IO | IO | AJ9 |
| gpio2_52 | General-purpose IO | IO | AG9 |
| gpio2_53 | General-purpose IO | IO | AJ8 |
| gpio2_54 | General-purpose IO | IO | AH8 |
| gpio2_55 | General-purpose IO | IO | AJ7 |
| gpio2_56 | General-purpose IO | IO | J32 |
| gpio2_57 | General-purpose IO | IO | J33 |
| gpio2_58 | General-purpose IO | IO | H32 |
| gpio2_59 | General-purpose IO | IO | J31 |
| gpio2_60 | General-purpose IO | IO | G31 |
| gpio2_61 | General-purpose IO | IO | H31 |
| gpio2_62 | General-purpose IO | IO | G32 |
| gpio2_63 | General-purpose IO | IO | G33 |
| gpio3_64 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_65 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_66 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_67 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_68 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_69 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_70 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_71 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_72 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_73 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_74 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_75 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_76 | General-purpose IO | IO | G20 |
| gpio3_77 | General-purpose IO | IO | F20 |
| gpio3_78 | General-purpose IO | IO | F17 |
| gpio3_79 | General-purpose IO | IO | E20 |
| gpio3_80 | General-purpose IO | IO | E14 |
| gpio3_81 | General-purpose IO | IO | F14 |
| gpio3_82 | General-purpose IO | IO | G14 |
| gpio3_83 | General-purpose IO | IO | E17 |
| gpio3_84 | General-purpose IO | IO | F13 |
| gpio3_85 | General-purpose IO | IO | N9 |
| gpio3_86 | General-purpose IO | IO | G13 |
| gpio3_87 | General-purpose IO | IO | E13 |
| gpio3_92 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_93 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio3_94 | General-purpose IO | IO | K28 |
| gpio3_95 | General-purpose IO | IO | K29 |

Table 3-35. GPIO Signal Descriptions⁽²⁾ (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|--------------------|----------|-------------------|
| gpio4_100 | General-purpose IO | IO | AE27 |
| gpio4_101 | General-purpose IO | IO | AD29 |
| gpio4_102 | General-purpose IO | IO | AD28 |
| gpio4_103 | General-purpose IO | IO | AF29 |
| gpio4_104 | General-purpose IO | IO | AG29 |
| gpio4_105 | General-purpose IO | IO | AD26 |
| gpio4_106 | General-purpose IO | IO | AD27 |
| gpio4_107 | General-purpose IO | IO | AA26 |
| gpio4_108 | General-purpose IO | IO | AA27 |
| gpio4_109 | General-purpose IO | IO | AA28 |
| gpio4_110 | General-purpose IO | IO | AA29 |
| gpio4_111 | General-purpose IO | IO | Y29 |
| gpio4_112 | General-purpose IO | IO | Y28 |
| gpio4_113 | General-purpose IO | IO | G24 |
| gpio4_114 | General-purpose IO | IO | H24 |
| gpio4_115 | General-purpose IO | IO | E24 |
| gpio4_116 | General-purpose IO | IO | F24 |
| gpio4_117 | General-purpose IO | IO | G21 |
| gpio4_118 | General-purpose IO | IO | H21 |
| gpio4_119 | General-purpose IO | IO | E21 |
| gpio4_120 | General-purpose IO | IO | F21 |
| gpio4_96 | General-purpose IO | IO | W32 |
| gpio4_97 | General-purpose IO | IO | AF28 |
| gpio4_98 | General-purpose IO | IO | AE29 |
| gpio4_99 | General-purpose IO | IO | AE28 |
| gpio5_128 | General-purpose IO | IO | AH25 |
| gpio5_129 | General-purpose IO | IO | AG25 |
| gpio5_130 | General-purpose IO | IO | AJ26 |
| gpio5_131 | General-purpose IO | IO | AH26 |
| gpio5_132 | General-purpose IO | IO | AK28 |
| gpio5_133 | General-purpose IO | IO | AJ27 |
| gpio5_134 | General-purpose IO | IO | AL32 |
| gpio5_135 | General-purpose IO | IO | AL31 |
| gpio5_136 | General-purpose IO | IO | AK31 |
| gpio5_137 | General-purpose IO | IO | AK32 |
| gpio5_138 | General-purpose IO | IO | AL33 |
| gpio5_139 | General-purpose IO | IO | AM32 |
| gpio5_140 | General-purpose IO | IO | AM30 |
| gpio5_141 | General-purpose IO | IO | AL30 |
| gpio5_142 | General-purpose IO | IO | AL29 |
| gpio5_143 | General-purpose IO | IO | AN31 |
| gpio5_144 | General-purpose IO | IO | AM31 |
| gpio5_145 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio5_146 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio5_147 | General-purpose IO | IO | AL28 |
| gpio5_148 | General-purpose IO | IO | AL30 |
| gpio5_149 | General-purpose IO | IO | NA ⁽³⁾ |

Table 3-35. GPIO Signal Descriptions⁽²⁾ (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--------------------------|------------------------|-----------------|--------------------------|
| gpio5_150 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio5_151 | General-purpose IO | IO | NA ⁽³⁾ |
| gpio5_152 | General-purpose IO | IO | AN29 |
| gpio5_153 | General-purpose IO | IO | AJ25 |
| gpio5_154 | General-purpose IO | IO | AJ24 |
| gpio5_155 | General-purpose IO | IO | AG24 |
| gpio5_156 | General-purpose IO | IO | AH24 |
| gpio5_158 | General-purpose IO | IO | K26 |
| gpio5_159 | General-purpose IO | IO | K27 |
| gpio6_160 | General-purpose IO | IO | AN13 |
| gpio6_161 | General-purpose IO | IO | AM13 |
| gpio6_162 | General-purpose IO | IO | AL12 |
| gpio6_163 | General-purpose IO | IO | AL13 |
| gpio6_164 | General-purpose IO | IO | AL18 |
| gpio6_165 | General-purpose IO | IO | AM18 |
| gpio6_166 | General-purpose IO | IO | AL17 |
| gpio6_167 | General-purpose IO | IO | AM17 |
| gpio6_168 | General-purpose IO | IO | AN17 |
| gpio6_169 | General-purpose IO | IO | AL16 |
| gpio6_170 | General-purpose IO | IO | AM16 |
| gpio6_171 | General-purpose IO | IO | AL15 |
| gpio6_172 | General-purpose IO | IO | AM15 |
| gpio6_173 | General-purpose IO | IO | AN15 |
| gpio6_174 | General-purpose IO | IO | AL14 |
| gpio6_175 | General-purpose IO | IO | AM14 |
| gpio6_176 | General-purpose IO | IO | AM12 |
| gpio6_177 | General-purpose IO | IO | AL11 |
| gpio6_178 | General-purpose IO | IO | AM11 |
| gpio6_179 | General-purpose IO | IO | AN11 |
| gpio6_180 | General-purpose IO | IO | AL10 |
| gpio6_181 | General-purpose IO | IO | AM10 |
| gpio6_182 ⁽¹⁾ | General-purpose IO | IO | AN9 / AN9 ⁽¹⁾ |
| gpio6_183 ⁽¹⁾ | General-purpose IO | IO | AM9 / AM9 ⁽¹⁾ |
| gpio6_184 ⁽¹⁾ | General-purpose IO | IO | AL9 / AL9 ⁽¹⁾ |
| gpio6_185 ⁽¹⁾ | General-purpose IO | IO | AM8 / AM8 ⁽¹⁾ |
| gpio6_186 ⁽¹⁾ | General-purpose IO | IO | AL8 / AL8 ⁽¹⁾ |
| gpio6_187 ⁽¹⁾ | General-purpose IO | IO | AN7 / AN7 ⁽¹⁾ |
| gpio6_188 | General-purpose IO | IO | W31 |
| gpio6_189 | General-purpose IO | IO | W33 |
| gpio6_190 | General-purpose IO | IO | AJ33 |
| gpio6_191 | General-purpose IO | IO | AK30 |
| gpio7_192 | General-purpose IO | IO | AN23 |
| gpio7_193 | General-purpose IO | IO | AM23 |
| gpio7_194 | General-purpose IO | IO | AM22 |
| gpio7_195 | General-purpose IO | IO | AL23 |
| gpio7_196 | General-purpose IO | IO | AF20 |
| gpio7_197 | General-purpose IO | IO | AH17 |

Table 3-35. GPIO Signal Descriptions⁽²⁾ (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|--------------------------|-----------------------|----------|--------------------------|
| gpio7_198 | General-purpose IO | IO | AG20 |
| gpio7_199 | General-purpose IO | IO | AH20 |
| gpio7_200 | General-purpose IO | IO | AJ21 |
| gpio7_201 | General-purpose IO | IO | AJ20 |
| gpio8_224 | General-purpose IO | IO | AE6 |
| gpio8_225 | General-purpose IO | IO | AE5 |
| gpio8_226 | General-purpose IO | IO | AF6 |
| gpio8_227 | General-purpose IO | IO | AE7 |
| gpio8_228 | General-purpose IO | IO | AD5 |
| gpio8_229 | General-purpose IO | IO | AD6 |
| gpio8_230 | General-purpose IO | IO | AD7 |
| gpio8_231 | General-purpose IO | IO | AJ5 |
| gpio8_232 | General-purpose IO | IO | AH4 |
| gpio8_233 ⁽¹⁾ | General-purpose IO | IO | AG5 / AG5 ⁽¹⁾ |
| gpio8_234 ⁽¹⁾ | General-purpose IO | IO | AF5 / AF5 ⁽¹⁾ |
| gpio8_in236 | General-purpose input | I | U6 |
| gpio8_in237 | General-purpose input | I | U5 |
| gpio8_in238 | General-purpose input | I | P5 |
| gpio8_in239 | General-purpose input | I | P6 |
| gpio8_in240 | General-purpose input | I | P8 |
| gpio8_in241 | General-purpose input | I | P7 |
| gpio8_in242 | General-purpose input | I | N5 |
| gpio8_in243 | General-purpose input | I | N6 |
| gpio8_in244 | General-purpose input | I | N7 |
| gpio8_in245 | General-purpose input | I | N8 |
| gpio8_in246 | General-purpose input | I | Y6 |
| gpio8_in247 | General-purpose input | I | Y5 |
| gpio8_in248 | General-purpose input | I | Y7 |
| gpio8_in249 | General-purpose input | I | Y8 |
| gpio8_in250 | General-purpose input | I | AA5 |
| gpio8_in251 | General-purpose input | I | AA6 |
| gpio8_in252 | General-purpose input | I | J6 |
| gpio8_in253 | General-purpose input | I | J7 |
| gpio8_in254 | General-purpose input | I | K6 |
| gpio8_in255 | General-purpose input | I | K5 |

(1) gpio6_182, gpio6_183, gpio6_184, gpio6_185, gpio6_186, gpio6_187, gpio8_233, gpio8_234 GPIOs (balls AN9 / AM9 / AL9 / AM8 / AL8 / AN7 / AG5 / AG5 / AF5) can output the same GPIO in mode 0 or in mode 6.

(2) The following naming convention is used for the GPIO: gpio(N)_(wk)(In / Out)(Number) with:

- N: bank name
- wk (for wakeable): the always-on GPIOs that have the capability to wake-up domains. If not specified, this means that the GPIO is not wakeable.
- In: Input only general-purpose signal
- Out: Output only general-purpose signal

(3) NA in this table stands for not applicable for the device.

3.4.8 System and Miscellaneous

3.4.8.1 DM Timer

NOTE

For more information, see the Timers section of the Device TRM.

Table 3-36. DM Timer Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|------------------------------------|----------|-----------------|
| timer5_pwm_evt | DM timer event input or PWM output | IO | AD5 |
| timer6_pwm_evt | DM timer event input or PWM output | IO | AD6 |
| timer8_pwm_evt | DM timer event input or PWM output | IO | AD7 / AG5 |
| timer9_pwm_evt | DM timer event input or PWM output | IO | AJ33 |
| timer10_pwm_evt | DM timer event input or PWM output | IO | W31 |
| timer11_pwm_evt | DM timer event input or PWM output | IO | AE7 |

3.4.8.2 Keypad

NOTE

For more information, see Keyboard Controller / Keyboard Controller Environment section of the Device TRM.

Table 3-37. Keypad Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-----------------|-----------------|----------|-----------------|
| kbd_row0 | Keypad row 0 | I | J27 / AM8 |
| kbd_row1 | Keypad row 1 | I | H28 / AL8 |
| kbd_row2 | Keypad row 2 | I | H29 / AN7 |
| kbd_row3 | Keypad row 3 | I | G29 / AM14 |
| kbd_row4 | Keypad row 4 | I | E29 / AM18 |
| kbd_row5 | Keypad row 5 | I | E27 / AM13 |
| kbd_row6 | Keypad row 6 | I | F26 / AM11 |
| kbd_row7 | Keypad row 7 | I | E26 / AL11 |
| kbd_row8 | Keypad row 8 | I | J28 / AM12 |
| kbd_col0 | Keypad column 0 | O | J32 / AN9 |
| kbd_col1 | Keypad column 1 | O | J33 / AM9 |
| kbd_col2 | Keypad column 2 | O | H32 / AL9 |
| kbd_col3 | Keypad column 3 | O | J31 / AL14 |
| kbd_col4 | Keypad column 4 | O | G31 / AL18 |
| kbd_col5 | Keypad column 5 | O | H31 / AN13 |
| kbd_col6 | Keypad column 6 | O | G32 / AM10 |
| kbd_col7 | Keypad column 7 | O | G33 / AL10 |
| kbd_col8 | Keypad column 8 | O | F25 / AN11 |

3.4.8.3 System And Miscellaneous

NOTE

For more information, see:

- Power, Reset and Clock Management / PRCM Subsystem Environment / External Clock Signals section, or
- Power, Reset and Clock Management / PRCM Subsystem Environment / External Reset Signals section, or
- Power, Reset and Clock Management / PRCM Subsystem Environment / External Power Control Signals section of the Device TRM.

NOTE

Slicer functionality is not supported in the device.

Table 3-38. System And Miscellaneous Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|------------------------------|--|----------|-------------------|
| fref_xtal_in | Crystal oscillator input | AI - I | L32 |
| fref_xtal_out | Crystal oscillator output | AO | M32 |
| fref_xtal_clk ⁽¹⁾ | Crystal oscillator output – buffered directly from the input clock (dedicated for audio) | AO | L33 |
| fref_slicer_in | Slicer positive input clock | AI | NA ⁽²⁾ |
| fref_clk_ioreq | FREF input clock request for main clock | IO | N31 |
| fref_clk0_out | FREF clock 0 output: activated by default | O | M31 |
| fref_clk1_out | FREF clock 1 output | O | P31 |
| fref_clk2_out | FREF clock 2 output | O | NA ⁽²⁾ |
| fref_clk3_out | FREF clock 3 output | O | NA ⁽²⁾ |
| fref_clk1_req | FREF clock request 1 | I | NA ⁽²⁾ |
| fref_clk2_req | FREF clock request 2 | I | NA ⁽²⁾ |
| sys_32k | 32-kHz clock input | I | L31 |
| sys_nreswron | OMAP power-on reset input | I | N33 |
| sys_nreswarm | System warm reset output or input | IOD | N32 |
| sys_pwr_req | Power request to exit off mode. Active high by default but configurable | O | T31 |
| sys_nirq1 | External interrupt 1 (aimed at PMIC power device connection) | I | R33 |
| sys_nirq2 | External interrupt 2 (aimed at PMIC power device connection) | I | T32 |
| sys_drm_msecure | Secure transaction mode request (companion 0) | O | AF5 |
| sys_aux_msecure | Secure transaction mode request (companion 1) | O | NA ⁽²⁾ |
| sys_secure_indicator | Secure transaction mode external indication | O | AG5 |
| sys_boot0 | Boot configuration: latched at power-on reset | I | U31 |
| sys_boot1 | Boot configuration: latched at power-on reset | I | U32 |
| sys_boot2 | Boot configuration: latched at power-on reset | I | U33 |
| sys_boot3 | Boot configuration: latched at power-on reset | I | V31 |
| sys_boot4 | Boot configuration: latched at power-on reset | I | V32 |
| sys_boot5 | Boot configuration: latched at power-on reset | I | NA ⁽²⁾ |
| sys_ndmareq0 | External DMA request pipe 1 | I | AN29 |
| sys_ndmareq1 | External DMA request pipe 2 | I | NA ⁽²⁾ |
| sys_nodeid0 | cJTAG node identifier bit 0 (up to 4 processors) | I | AE6 |
| sys_nodeid1 | cJTAG node identifier bit 1 (up to 4 processors) | I | AE5 |

- (1) `fref_xtal_clk` is dedicated to audio purpose. A clean network is recommended.
 (2) NA in this table stands for not applicable for the device.

3.4.8.4 Power Supplies

NOTE

For more information, see Power, Reset and Clock Management / PRCM Subsystem Environment / External Voltage Inputs section of the Device TRM.

Table 3-39. Power Supply Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-------------------------------|---|----------|--|
| <code>vdds_1p8</code> | Second IO power supply signal to ensure the VDDS ramping, and power supply for IO banks 2, 4, 5, 8-12, 14-16, 18, 19, 21, 23-26 | PWR | H20 / J23 / J22 / J14 / J13 / J12 / L9 / M9 / P26 / P25 / R25 / U27 / U26 / W25 / Y25 / Y9 / AA25 / AA9 / AB25 / AC25 / AC9 / AD25 / AE24 / AE21 / AE15 / AE14 / AE13 / AF21 / U28 |
| <code>vdds_emmc</code> | eMMC dual voltage IO power supply | PWR | AB9 |
| <code>vdds_c2c</code> | Miscellaneous IO power supply | PWR | J21 / J20 |
| <code>vdds_hsic</code> | HS interchip data power supply | PWR | N26 |
| <code>vdda_dsiporta</code> | DSI PHY (Port A) display primary port 1 – (main cut) power supply | PWR | AA33 |
| <code>vssa_dsiporta</code> | DSI PHY (Port A) ground | GND | Y30 |
| <code>vdda_dsiportc</code> | DSI PHY (Port C) display primary port 2 – main cut power supply | PWR | AE33 |
| <code>vssa_dsiportc</code> | DSI PHY (Port C) ground | GND | AD30 |
| <code>vdds_hdmi</code> | HDMI (digital part) power supply | PWR | AE23 |
| <code>vdda_hdmi</code> | HDMI PHY (TMDS) power supply | PWR | AN25 |
| <code>vssa_hdmi</code> | HDMI PHY ground | GND | AK24 |
| <code>vdda_csiporta</code> | CSI (Port A) PHY camera (main cut) power supply | PWR | N3 |
| <code>vssa_csiporta</code> | CSI (Port A) PHY camera (main cut) ground | GND | P4 |
| <code>vdda_csiportb</code> | CSI (Port B) PHY camera (main cut) power supply | PWR | AA7 |
| <code>vssa_csiportb</code> | CSI (Port B) PHY camera (main cut) ground | GND | Y4 |
| <code>vdda_csiportc</code> | CSI (Port C) PHY camera (main cut) power supply | PWR | J5 |
| <code>vssa_csiportc</code> | CSI (Port C) PHY camera (main cut) ground | GND | K4 |
| <code>vdda_sata</code> | SATA PHY power supply | PWR | E9 |
| <code>vssa_sata</code> | SATA PHY ground | GND | D10 |
| <code>vdds_sdcard</code> | SD Card power supply | PWR | E5 |
| <code>vdds_usbhs18</code> | USB HS (digital part) power supply | PWR | AE18 |
| <code>vdda_usbhs33</code> | USB HS PHY power supply | PWR | AN21 |
| <code>vssa_usbhs</code> | USB HS PHY ground | GND | AK20 |
| <code>vdda_usbss18</code> | USB SS DRD PHY power supply | PWR | AE19 |
| <code>vssa_usbss</code> | USB SS PHY ground | GND | AK21 |
| <code>vdds_osc</code> | Crystal oscillator IO power supply | PWR | J24 |
| <code>vssa_xtal</code> | Crystal oscillator IO Kelvin ground (same routing as OMAP3630 and OMAP4430) | GND | L30 |
| <code>vddq_vref_ddrch1</code> | VREF cell power supply for DDR3 and DDR3L DQ channel 1 (or EMIF1) | PWR | J16 |
| <code>vddq_vref_ddrch2</code> | VREF cell power supply for DDR3 and DDR3L DQ channel 2 (or EMIF2) | PWR | V10 |

Table 3-39. Power Supply Signal Descriptions (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|-------------------------------|--|----------|---|
| vdds_dds_ch1 | DDR3 and DDR3L (Channel 1) dm / dq / ndqs / addr / ba / ncas / nras / nreset / nwe / odt power supply | PWR | A27 / A11 / A3 / H30 / H10 / J19 / J18 / J10 / K30 / K25 / K23 / K15 / K14 / L25 / M25 / A21 |
| vdds_dds_ch2 | DDR3 and DDR3L (Channel 2) dm / dq / ndqs / addr / ba / ncas / nras / nreset / nwe / odt power supply | PWR | E1 / J9 / K8 / N1 / R9 / T9 / V9 / W9 / AA1 / AC10 / AE12 / AE11 / AE10 / AJ1 / AM2 |
| ddrch1_vref_dq | DDR3 and DDR3L, DQ Channel 1 VREF output power supply to memory | PWR | A19 |
| ddrch2_vref_dq | DDR3 and DDR3L, DQ Channel 2 VREF output power supply to memory | PWR | U1 |
| ddr3ch1_vref_ca | DDR3 and DDR3L addr / ba / ncas / nras / nreset / nwe / odt Channel 1 VREF output power supply to memory | PWR | A9 |
| ddr3ch2_vref_ca | DDR3 and DDR3L addr / ba / ncas / nras / nreset / nwe / odt Channel 2 VREF output power supply to memory | PWR | AE1 |
| vdd_core | Core and oscillator power supply | PWR | J11 / K22 / K12 / K11 / K9 / L14 / L13 / L12 / L10 / M14 / M13 / M11 / M10 / N15 / N14 / N11 / P11 / W24 / W22 / Y24 / Y23 / AA23 / AB24 / AB23 / AC24 / AC22 / AC21 / AD23 / AD22 / AD20 / AD16 / AD15 / AD14 / AD12 |
| vdd_core_sense ⁽¹⁾ | Core and oscillator output sensor feedback | PWR | AH21 |
| vdd_mm | Multimedia power supply | PWR | T14 / T13 / T11 / T10 / W13 / W12 / W10 / Y19 / Y15 / Y11 / Y10 / AA19 / AA16 / AA15 / AA11 / AB19 / AB15 / AB13 / AB11 / AB10 / AC20 / AC16 / AC14 / AC13 / AC12 / AD19 / AD11 |
| vdd_mm_sense ⁽¹⁾ | Multimedia sensor output sensor feedback | PWR | AG21 |
| vdd_mpu | MPU power supply | PWR | K20 / K19 / K18 / L24 / L22 / L21 / L20 / L18 / M24 / M23 / M20 / M19 / N23 / N18 / P24 / P23 / P22 / P18 / R24 / T24 / T23 / T21 / T20 |
| vdd_mpu_sense ⁽¹⁾ | MPU sensor output sensor feedback | PWR | U29 |
| vss_mpu_sense ⁽¹⁾ | MPU sensor output sensor feedback ground | GND | AJ29 |
| vpp1 | eFuse power supply | PWR | AD9 |
| vss | Main ground | GND | D28 / D26 / D24 / D23 / D21 / D20 / D18 / D16 / D14 / D13 / D11 / D8 / D6 / F4 / H4 / L16 / L4 / M21 / M17 / M15 / N30 / N22 / N21 / N20 / N19 / N17 / N16 / N13 / N12 / N4 / P30 / P21 / P19 / P16 / P15 / P13 / P12 / P10 / P9 / R22 / R21 / R20 / R19 / R18 / R17 / R16 / R15 / R14 / R13 / R12 / R10 / T30 / T19 / T17 / T15 / T4 / U22 / U21 / U19 / U18 / U17 / U16 / U15 / U13 / U12 / V30 / V24 / V23 / V21 / V20 / V19 / V17 / V15 / V14 / V13 / V11 / V4 / W21 / W20 / W19 / W18 / W17 / W16 / W15 / W14 / Y22 / Y21 / Y18 / Y16 / Y13 / Y12 / AA30 / AA22 / AA21 / AA20 / AA18 / AA17 / AA14 / AA13 / AA12 / AA4 / AB21 / AB20 / AB17 / AB14 / AC30 / AC18 / AC4 / AD4 / AF30 / AF4 / AH30 / AK26 / AK23 / AK14 / AK13 / F30 / AK11 / AK10 / AK8 / AK6 |
| vdda_dppll_core_emu_abe | Core, EMU, and ABE DPLL power supply | PWR | Y26 |
| vdda_dppll_mm_l4per | MM and L4 interconnect DPLL power supply | PWR | U8 |
| vdda_dppll_hdmi | HDMI PHY DPLL power supply | PWR | AF24 |
| vdda_dppll_mpu | MPU DPLL power supply | PWR | Y27 |
| vdda_ldo_core | Core SRAM LDO power supply | PWR | AE22 |
| vdda_ldo_mm | MM SRAM LDO power supply | PWR | AE20 |
| vdda_ldo_mpu | MPU SRAM LDO power supply | PWR | J15 |
| vdda_ldo_emu_wkup | Wake-up / emulation LDOs power supply | PWR | N25 |

Table 3-39. Power Supply Signal Descriptions (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM [4] |
|------------------------------|---------------------------------|----------|-----------------|
| vdda_vbgap_core | Bandgap, core LDOs power supply | PWR | AE16 |
| cap_vdda_ldo_sram_core_array | Core SRAM array LDO output | PWR | T25 |
| cap_vdda_ldo_sram_mm_array | MM SRAM array LDO output | PWR | AG17 |
| cap_vdda_ldo_sram_mpu_array | MPU SRAM array LDO output | PWR | H17 |
| cap_vdda_ldo_sram_mpu_array2 | MPU SRAM array2 LDO output | PWR | K16 |
| cap_vddldo_emu_wkup | MPU wake-up and EMU LDO output | PWR | V25 |
| cap_vbb_ldo_mm | MPU MM LDO output | PWR | AD18 |
| cap_vbb_ldo_mpu | MPU MPU LDO output | PWR | H13 |

(1) An optimized power distribution network is recommended for vdd_mpu_sense, vss_mpu_sense, vdd_mm_sense, and vdd_core_sense SMPS feedback sensors between the Device and the power management IC (PMIC).

4 Specifications

NOTE

For more information, see Power, Reset and Clock Management / PRCM Subsystem Environment / External Voltage Inputs or Initialization / Preinitialization / Power Requirements section of the Device TRM.

4.1 Absolute Maximum Ratings

Stresses beyond those listed as absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under , *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 4-1. Absolute Maximum Rating Over Junction Temperature Range

| PARAMETER | | Limits |
|--|---|-----------------------------|
| Supply voltage ranges (steady state) | Core (vdd_mpu, vdd_mm, vdd_core, vdds_hsic, vddq_vref_ddrch1, vddq_vref_ddrch2, vdda_ldo_emu_wkup) | –0.4 V to 1.5 V |
| | I/O analog (vdds_1p8, vdda_dsiporta, vdda_dsiportc, vdda_hdmi, vdda_csiporta, vdda_csiportb, vdda_csiportc, vdda_sata, vdds_usbhs18, vdda_usbss18, vdda_dpil_core_emu_abe, vdda_dpil_mm_l4per, vdda_dpil_hdmi, vdda_dpil_mpu, vdda_ldo_mm, vdda_ldo_mpu, vdda_vbgap_core) | –0.5 V to 2.0 V |
| | I/O 1.8 V (vdds_c2c, vdds_hdmi, vdds_osc, vdda_ldo_core, vdds_emmc) | –0.5 V to 2.1 V |
| | I/O 3.3 V (vdds_sdcard, vdda_usbhs33) | –0.5 V to 3.8 V |
| Input and output voltage ranges (steady state) | Core I/Os | –0.4 V to 1.5 V |
| | Analog I/Os | –0.5 V to 2.0 V |
| | 1.8-V I/Os | –0.5 V to 2.1 V |
| | 3.3-V dual-voltage I/Os operating at 1.8 V | –0.5 V to 2.1 V |
| | 3.3-V I/Os | –0.5 V to 3.8 V |
| T _J | Absolute junction temperature range (vpp turned off—floating) | –40°C to 125°C |
| Latch-up I-test performance | Current-pulse injection on each I/O pin | ±100 mA ⁽¹⁾ |
| Latch-up overvoltage performance | Voltage injection on each supply | 1.5 × Vddmax ⁽²⁾ |

(1) Pins stressed per JEDEC JESD78D at 120°C (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

(2) Supplies stressed per JEDEC JESD78D at 120°C (Class II) and passed specified voltage injection.

Table 4-2 summarizes the maximum estimated power consumption at the ball level.

Table 4-2. Maximum Current Ratings at Ball Level⁽¹⁾

| PARAMETER | | MAX | UNIT |
|-------------------------|---|--------------------|------|
| vdd_mpu ⁽¹⁾ | Maximum current rating for MPU MPU at HIGH | 4400 | mA |
| vdd_mm ⁽¹⁾ | Maximum current rating for multimedia | 2145 | mA |
| vdd_core ⁽¹⁾ | Maximum current rating for core, DLL | 890 | mA |
| vdds_1p8 | Maximum current rating for second IO signal to ensure the VDDS ramping | See ⁽³⁾ | mA |
| vdds_emmc | Maximum current rating for eMMC dual-voltage IO | See ⁽³⁾ | mA |
| vdds_c2c | Maximum current rating for Miscalenious IO | See ⁽³⁾ | mA |
| vdds_hsic | Maximum current rating for HS interchip data | See ⁽³⁾ | mA |
| vdda_dsiporta | Maximum current rating for DSI PHY (Port A) display primary port 1 (main cut), DSI1_A | 19.3 | mA |
| vdda_dsiportc | Maximum current rating for DSI PHY (Port C) display primary port 2 (main cut), DSI1_C | 19.3 | mA |
| vdds_hdmi | Maximum current rating for HDMI IOs (CEC, HPD, DDC) | See ⁽³⁾ | mA |

Table 4-2. Maximum Current Ratings at Ball Level⁽¹⁾ (continued)

| PARAMETER | | MAX | UNIT |
|-------------------------|--|--------------------|------|
| vdda_hdmi | Maximum current rating for HDMI PHY (TMDS) | 15.0 | mA |
| vdda_csiporta | Maximum current rating for CSI (Port A) PHY camera (main cut) | 4.6 | mA |
| vdda_csiportb | Maximum current rating for CSI (Port B) PHY camera (main cut) | 2.7 | mA |
| vdda_csiportc | Maximum current rating for CSI (Port C) PHY camera (main cut) | 1.75 | mA |
| vdda_sata | Maximum current rating for SATA PHY | 40.0 | mA |
| vdds_sdcard | Maximum current rating for SD Card | See ⁽³⁾ | mA |
| vdds_usbhs18 | Maximum current rating for USB HS (digital part) | 26.0 | mA |
| vdda_usbhs33 | Maximum current rating for USB HS PHY | 34.0 | mA |
| vdda_usbss18 | Maximum current rating for USB SS DRD PHY | 45.0 | mA |
| vdds_osc | Maximum current rating for crystal oscillator IO | 2.0 | mA |
| vdds_ddr_ch1 | Maximum current rating for DDR3 and DDR3L (channel 1) dm / dq / ndqs | 400 | mA |
| vdds_ddr_ch2 | Maximum current rating for DDR3 and DDR3L (channel 2) dm / dq / ndqs | 400 | mA |
| vddq_vref_ddrch1 | Maximum current rating for VREF cell power supply for DDR3 and DDR3L DQ channel 1 (or EMIF1) | 400 | mA |
| vddq_vref_ddrch2 | Maximum current rating for VREF cell power supply for DDR3 and DDR3L DQ channel 2 (or EMIF2) | 400 | mA |
| vpp1 ⁽²⁾ | Maximum current rating for eFuse | 50 | mA |
| vdda_dppll_core_emu_abe | Maximum current rating for core, EMU, and ABE DPLL | 9.0 | mA |
| vdda_dppll_mm_l4per | Maximum current rating for MM and L4 interconnect DPLL | 6.0 | mA |
| vdda_dppll_hdmi | Maximum current rating for HDMI PHY DPLL | 6.0 | mA |
| vdda_dppll_mpu | Maximum current rating for MPU DPLL | 3.0 | mA |
| vdda_ldo_core | Maximum current rating for core SRAM LDO | 60.0 | mA |
| vdda_ldo_mm | Maximum current rating for MM SRAM LDO | 85.0 | mA |
| vdda_ldo_mpu | Maximum current rating for MPU SRAM LDO | 145.0 | mA |
| vdda_ldo_emu_wkup | Maximum current rating for wake-up / emulation LDOs | 75.0 | mA |
| vdda_vbgap_core | Maximum current rating for bandgap, core LDOs | 5.0 | mA |

(1) With SmartReflex™ enabled

(2) VPP1 must not be connected.

(3) The sum of the maximum current consumption for these power supplies is 260 mA.

4.2 Recommended Operating Conditions

The device is used under the recommended operating conditions described in [Table 4-3](#).

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 4-3. Recommended Operating Conditions

| PARAMETER | DESCRIPTION | MIN ⁽²⁾ | NOM | MAX DC ⁽³⁾ | MAX ⁽²⁾ | UNIT |
|---|---|--------------------------------|------|-----------------------|--------------------|---------------------|
| Input Power Supply Voltage Range | | | | | | |
| vdd_mpu | Supply voltage range for MPU domain | See Table 4-8 | | | | V |
| vdd_mm | Supply voltage range for multimedia domain | See Table 4-10 | | | | V |
| vdd_core | Supply voltage range for OMAP core and DLL domain | See Table 4-13 | | | | V |
| vdda_dppll_mpu | Supply voltage for MPU DPLLs | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | 50 | | | mV _{PPmax} |

Table 4-3. Recommended Operating Conditions (continued)

| PARAMETER | DESCRIPTION | MIN ⁽²⁾ | NOM | MAX DC ⁽³⁾ | MAX ⁽²⁾ | UNIT | |
|----------------------------|---|--------------------|------|-----------------------|--------------------|---------------------|---------------------|
| vdda_dpll_core_emu_ab e | Supply voltage for core, emulation, and audio DPLLs | 1.71 | 1.80 | 1.836 | 1.89 | V | |
| | Maximum noise (peak-peak) | | 50 | | | mV _{PPmax} | |
| vdda_dpll_mm_l4per | Supply voltage for multimedia and L4 interconnect DPLLs | 1.71 | 1.80 | 1.836 | 1.89 | V | |
| | Maximum noise (peak-peak) | | 50 | | | mV _{PPmax} | |
| vdda_dpll_hdmi | Supply voltage for HDMI DPLL | 1.71 | 1.80 | 1.836 | 1.89 | V | |
| | Maximum noise (peak-peak) | | 50 | | | mV _{PPmax} | |
| vdda_ldo_mpu | Supply voltage for MPU SRAM LDO | 1.71 | 1.80 | 1.836 | 1.89 | V | |
| | Maximum noise (peak-peak) | | 50 | | | mV _{PPmax} | |
| vdda_ldo_core | Supply voltage for core SRAM LDO | 1.71 | 1.80 | | 1.89 | V | |
| | Maximum noise (peak-peak) | | 50 | | | mV _{PPmax} | |
| vdda_ldo_mm | Supply voltage for MM SRAM LDO | 1.71 | 1.80 | 1.836 | 1.89 | V | |
| | Maximum noise (peak-peak) | | 50 | | | mV _{PPmax} | |
| vdda_ldo_emu_wkup | Supply voltage for wake-up and emulation LDOs | 1.14 | 1.20 | | 1.26 | V | |
| | Maximum noise (peak-peak) | | 50 | | | mV _{PPmax} | |
| vdda_vbgap_core | Supply voltage for bandgap, core LDOs power supply | 1.71 | 1.80 | 1.836 | 1.89 | V | |
| | Maximum noise (peak-peak) | | 50 | | | mV _{PPmax} | |
| vdda_csiporta | Supply voltage for CSI (Port A) PHY camera (main cut) | 1.5-V Mode | 1.43 | 1.50 | 1.53 | 1.57 | V |
| | | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | |
| | Maximum noise (peak-peak) | 1.5-V Mode | | 50 | | | mV _{PPmax} |
| | | 1.8-V Mode | | | | | |
| vdda_csiportb | Supply voltage for CSI (Port B) PHY camera (main cut) | 1.5-V Mode | 1.43 | 1.50 | 1.53 | 1.57 | V |
| | | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | |
| | Maximum noise (peak-peak) | 1.5-V Mode | | 50 | | | mV _{PPmax} |
| | | 1.8-V Mode | | | | | |
| vdda_csiportc | Supply voltage for CSI (Port C) PHY camera (main cut) | 1.5-V Mode | 1.43 | 1.50 | 1.53 | 1.57 | V |
| | | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | |
| | Maximum noise (peak-peak) | 1.5-V Mode | | 50 | | | mV _{PPmax} |
| | | 1.8-V Mode | | | | | |
| vdda_dsiporta | Supply voltage for DSI PHY (Port A) display primary port 1—(main cut), DSI1_A | 1.5-V Mode | 1.43 | 1.50 | 1.53 | 1.57 | V |
| | | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | |
| | Maximum noise (peak-peak) | 1.5-V Mode | | 50 | | | mV _{PPmax} |
| | | 1.8-V Mode | | | | | |
| vdda_dsiportc | Supply voltage for DSI PHY (Port C) display primary port 2—main cut, DSI1_C | 1.5-V Mode | 1.43 | 1.50 | 1.53 | 1.57 | V |
| | | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | |
| | Maximum noise (peak-peak) | 1.5-V Mode | | 50 | | | mV _{PPmax} |
| | | 1.8-V Mode | | | | | |
| vdda_hdmi | Supply voltage for HDMI (analog part) | 1.5-V Mode | 1.43 | 1.50 | 1.53 | 1.57 | V |
| | | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | |
| | Maximum noise (peak-peak) | 1.5-V Mode | | 50 | | | mV _{PPmax} |
| | | 1.8-V Mode | | | | | |

Table 4-3. Recommended Operating Conditions (continued)

| PARAMETER | DESCRIPTION | MIN ⁽²⁾ | NOM | MAX DC ⁽³⁾ | MAX ⁽²⁾ | UNIT | |
|---------------------|---|--------------------|------|-----------------------|--------------------|------|---------------------|
| vdds_hdmi | Supply voltage for HDMI IOs (CEC, HPD, DDC) | 1.2-V Mode | 1.14 | 1.20 | | 1.26 | V |
| | | 1.8-V Mode | 1.71 | 1.80 | | 1.89 | |
| | Maximum noise (peak-peak) | 1.2-V Mode | | 50 | | | mV _{PPmax} |
| | | 1.8-V Mode | | | | | |
| vdda_sata | Supply voltage for SATA PHY | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | mV _{PPmax} |
| vdda_usbhs33 | Supply voltage for USB HS PHY | 3.3-V Mode | 3.14 | 3.30 | 3.366 | 3.46 | V |
| | Maximum noise (peak-peak) | 3.3-V Mode | | 50 | | | mV _{PPmax} |
| vdds_usbhs18 | Supply voltage for USB HS (digital part) | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | mV _{PPmax} |
| vdda_usbss18 | Supply voltage for USB SS DRD PHY | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | mV _{PPmax} |
| vdds_c2c | Supply voltage for Miscalenious IO | 1.2-V Mode | 1.14 | 1.20 | | 1.26 | V |
| | | 1.8-V Mode | 1.71 | 1.80 | | 1.89 | |
| | Maximum noise (peak-peak) | 1.2-V Mode | | 50 | | | mV _{PPmax} |
| | | 1.8-V Mode | | | | | |
| vdds_emmc | Supply voltage for eMMC | 1.2-V Mode | 1.14 | 1.20 | | 1.26 | V |
| | | 1.8-V Mode | 1.71 | 1.80 | | 1.89 | |
| | Maximum noise (peak-peak) | 1.2-V Mode | | 50 | | | mV _{PPmax} |
| | | 1.8-V Mode | | | | | |
| vdds_hsic | Supply voltage for HS interchip data | 1.2-V Mode | 1.14 | 1.20 | | 1.26 | V |
| | Maximum noise (peak-peak) | 1.2-V Mode | | 50 | | | mV _{PPmax} |
| vdds_osc | Supply voltage for crystal oscillator | 1.8-V Mode | 1.71 | 1.80 | | 1.89 | V |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | mV _{PPmax} |
| vdds_sdcard | Supply voltage for SD Card | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | | 3.0-V Mode | 2.70 | 3.00 | 3.06 | 3.60 | |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | mV _{PPmax} |
| | | 3.0-V Mode | | | | | |
| vdds_1p8v | Supply voltage for 1.8-V IO macros | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | mV _{PPmax} |
| vpp1 ⁽⁴⁾ | Supply voltage for eFuse | See ⁽⁴⁾ | | | | | V |
| vdds_ddr_ch1 | DDR3, DDR3 (Channel 1) dm / dq / ndqs / addr / ba / ncas / nras / nreset / nwe / odt power supply | 1.35 | 1.50 | 1.53 | 1.58 | | V |
| | DDR3L, DDR3L (Channel 1) dm / dq / ndqs / addr / ba / ncas / nras / nreset / nwe / odt power supply | 1.28 | 1.35 | 1.377 | 1.42 | | |
| | Maximum noise (peak-peak) | | | | 75 | | mV _{PPmax} |

Table 4-3. Recommended Operating Conditions (continued)

| PARAMETER | DESCRIPTION | MIN ⁽²⁾ | NOM | MAX DC ⁽³⁾ | MAX ⁽²⁾ | UNIT |
|--|---|-----------------------------|--------------------|-----------------------|---------------------|---------------------|
| vdds_dds_ch2 | DDR3, DDR3 (Channel 2) dm / dq / ndqs / addr / ba / ncas / nras / nreset / nwe / odt power supply | 1.35 | 1.50 | 1.53 | 1.58 | V |
| | DDR3L, DDR3L (Channel 2) dm / dq / ndqs / addr / ba / ncas / nras / nreset / nwe / odt power supply | 1.28 | 1.35 | 1.377 | 1.42 | |
| | Maximum noise (peak-peak) | | | | 75 | mV _{PPmax} |
| vddq_vref_ddsrch1 | VREF cell power supply for DDR3, DDR3L, DQ channel 1 (or EMIF1) | vdds_dds_ch1 ⁽⁵⁾ | | | | V |
| | Maximum noise (peak-peak) | | | | 75 | mV _{PPmax} |
| vddq_vref_ddsrch2 | VREF cell power supply for DDR3, DDR3L, DQ channel 2 (or EMIF2) | vdds_dds_ch2 ⁽⁵⁾ | | | | V |
| | Maximum noise (peak-peak) | | | | 75 | mV _{PPmax} |
| vss | Main ground | | 0 | | | V |
| vssa_dsiporta | DSI PHY (Port A) DSI1_A ground | | 0 | | | V |
| vssa_dsiportc | DSI PHY (Port C) DSI1_C ground | | 0 | | | V |
| vssa_hdmi | HDMI PHY ground | | 0 | | | V |
| vssa_csiporta | CSI (Port A) PHY camera (main cut) ground | | 0 | | | V |
| vssa_csiportb | CSI (Port B) PHY camera (main cut) ground | | 0 | | | V |
| vssa_csiportc | CSI (Port C) PHY camera (main cut) ground | | 0 | | | V |
| vssa_sata | SATA PHY ground | | 0 | | | V |
| vssa_usbhs | USB HS PHY ground | | 0 | | | V |
| vssa_usbss | USB SS PHY ground | | 0 | | | V |
| vssa_xtal | Crystal oscillator IO Kelvin ground (same routing as for OMAP3630 and OMAP4430) | | 0 | | | V |
| vss_mpu_sense | MPU sensor ground | | 0 | | | V |
| T _B ⁽⁶⁾ | Operating board (PCB) temperature range | –40 | | | 85 | °C |
| T _J ⁽⁶⁾ | Operating junction temperature range (vpp turned off—floating) | Extended –40 | | | 105 | |
| T _{J-VPP} ⁽⁴⁾ | Operating junction temperature range during eFuse programming (vpp turned on) | –10 | | | 65 | °C |
| Output Power Supply Voltage Range | | | | | | |
| ddrch1_vref_dq | DDR3, DDR3L DQ channel 1 VREF output power supply to memory | 0.49 × vdds_dds_ch1 | 0.5 × vdds_dds_ch1 | | 0.51 × vdds_dds_ch1 | V |
| | Maximum noise (peak-peak) | –0.01 × vdds_dds_ch1 | | | 0.01 × vdds_dds_ch1 | mV _{PPmax} |
| ddrch2_vref_dq | DDR3, DDR3L DQ channel 2 VREF output power supply to memory | 0.49 × vdds_dds_ch2 | 0.5 × vdds_dds_ch2 | | 0.51 × vdds_dds_ch2 | V |
| | Maximum noise (peak-peak) | –0.01 × vdds_dds_ch2 | | | 0.01 × vdds_dds_ch2 | mV _{PPmax} |

Table 4-3. Recommended Operating Conditions (continued)

| PARAMETER | DESCRIPTION | MIN ⁽²⁾ | NOM | MAX DC ⁽³⁾ | MAX ⁽²⁾ | UNIT |
|-----------------|---|-----------------------|---------------------|-----------------------|----------------------|---------------------|
| ddr3ch1_vref_ca | DDR3, DDR3L addr / ba / ncas / nras / nreset / nwe / odt channel 1 VREF output power supply to memory | 0.49 × vdds_ ddr_ch1 | 0.5 × vdds_ ddr_ch1 | | 0.51 × vdds_ ddr_ch1 | V |
| | Maximum noise (peak-peak) | −0.01 × vdds_ ddr_ch1 | | | 0.01 × vdds_ ddr_ch1 | mV _{PPmax} |
| ddr3ch2_vref_ca | DDR3, DDR3L addr / ba / ncas / nras / nreset / nwe / odt channel 2 VREF output power supply to memory | 0.49 × vdds_ ddr_ch2 | 0.5 × vdds_ ddr_ch2 | | 0.51 × vdds_ ddr_ch2 | V |
| | Maximum noise (peak-peak) | −0.01 × vdds_ ddr_ch2 | | | 0.01 × vdds_ ddr_ch2 | mV _{PPmax} |

- (1) Refer to Power on Hours table for limitations.
- (2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.
- (3) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power-On-Hours). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.
- (4) A pulse width of 1000 ns and an amplitude of 2 V is required to program each eFuse bit. Otherwise, VPP1 must not be supplied.
- (5) vddq_vref_ddrch1 must be supplied from the same regulator as vdds_ ddr_ch1. vddq_vref_ddrch2 must be supplied from the same regulator as vdds_ ddr_ch2.
- (6) The board temperature (T_B) and junction temperature (T_J) range is defined for 2S2P board types (reference JEDEC standard JESD51-9, *Test Board for Array Surface Mount Package Thermal Measurements*). The board temperature is measured at 1 mm from the package edge.

4.3 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each OPP (operating performance point) for processor clocks and device core clocks.

Table 4-4 describes the supported operating performance point (OPP) on MPU for the device.

Table 4-4. vdd_mpu Operating Points (1)

| Devices | OPP_NOM_MPU | OPP_HIGH_MPU |
|----------|-------------|--------------|
| OMAP5432 | √ | √ |

- (1) This table is specific to vdd_mpu with AVS feature enabled.

Table 4-5 describes the supported operating performance point (OPP) on MM for the devices.

Table 4-5. vdd_mm Operating Points (1)

| Devices | OPP_NOM_MM | OPP_OD_MM |
|----------|------------|-----------|
| OMAP5432 | √ | √ |

- (1) This table is specific to vdd_mm with AVS feature enabled.

Table 4-6 describes the supported operating performance point (OPP) on CORE for the devices.

Table 4-6. vdd_core Operating Points (1)

| Devices | OPP_NOM_CORE |
|----------|--------------|
| OMAP5432 | √ |

(1) This table is specific to vdd_mm with AVS feature enabled.

NOTE

All clocks frequencies mentioned in this document assume a system clock of 19.2MHz.

4.3.1 AVS and ABB Requirements

Adaptive Voltage Scaling (AVS) and Adaptive Body Biasing (ABB) are required on most of the VDD_* domains as defined in [Table 4-7](#)

Table 4-7. AVS and ABB Requirements per VDD_* Domain

| Domain | AVS Required? | ABB Required? |
|----------|-------------------|-------------------|
| VDD_CORE | Yes, for all OPPs | No |
| VDD_MPU | Yes, for all OPPs | Yes, for all OPPs |
| VDD_MM | Yes, for all OPPs | Yes, for all OPPs |

4.3.2 Micro Processor Unit (MPU)

[Table 4-8](#) shows the recommended voltages ranges for MPU voltage domain.

Table 4-8. MPU Voltage Domain

| DOMAIN | CONDITION | OPP_NOM_MPU | | | OPP_HIGH_MPU | | | | RETENTION |
|------------|----------------------------------|------------------------|-----------------|----------------------|------------------------|-----------------|---------------------|----------------------|-----------|
| | | MIN (2) | NOM (1) | MAX (2) | MIN (2) | NOM (1) | MAX DC (3) | MAX (2) | MIN (2) |
| VD_MPU (V) | BOOT (Before AVS is enabled) (4) | 1.014 | 1.05 | 1.11 | Not Applicable | | | | 0.65 |
| | After AVS is enabled (4) | AVS Voltage (5) – 3.5% | AVS Voltage (5) | AVS Voltage (5) + 5% | AVS Voltage (5) – 3.5% | AVS Voltage (5) | AVS Voltage (5) +2% | AVS Voltage (5) + 5% | |

(1) In a typical implementation, the power supply should target the NOM voltage.

(2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.

(3) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power-On-Hours). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.

(4) For all OPPs, AVS must be enabled to avoid impact on device reliability, lifetime POH (Power-On-Hours), and device power.

(5) The AVS Voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the CONTROL_STD_FUSE_OPP_VDD Registers in the Control Module Section of the TRM. The power supply should be adjustable over the following ranges for each required OPP:

- OPP_NOM_MPU: 0.85V - 1.10V
- OPP_HIGH_MPU: 0.85V - 1.25V

The AVS Voltages will be within the above specified ranges.

[Table 4-9](#) shows the recommended vdd_mpu voltages ranges (MPU voltage at ball level) with AVS disabled.

Table 4-9. MPU Clocks AC Performances(1)(2)

| Description | Source Clock | OPP_NOM_MPU | | OPP_HIGH_MPU | |
|---------------------------|---------------------------|-----------------|---------------------------------|-----------------|--------------------------|
| | | Max Freq. (MHz) | Ratio | Max Freq. (MHz) | Ratio |
| DPLL_MPU Locked Frequency | - | 2000 | - | 1500 | - |
| MPU_GCLK (CLKOUT_M2) | DPLL_MPU Locked Frequency | 1000 | 2 * (M2 = 1) (DCC disabled) (3) | 1500 | M2 = 1 (DCC enabled) (3) |

- (1) The DPLL ratios are configurable by software programming. For more information regarding the recommended DPLL ratios, including M2 above, see [Section 5.2.3](#).
- (2) The DPLL ratios documented in this table are recommended ratios. Other values may apply.
- (3) For more information on the Duty Cycle Correction feature, see the PRCM chapter of the Device TRM.

NOTE

The programmable divider for the asynchronous bridge to Audio Back-end (ABE) must be set to:

- MPU_GCLK / 16 when MPU_GCLK clock is running at OPP_HIGH_MPU.
- MPU_GCLK / 8 when MPU_GCLK clock is running at OPP_NOM_MPU.

The programmable divider for the asynchronous bridge to L3 must be set to:

- MPU_GCLK / 8 when MPU_GCLK clock is running at OPP_HIGH_MPU.
- MPU_GCLK / 4 when MPU_GCLK clock is running at OPP_NOM_MPU.

For more information on the programmable dividers for the asynchronous bridges, see the CM_MPU_MPU_CLKCTRL register, CLKSEL_ABE_DIV_MODE and CLKSEL_EMIF_DIV_MODE bits, in the Device TRM.

Please make sure to set the corresponding register bits (increasing the divider value) before increasing the MPU_GCLK clock frequency (by sequence to a higher OPP).

Please make sure to decrease the MPU_GCLK clock frequency (by sequence to a lower OPP) before setting the corresponding register bits (decreasing the divider value).

CAUTION

During MPU DVFS sequencing to a higher OPP, please make sure to increase the voltage prior to the clocks frequencies.

During MPU DVFS sequencing to a lower OPP, please make sure to decrease the clocks frequencies prior to the voltage.

Not respecting this MPU DVFS sequencing may lead to internal timing violations.

4.3.3 MultiMedia (MM) and 3D Graphic Accelerator (GPU)

4.3.3.1 MultiMedia (MM)

[Table 4-10](#) shows the recommended voltages ranges for MultiMedia voltage domain.

Table 4-10. MultiMedia Voltage Domain

| DOMAIN | CONDITION | OPP_NOM_MM | | | OPP_OD_MM | | | | RETENTION |
|------------|----------------------------------|------------------------|-----------------|----------------------|------------------------|-----------------|---------------------|----------------------|-----------|
| | | MIN (2) | NOM (1) | MAX (2) | MIN (2) | NOM (1) | MAX DC (3) | MAX (2) | MIN (2) |
| vdd_mm (V) | BOOT (Before AVS is enabled) (4) | 1.014 | 1.05 | 1.11 | Not Applicable | | | | 0.65 |
| | After AVS is enabled (4) | AVS Voltage (5) – 3.5% | AVS Voltage (5) | AVS Voltage (5) + 5% | AVS Voltage (5) – 3.5% | AVS Voltage (5) | AVS Voltage (5) +2% | AVS Voltage (5) + 5% | |

- (1) In a typical implementation, the power supply should target the NOM voltage.
- (2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.
- (3) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power-On-Hours). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.
- (4) For all OPPs, AVS must be enabled to avoid impact on device reliability, lifetime POH (Power-On-Hours), and device power.
- (5) The AVS Voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the CONTROL_STD_FUSE_OPP_VDD Registers in the Control Module Section of the TRM. The power supply should be adjustable over the following ranges for each required OPP:
 - OPP_NOM_MM: 0.85V - 1.10V
 - OPP_OD_MM: 0.85V - 1.15V
 The AVS Voltages will be within the above specified ranges.

Table 4-11 describes the standard processors clocks speed characteristics vs vdd_mm (MultiMedia voltage at ball level).

Table 4-11. MultiMedia Clocks AC Performances(1)(2)

| Description | Source Clock | OPP_NOM_MM | | OPP_OD_MM | |
|---------------------------|---------------------------|-----------------|---------|-----------------|---------|
| | | Max Freq. (MHz) | Ratio | Max Freq. (MHz) | Ratio |
| DPLL_IVA Locked Frequency | - | 2330 | - | 1062.4 | - |
| IVA_GCLK (CLKOUTX2_H12) | DPLL_IVA Locked Frequency | 388.3 | H12 = 6 | 531.2 | H12 = 2 |
| DSP_GCLK (CLKOUTX2_H11) | DPLL_IVA Locked Frequency | 466 | H11 = 5 | 531.2 | H11 = 2 |

- (1) The DPLL ratios are configurable by software programming. For more information regarding the recommended DPLL ratios, including H11, H12 above, see [Section 5.2.3](#).
- (2) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

4.3.3.2 3D Graphic Accelerator (GPU)

Table 4-12 shows the standard graphic accelerator (GPU) clocks speed characteristics vs vdd_mm (MultiMedia voltage at ball level).

Table 4-12. Graphic Accelerator (GPU) Clocks(1)(3)

| Description | Source Clock | OPP_NOM_MM | | OPP_OD_MM (2) | |
|---|----------------------------|-----------------|---------------|-----------------|-------------|
| | | Max Freq. (MHz) | Ratio | Max Freq. (MHz) | Ratio |
| Configuration 1 - From CORE DPLL – Locked Frequency @2127.36 MHz Maximum | | | | | |
| DPLL_CORE Locked Frequency | - | 2127.36 | - | 2127.36 | - |
| CORE_GPU_CLK (CLKOUTX2_H14) | DPLL_CORE Locked Frequency | 425.47 | H14 = 2.5 (4) | 531.84 | H14 = 2 (4) |
| GPU_CORE_GCLK | CORE_GPU_GCLK | 425.47 | 1 | 531.84 | 1 |
| Configuration 2 - From PER DPLL – Locked Frequency @768 MHz Maximum | | | | | |
| DPLL_PER Locked Frequency | - | 768 | - | | |
| PER_GPU_CLK (CLKOUTX2_H14) | DPLL_PER Locked Frequency | 384 | H14 = 2 | | |
| GPU_HYD_GCLK | PER_GPU_CLK | 384 | 1 | | |

- (1) The DPLL ratios are configurable by software programming. For more information regarding the recommended DPLL ratios, including H14 above, see [Section 5.2.3](#).
- (2) The DPLL CORE is in the CORE domain that supports up to OPP_NOM_CORE operating point compared to the 3D GPU graphic accelerator (GPU) which is in the MultiMedia (MM) domain which supports up to the OPP_OD_MM operating point. Hence, based on the CORE_GPU_CLK output clocks of DPLL_CORE, the 3D graphic accelerator clock (GPU_CORE_GCLK) can support up to OPP_HIGH_MM @600MHz based on the DPLL CORE in OPP_NOM_CORE operating point.
- (3) The DPLL ratios documented in this table are recommended ratios. Other values may apply.
- (4) For DPLL CORE, an additional division by 2 is performed after the HS divider.

CAUTION

During MM / GPU DVFS sequencing to a higher OPP, please make sure to increase the voltage prior to the clocks frequencies.

During MM / GPU DVFS sequencing to a lower OPP, please make sure to decrease the clocks frequencies prior to the voltage.

Not respecting this MM / GPU DVFS sequencing may lead to internal timing violations.

4.3.4 CORE

Table 4-13 shows the recommended voltages ranges for Core voltage domain.

Table 4-13. Core Voltage Domain

| DOMAIN | CONDITION | OPP_NOM | | | RETENTION |
|--------------|----------------------------------|------------------------|-----------------|----------------------|-----------|
| | | MIN (2) | NOM (1) | MAX (2) | MIN (2) |
| vdd_core (V) | BOOT (Before AVS is enabled) (3) | 1.014 | 1.05 | 1.11 | 0.81 |
| | After AVS is enabled (3) | AVS Voltage (4) – 3.5% | AVS Voltage (4) | AVS Voltage (4) + 5% | |

- (1) In a typical implementation, the power supply should target the NOM voltage.
- (2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.
- (3) For all OPPs, AVS must be enabled to avoid impact on device reliability, lifetime POH (Power-On-Hours), and device power.
- (4) The AVS Voltages are device-dependent, voltage domain-dependent, and OPP-dependent . They must be read from the CONTROL_STD_FUSE_OPP_VDD Registers in the Control Module Section of the TRM. The power supply should be adjustable over the following ranges for each required OPP:
 - OPP_NOM_CORE: 0.85V - 1.06V
 The AVS Voltages will be within the above specified ranges.

Table 4-14 shows the standard DPLL CORE clocks speed characteristics vs vdd_core (Core voltage at ball level).

Table 4-14. Core Clocks AC Performances – From DPLL CORE (1)(2)

| Description | Source Clock | OPP_NOM_CORE | |
|------------------------------|----------------------------|-----------------|--------------|
| | | Max Freq. (MHz) | Ratio |
| DPLL_CORE Locked Frequency | - | 2127.36 | - |
| CORE_DLL_GCLK (CLKOUTX2_H11) | DPLL_CORE Locked Frequency | 265.92 | H11 = 8 |
| CORE_X2_CLK (CLKOUTX2_H12) | DPLL_CORE Locked Frequency | 531.84 | H12 = 4 |
| L3MAIN2_L3_GICLK | CORE_X2_CLK | 265.92 | 2 |
| L3MAIN2_L4_GICLK | L3MAIN2_L3_GICLK | 132.96 | 2 |
| EMIF_PHY_GCLK (CLKOUT_M2) | DPLL_CORE Locked Frequency | 531.84 | 2 * (M2 = 2) |
| EMIF_FCLK (DDRPHY divider) | EMIF_PHY_GCLK | 265.92 | 2 |
| GPMC_CLK | L3MAIN2_L3_GICLK | 265.92 | 2 |

- (1) The DPLL ratios are configurable by software programming. For more information regarding the recommended DPLL ratios, including M2, H11, H12 above, see [Section 5.2.3](#).
- (2) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

4.3.5 OPP Dependencies

NOTE

The OPP dependencies apply only when both voltage domains are in ON state. That is:

- Any module in the domain may be powered, clocked and active
- SMPS is in active mode, delivering the voltage corresponding to current OPP

For more information on the Voltage Domain definitions, see the Power, Reset and Clock Management / Voltage Management Functional Description section in the Device TRM

[Table 4-15](#) shows the acceptable OPP dependencies between MPU, CORE and MultiMedia voltage domains.

Table 4-15. OPP Dependencies between MPU, CORE and MultiMedia

| vdd_mpu | vdd_core | vdd_mm |
|--------------|--------------|------------|
| OPP_NOM_MPU | OPP_NOM_CORE | OPP_NOM_MM |
| OPP_HIGH_MPU | OPP_NOM_CORE | OPP_NOM_MM |
| OPP_NOM_MPU | OPP_NOM_CORE | OPP_OD_MM |
| OPP_HIGH_MPU | OPP_NOM_CORE | OPP_OD_MM |

4.4 Electrical Characteristics

This section summarizes the dc electrical characteristics.

NOTE

The interfaces or signals described in this section correspond to the interfaces or signals available in multiplexing mode 0.

All interfaces or signals multiplexed on the balls described in this section have the same dc electrical characteristics, unless multiplexing involves a PHY/GPIO combination in which case different dc electrical characteristics are specified for the different multiplexing modes.

4.4.1 DDR3 and DDR3L DC Electrical Characteristics

Table 4-16 summarizes the DDR3 and DDR3L dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (i[2:0], sr[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the Device TRM.

Table 4-16. DDR3 and DDR3L DC Electrical Characteristics⁽³⁾

| PARAMETER | | MIN | NOM | MAX | UNIT | |
|---|--|--|-----|--|------|---|
| Signal Names in Mode 0 (Single-Ended Signals): ddrch1_dm[0-3], ddrch1_dq[0-31], ddr3ch1_a[0-9], ddr3ch1_a10_ap, ddr3ch1_a11, ddr3ch1_a12_nbc, ddr3ch1_a[13-15], ddr3ch1_cke[0-1], ddr3ch1_ncs[0-1], ddr3ch1_ba[0-2], ddr3ch1_ncas, ddr3ch1_nras, ddr3ch1_nreset, ddr3ch1_nwe, ddr3ch1_odt[0-1], ddrch2_dm[0-3], ddrch2_dq[0-31], ddrch2_dqs[0-3], ddrch2_ndqs[0-3], ddr3ch2_a[0-9], ddr3ch2_a10_ap, ddr3ch2_a11, ddr3ch2_a12_nbc, ddr3ch2_a[13-15], ddr3ch2_ck[a-b], ddr3ch2_cke[0-1], ddr3ch2_nck[a-b], ddr3ch2_ncs[0-1], ddr3ch2_ba[0-2], ddr3ch2_ncas, ddr3ch2_nras, ddr3ch2_nreset, ddr3ch2_nwe, ddr3ch2_odt[0-1] | | | | | | |
| Bottom Balls: A29 / B24 / C30 / B6 / C28 / A31 / C29 / B30 / B29 / C26 / B28 / B26 / C23 / C22 / C21 / B22 / C24 / C25 / B25 / A25 / E31 / E33 / E32 / F32 / C33 / D30 / F31 / C32 / C6 / A5 / B5 / C5 / B2 / B3 / C3 / D4 / A7 / B7 / C7 / B8 / C8 / B9 / C10 / B12 / C12 / A13 / B13 / C13 / B14 / C14 / A15 / B15 / C9 / A17 / B10 / B17 / C15 / B16 / C16 / C17 / B19 / C19 / B20 / C20 / B21 / J1 / AJ3 / G1 / AL4 / K3 / H2 / H3 / J3 / J2 / M3 / L2 / L1 / AK3 / AG1 / AH3 / AJ2 / AH2 / AL1 / AL3 / AK4 / G3 / D3 / C2 / C1 / D2 / F2 / G2 / F3 / AM3 / AL5 / AM4 / AN3 / AL7 / AL6 / AM7 / AM6 / AG2 / AG3 / F2 / AF3 / AE2 / AE3 / AC3 / AB2 / AB3 / AA2 / AA3 / Y2 / Y3 / W1 / W2 / W3 / AD2 / U3 / AD3 / T2 / V2 / V3 / U2 / T3 / R3 / P2 / P3 / N2 / M2 | | | | | | |
| Driver mode | | | | | | |
| V _{OH} | High-level output threshold (I _{OH} = 0.1 mA) | 0.9 × vddx_ddr3 ⁽¹⁾ | | vddx_ddr3 ⁽¹⁾ + 0.2 | V | |
| V _{OL} | Low-level output threshold (I _{OL} = 0.1 mA) | −0.2 | | 0.1 × vddx_ddr3 ⁽¹⁾ | V | |
| C _{PAD} | Pad capacitance (including package capacitance) | | | 3 | pF | |
| Z _O | Output impedance (drive strength) ⁽⁵⁾ | I[2:0] = 000 (Imp80) | 68 | 80 | 92 | Ω |
| | | I[2:0] = 001 (Imp60) | 51 | 60 | 69 | |
| | | I[2:0] = 010 (Imp48) | 41 | 48 | 55 | |
| | | I[2:0] = 011 (Imp40) | 34 | 40 | 46 | |
| | | I[2:0] = 100 (Imp34) | 29 | 34 | 39 | |
| Single-Ended Receiver mode | | | | | | |
| V _{IH} | High-level input threshold | vddy_vref_ddr3 ⁽²⁾ + 0.10 | | vddx_ddr3 ⁽¹⁾ + 0.2 | V | |
| V _{IL} | Low-level input threshold | −0.2 | | vddy_vref_ddr3 ⁽²⁾ − 0.10 | V | |
| V _{CM} | Input common-mode voltage | vddy_vref_ddr3 ⁽²⁾ − 0.1 × vddx_ddr3 ⁽¹⁾ | | vddy_vref_ddr3 ⁽²⁾ + 0.1 × vddx_ddr3 ⁽¹⁾ | V | |
| Z _I | Input impedance | odt[1:0] ⁽⁴⁾ = 00 | Off | Off | Off | Ω |
| | | odt[1:0] ⁽⁴⁾ = 01 | 48 | 60 | 72 | |
| | | odt[1:0] ⁽⁴⁾ = 10 | 64 | 80 | 96 | |
| | | odt[1:0] ⁽⁴⁾ = 11 | 78 | 120 | 162 | |
| C _{PAD} | Pad capacitance (including package capacitance) | | | 3 | pF | |

Table 4-16. DDR3 and DDR3L DC Electrical Characteristics⁽³⁾ (continued)

| PARAMETER | | MIN | NOM | MAX | UNIT | |
|---|--|--|--|---------------------------------------|--------------------------------------|---|
| Signal Names in Mode 0 (Differential Signals): ddrch1_dqs[0-3], ddrch1_ndqs[0-3], ddr3ch1_ck[a-b], ddr3ch1_nck[a-b], ddrch2_dqs[0-3], ddrch2_ndqs[0-3], ddr3ch2_ck[a-b], ddr3ch2_nck[a-b], | | | | | | |
| Bottom Balls: C27 / B23 / D31 / C4 / B27 / A23 / D32 / B4 / C11 / C18 / B11 / B18 / K2 / AK2 / E2 / AM5 / L3 / AL2 / E3 / AN5 / AC2 / R2 / AC1 / R1 | | | | | | |
| Driver mode | | | | | | |
| V _{OH} | High-level output threshold (I _{OH} = 0.1 mA) | 0.9 × vddx_dds3 ⁽¹⁾ | | | V | |
| V _{OL} | Low-level output threshold (I _{OL} = 0.1 mA) | | | 0.1 × vddx_dds3 ⁽¹⁾ | V | |
| C _{PAD} | Pad capacitance (including package capacitance) | | | 3 | pF | |
| Z _O | Output impedance (drive strength) ⁽⁵⁾ | I[2:0] = 000 (Imp80) | 68 | 80 | 92 | Ω |
| | | I[2:0] = 001 (Imp60) | 51 | 60 | 69 | |
| | | I[2:0] = 010 (Imp48) | 41 | 48 | 55 | |
| | | I[2:0] = 011 (Imp40) | 34 | 40 | 46 | |
| | | I[2:0] = 100 (Imp34) | 29 | 34 | 39 | |
| Single-Ended Receiver mode | | | | | | |
| V _{IH} | High-level input threshold | 0.5 × vddx_dds3 ⁽¹⁾ + 0.13 | | vddx_dds3 ⁽¹⁾ + 0.2 | V | |
| V _{IL} | Low-level input threshold | -0.2 | | 0.5 × vddx_dds3 ⁽¹⁾ - 0.13 | V | |
| Z _I | Input impedance | odt[1:0] ⁽⁴⁾ = 00 | OFF | OFF | OFF | Ω |
| | | odt[1:0] ⁽⁴⁾ = 01 | 48 | 60 | 72 | |
| | | odt[1:0] ⁽⁴⁾ = 10 | 64 | 80 | 96 | |
| | | odt[1:0] ⁽⁴⁾ = 11 | 78 | 120 | 162 | |
| C _{PAD} | Pad capacitance (including package capacitance) | | | 3 | pF | |
| Differential Receiver mode | | | | | | |
| V _{SWING} | Input voltage swing | 0.20 | | vddx_dds3 ⁽¹⁾ + 0.4 | V | |
| V _{CM} | Input common-mode voltage | 0.4 × vddx_dds3 ⁽¹⁾ | | 0.6 × vddx_dds3 ⁽¹⁾ | V | |
| Z _I | Input impedance | odt[1:0] ⁽⁴⁾ = 00 | OFF | OFF | OFF | Ω |
| | | odt[1:0] ⁽⁴⁾ = 01 | 48 | 60 | 72 | |
| | | odt[1:0] ⁽⁴⁾ = 10 | 64 | 80 | 96 | |
| | | odt[1:0] ⁽⁴⁾ = 11 | 78 | 120 | 162 | |
| C _{PAD} | Pad capacitance (including package capacitance) | | | 3 | pF | |
| Signal Names in Mode 0 (VREF Signals): ddrch1_vref_dq, ddrch2_vref_dq, ddr3ch1_vref_ca, ddr3ch2_vref_ca | | | | | | |
| Bottom Balls: A19 / U1 / A9 / AE1 | | | | | | |
| V _{REF} | Reference internal generation dc voltage level | vref_tap[1:0] = 00, 2-μA current load | 0.49 × vddq_vref_dds3 ⁽²⁾ | 0.50 × vddq_vref_dds3 ⁽²⁾ | 0.51 × vddq_vref_dds3 ⁽²⁾ | V |
| | | vref_tap[1:0] = 01, 4-μA current load | 0.49 × vddq_vref_dds3 ⁽²⁾ | 0.50 × vddq_vref_dds3 ⁽²⁾ | 0.51 × vddq_vref_dds3 ⁽²⁾ | |
| | | vref_tap[1:0] = 10, 8-μA current load | 0.49 × vddq_vref_dds3 ⁽²⁾ | 0.50 × vddq_vref_dds3 ⁽²⁾ | 0.51 × vddq_vref_dds3 ⁽²⁾ | |
| | | vref_tap[1:0] = 11, 32-μA current load | 0.49 × vddq_vref_dds3 ⁽²⁾ | 0.50 × vddq_vref_dds3 ⁽²⁾ | 0.51 × vddq_vref_dds3 ⁽²⁾ | |
| C _{CAP} | Decoupling capacitor | ccap[1:0] = 00 | No capacitor connected | | | |
| | | ccap[1:0] = 01 | Capacitor between Bias2 and V _{SS} | | | |
| | | ccap[1:0] = 10 | Capacitor between Bias2 and V _{DSS} | | | |
| | | ccap[1:0] = 11 | Capacitor between Bias2 and V _{SS} and capacitor between Bias2 and V _{DSS} | | | |

(1) vddx_dds3 can have the value vdds_dds_ch1, vdds_dds_ch2, vddq_vref_dds3, or vddq_vref_dds3 depending on the ball used. For more information on the power supply name and the corresponding ball, see Table 3-1, POWER NAME [9] column.

(2) vddq_vref_dds3 can have the value vddq_vref_dds3 or vddq_vref_dds3 depending on the ball used. For more information on the power supply name and the corresponding ball, see Table 3-1, POWER NAME [9] column.

(3) Output transition time or turn-on time is measured with the measurement setup (see Figure 4-1) with Z_O = 40 Ω and C_{LOAD} = 5 pF (lumped, no transmission line model).

- (4) The ODT register can configure the on-die termination impedance. For more information, see the Device TRM.
- (5) It is recommended to use 34 Ω and 40 Ω for actual use cases, for optimum performance.

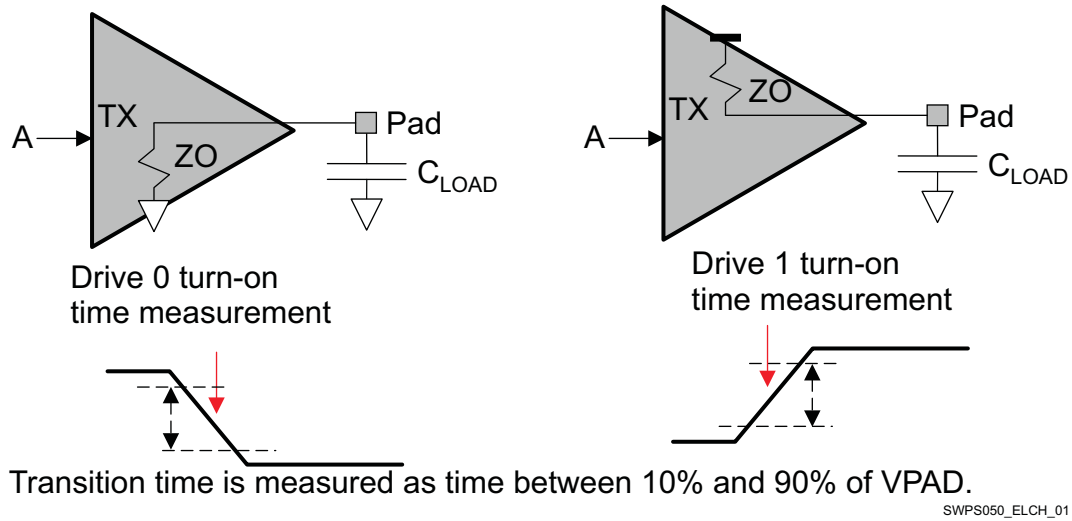


Figure 4-1. Output Transition Time Measurement

4.4.2 Camera DC Electrical Characteristics

4.4.2.1 CSI-2 MIPI D-PHY and CCPV2 DC Electrical Characteristics

Table 4-17 summarizes the CSI-2 MIPI D-PHY and CCPV2 dc electrical characteristics in multiplexing mode 0.

Table 4-17. CSI-2 MIPI D-PHY and CCPV2 RX DC Electrical Characteristics

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--|--|------------------------|-----|------------------------|------------------|
| Signal Names in Mode 0⁽¹¹⁾: csiporc_lane[1:0]x, csiporc_lane[1:0]y, csiporb_lane[2:0]x, csiporb_lane[2:0]y, csiporta_lane[4:0]x, csiporta_lane[4:0]y | | | | | |
| Bottom Balls: J2 / K2 / J3 / K3 / Y3 / W3 / V3 / Y2 / W2 / V2 / L2 / M2 / N2 / P2 / R2 / L3 / M3 / N3 / P3 / R3 | | | | | |
| MIPI D-PHY Mode Low-Power Receiver (LP-RX) | | | | | |
| V _{IH} | Input high-level voltage | 880 | | 1350 | mV |
| V _{IL} | Input low-level voltage | | | 550 | mV |
| V _{ITH} | Input high-level threshold ⁽¹⁾ | | | 880 | mV |
| V _{ITL} | Input low-level threshold ⁽²⁾ | 550 | | | mV |
| V _{HYS} | Input hysteresis ⁽³⁾ | 25 | | | mV |
| MIPI D-PHY Mode Ultralow Power Receiver (ULP-RX) | | | | | |
| V _{IH} | Input high-level voltage | 880 | | | mV |
| V _{IL} | Input low-level voltage | | | 300 | mV |
| V _{ITH} | Input high-level threshold ⁽¹⁾ | | | 880 | mV |
| V _{ITL} | Input low-level threshold ⁽⁴⁾ | 300 | | | mV |
| V _{HYS} | Input hysteresis ⁽³⁾ | 25 | | | mV |
| MIPI D-PHY Mode High-Speed Receiver (HS-RX) | | | | | |
| V _{IDTH} | Differential input high-level threshold | 70 | | | mV |
| V _{IDTL} | Differential input low-level threshold | | | -70 | mV |
| V _{IDMAX} | Maximum differential input voltage ⁽⁷⁾ | | | 270 | mV |
| V _{IHHS} | Single-ended input high voltage ⁽⁵⁾ | | | 460 | mV |
| V _{ILHS} | Single-ended input low voltage ⁽⁵⁾ | -40 | | | mV |
| V _{CMRXDC} | Differential input common-mode voltage ⁽⁵⁾⁽⁶⁾⁽⁸⁾ | 70 | | 330 | mV |
| Z _{ID} | Differential input impedance | 80 | 100 | 125 | Ω |
| CCP2 Mode (only on MIPI CSI-2 port B and MIPI CSI-2 port C) Signal Names: csiporc_lane[1:0]x, csiporc_lane[1:0]y, csiporb_lane[2:1]x, csiporb_lane[2:1]y | | | | | |
| Bottom Balls: J2 / K2 / J3 / K3 / Y3 / W3 / Y2 / W2 | | | | | |
| V _{CM} | Input common-mode voltage range ⁽⁸⁾ | 0.6 | 0.9 | 1.2 | V |
| V _{OS} | Receiver input dc offset | -20 | | 20 | mV |
| V _{ID} | Receiver input differential amplitude | 140 | 200 | 400 | mV _{PP} |
| ΔV _{ID} / V _{ID} | Amplitude mismatch between lane modules | -10% | | 10% | |
| ΔV _{CMRX} | Common-mode mismatch between lane modules | -100 | | 100 | mV |
| ΔV _{CMn} | Common-mode noise ripple ⁽⁹⁾ | -15 | | 15 | mV |
| Z _{ID} | Differential input impedance | 80 | 100 | 120 | Ω |
| GPI Mode⁽¹⁰⁾ Signal Names⁽¹¹⁾: csiporc_lane[1:0]x, csiporc_lane[1:0]y, csiporb_lane[2:0]x, csiporb_lane[2:0]y, csiporta_lane[4:0]x, csiporta_lane[4:0]y | | | | | |
| Bottom Balls: J2 / K2 / J3 / K3 / Y3 / W3 / V3 / Y2 / W2 / V2 / L2 / M2 / N2 / P2 / R2 / L3 / M3 / N3 / P3 / R3 | | | | | |
| V _{ITH} | Input high-level threshold | 0.65 × V _{DD} | | V _{DD} + 0.3 | V |
| V _{ITL} | Input low-level threshold | -0.3 | | 0.35 × V _{DD} | V |
| V _{HYS} | Input hysteresis voltage | 150 | | | mV |
| C _{IN} | Input capacitance | | | 1.3 | pF |
| t _{TIN} | Input transition time (t _R or t _F evaluated between 10% and 90% of V _{PAD}), minimum at minimum load and maximum at maximum load | | | 10 | ns |

- (1) V_{ITH} is the voltage at which the receiver is required to detect a high state in the input signal.
- (2) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. V_{ITL} is larger than the maximum single-ended line high voltage during HS transmission. Therefore, both low-power (LP) receivers will detect low during HS signaling.
- (3) To reduce noise sensitivity on the received signal, the LP receiver is required to incorporate a hysteresis, V_{HYST} . V_{HYST} is the difference between the V_{ITH} threshold and the V_{ITL} threshold.
- (4) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. Specification is relaxed for detecting 0 during ultralow power (ULP) state. The LP receiver is not required to detect HS single-ended voltage as 0 in this state.
- (5) Excluding possible additional RF interference of 200 mV_{PP} beyond 450 MHz.
- (6) This value includes a ground difference of 50 mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450 MHz.
- (7) This number corresponds to the V_{ODMAX} transmitter.
- (8) Common mode is defined as the average voltage level of X and Y: $V_{CMRX} = (V_X + V_Y) / 2$.
- (9) Common mode ripple may be due to t_R or t_F and transmission line impairments in the PCB.
- (10) The GPI mode is only available through multiplexing modes 3, 4, and 6. For more information, see [Table 3-1](#). The GPI mode is only supported in 1.8-V mode.
- (11) For more information regarding the pin name (or ball name) and corresponding signal name, see [Table 3-6](#), *CSI-2 MIPI D-PHY Signal Descriptions*, or [Table 3-7](#), *CCP2 PHY Signal Descriptions*.

4.4.3 Display DC Electrical Characteristics

4.4.3.1 HDMI DC Electrical Characteristics

NOTE

For more information on HDMI, please contact your TI representative.

4.4.3.2 DSI-1 MIPI D-PHY (DSI1_A and DSI1_C) DC Electrical Characteristics

[Table 4-18](#) summarizes the DSI-1 MIPI D-PHY dc electrical characteristics in multiplexing mode 0.

Table 4-18. DSI-1 MIPI D-PHY (DSI1_A and DSI1_C) TX DC Electrical Characteristics

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--|--|----------------------|-----|-------------------------|-----------------------|
| Signal Names in Mode 0: dsiporta_lane[4:0]x, dsiporta_lane[4:0]y, dsiportc_lane[4:0]x, dsiportc_lane[4:0]y | | | | | |
| Bottom Balls: R32 / T32 / V32 / W32 / Y32 / R31 / T31 / V31 / W31 / Y31 / AB32 / AC32 / AD32 / AE32 / AF32 / AB31 / AC31 / AD31 / AE31 / AF31 | | | | | |
| MIPI D-PHY Mode High-Speed Transmitter (HS-TX) | | | | | |
| V_{CMTX} | HS transmit static common-mode voltage ⁽¹⁾⁽²⁾ | 150 | 200 | 250 | mV |
| $ \Delta V_{CMTX(1,0)} $ | V_{CMTX} mismatch when output is Differential-1 or Differential-0 | | | 5 | mV |
| $ V_{OD} $ | HS transmit differential output voltage ⁽¹⁾⁽³⁾ | 140 | 200 | 270 | mV |
| $ \Delta V_{OD} $ | V_{OD} mismatch when output is Differential-1 or Differential-0 | | | 14 | mV |
| V_{OHHS} | HS output high voltage ⁽¹⁾ | | | 360 | mV |
| Z_{OS} | Single-ended output impedance | 40 | 50 | 62.5 | Ω |
| ΔZ_{OS} | Single-ended output impedance mismatch | | | 10% | |
| $\Delta V_{CMTX(HF)}$ | Common-level variation above 450 MHz | | | 15 | mV _{RMS} |
| $\Delta V_{CMTX(LF)}$ | Common-level variation between 50 MHz and 450 MHz | -50 | | 50 | mV _{PEAK} |
| t_{TOUT} | Output transition time (t_R or t_F evaluated between 20% and 80% of V_{PAD}) | 0.10 ⁽¹¹⁾ | | | ns |
| | | | | 0.3 ⁽⁸⁾⁽⁹⁾ | U _{INST,MIN} |
| | | | | 0.35 ⁽⁸⁾⁽¹⁰⁾ | |
| MIPI D-PHY Mode Low-Power Transmitter (LP-TX) | | | | | |
| V_{OL} | Thevenin output low level | -50 | | 50 | mV |
| V_{OH} | Thevenin output high level | 1.1 | 1.2 | 1.3 | V |
| Z_{OLP} | Output impedance of LP transmitter | 110 | | | Ω |
| t_{TOUT} | Output transition time (t_R or t_F evaluated between 20% and 80% of V_{PAD}) | | | 25 | ns |

Table 4-18. DSI-1 MIPI D-PHY (DSI1_A and DSI1_C) TX DC Electrical Characteristics (continued)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--|---|-----|-----|------|------|
| MIPI D-PHY Mode Low-Power Receiver (LP-RX) | | | | | |
| V _{IH} | Input high-level voltage | 880 | | 1350 | mV |
| V _{IL} | Input low-level voltage | | | 550 | mV |
| V _{ITH} | Input high-level threshold ⁽⁴⁾ | | | 880 | mV |
| V _{ITL} | Input low-level threshold ⁽⁵⁾ | 550 | | | mV |
| V _{HYS} | Input hysteresis ⁽⁶⁾ | 25 | | | mV |
| MIPI D-PHY Mode Ultralow Power Receiver (ULP-RX) | | | | | |
| V _{IH} | Input high-level voltage | 880 | | | mV |
| V _{IL} | Input low-level voltage | | | 300 | mV |
| V _{ITH} | Input high-level threshold ⁽⁴⁾ | | | 880 | mV |
| V _{ITL} | Input low-level threshold ⁽⁷⁾ | 300 | | | mV |
| V _{HYS} | Input hysteresis ⁽⁶⁾ | 25 | | | mV |
| MIPI D-PHY mode Low-Power Contention Detector (LP-CD) | | | | | |
| V _{IHCD} | Input high-level contention voltage | 450 | | | mV |
| V _{ILCD} | Input low-level contention voltage | | | 200 | mV |

(1) Value when driving into a differential load impedance anywhere in the range of 80 to 125 Ω.

(2) Common mode is defined as the average voltage level of X and Y: $V_{CMTX} = (V_X + V_Y) / 2$.

(3) $V_{OD} = V_X - V_Y$

(4) V_{ITH} is the voltage at which the receiver is required to detect a high state in the input signal.

(5) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. V_{ITL} is larger than the maximum single-ended line high voltage during HS transmission. Therefore, both LP receivers will detect low during HS signaling.

(6) To reduce noise sensitivity on the received signal, the LP receiver is required to incorporate a hysteresis, V_{HYST}. V_{HYST} is the difference between the V_{ITH} threshold and the V_{ITL} threshold.

(7) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. Specification is relaxed for detecting 0 during ultralow power (ULP) state. The LP receiver is not required to detect HS single-ended voltage as 0 in this state.

(8) $U_{INST,MIN} = 1/(2 \times f_{max})$, where f_{max} is the highest fundamental frequency of the HS data transmission.

(9) Applicable when operating at HS bit rates = 1 Gbps (UI = 1 ns).

(10) Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).

(11) Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates = 1 Gbps (UI = 1 ns) must not use values below 0.15 ns.

4.4.4 I²C DC Electrical Characteristics

Table 4-19 summarizes the I²C dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (LB0[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the Device TRM.

Table 4-19. I²C DC Electrical Characteristics

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|----------------------------|-----|----------------------------|------|
| Signal Names in Mode 0: i2c[5:2]_scl, i2c[5:2]_sda, i2c1_pmic_scl, i2c1_pmic_sda, sr_pmic_scl, sr_pmic_sda | | | | | |
| Bottom Balls: AL32 / AK22 / AB3 / AF30 / AL31 / AJ20 / AB2 / AF29 / K29 / H30 / H29 / J29 | | | | | |
| I²C Standard Mode—1.2 V and 1.8 V⁽³⁾ | | | | | |
| V _{IH} ⁽⁵⁾ | Input high-level threshold | 0.7 × vddsx ⁽¹⁾ | | vddsx ⁽¹⁾ + 0.5 | V |
| V _{IL} ⁽⁵⁾ | Input low-level threshold | −0.5 | | 0.3 × vddsx ⁽¹⁾ | V |
| I _i | Input current at each IO pin with an input voltage between 0.1 × vdd to 0.9 × vdd | −10 | | 10 | μA |
| C _i | Input capacitance | | | 10 | pF |

Table 4-19. I²C DC Electrical Characteristics (continued)

| PARAMETER | | MIN | NOM | MAX | UNIT | |
|--|---|---|------|--|------|----|
| V _{OL3} | Output low-level threshold open-drain at 3-mA sink current | NA ⁽²⁾ | | NA ⁽²⁾ | V | |
| t _{OF} | Output fall time from V _{IHmin} to V _{ILmax} with a bus capacitance C _B from 5 pF to 400 pF | | | 250 | ns | |
| t _{OR} | Output rise time from V _{ILmax} to V _{IHmin} with a capacitive load from 5 pF to 150 pF with internal pullup resistor enabled | 20 + 0.1 × C _B | | 250 | ns | |
| I²C Fast Mode—1.2 V and 1.8 V | | | | | | |
| V _{IH} ⁽⁵⁾ | Input high-level threshold | 0.7 × v _{ddsx} ⁽¹⁾ | | v _{ddsx} ⁽¹⁾ + 0.5 | V | |
| V _{IL} ⁽⁵⁾ | Input low-level threshold | –0.5 | | 0.3 × v _{ddsx} ⁽¹⁾ | V | |
| I _I | Input current at each IO pin with an input voltage between 0.1 × v _{dd} to 0.9 × v _{dd} | –10 | | 10 | μA | |
| C _I | Input capacitance | | | 10 | pF | |
| V _{OL3} | Output low-level threshold open-drain at 3-mA sink current | 0 | | 0.2 × v _{ddsx} ⁽¹⁾ | V | |
| t _{OF} | Output fall time from V _{IHmin} to V _{ILmax} with a bus capacitance C _B from 5 pF to 400 pF | 20 + 0.1 × C _B | | 250 | ns | |
| t _{OR} | Output rise time from V _{ILmax} to V _{IHmin} with a capacitive load from 5 pF to 150 pF with internal pullup resistor enabled | 20 + 0.1 × C _B | | 250 | ns | |
| R _{INPU} | Internal I ² C pullup resistance for a given load range | LB[1:0] = 00 | 3 | 4 (5 to 15 pF) | 6 | kΩ |
| | | LB[1:0] = 01 | 1.6 | 2.1 (15 to 50 pF) | 3.17 | |
| | | LB[1:0] = 10 | 0.64 | 0.84 (50 to 150 pF) | 1.27 | |
| | | LB[1:0] = 11 | | NA | | |
| I²C High-Speed Mode—1.2 V and 1.8 V | | | | | | |
| V _{IH} ⁽⁵⁾ | Input high-level threshold | 0.7 × v _{ddsx} ⁽¹⁾ | | v _{ddsx} ⁽¹⁾ + 0.5 | V | |
| V _{IL} ⁽⁵⁾ | Input low-level threshold | –0.5 | | 0.3 × v _{ddsx} ⁽¹⁾ | V | |
| I _I | Input current at each IO pin with an input voltage between 0.1 × v _{dd} to 0.9 × v _{dd} | –10 | | 10 | μA | |
| C _I | Input capacitance | | | 10 | pF | |
| V _{OL3} | Output low-level threshold open-drain at 3-mA sink current | 0 | | 0.2 × v _{ddsx} ⁽¹⁾ | V | |
| t _{OF} | Output fall time from V _{IHmin} to V _{ILmax} with a capacitive load from 5 pF to 100 pF at 3-mA sink current | 10 | | 40 | ns | |
| | Output fall time from V _{IHmin} to V _{ILmax} with a capacitive load of 400 pF at 3-mA sink current | 20 | | 80 | ns | |
| t _{OR} | Output rise time from V _{ILmax} to V _{IHmin} with a capacitive load from 5 pF to 80 pF with internal pullup resistor enabled | 10 | | 40 | ns | |
| R _{INPU} | Internal I ² C pullup resistance for a given load range | LB[1:0] = 00 | 1.37 | 1.8 (5 to 12 pF) | 2.72 | kΩ |
| | | LB[1:0] = 01 | 0.76 | 1.0 (12 to 25 pF) | 1.51 | |
| | | LB[1:0] = 10 | 0.4 | 0.525 (25 to 50 pF) | 0.79 | |
| | | LB[1:0] = 11 | 0.23 | 0.3 (50 to 80 pF) | 0.45 | |
| Non-I²C Mode (Normal Mode)⁽⁴⁾ | | | | | | |
| 1.2-V Mode | | | | | | |
| V _{IH} ⁽⁵⁾ | Input high-level threshold | 0.7 × v _{ddsx} ⁽¹⁾ | | v _{ddsx} ⁽¹⁾ + 0.5 | V | |
| V _{IL} ⁽⁵⁾ | Input low-level threshold | –0.5 | | 0.3 × V _{DD} | V | |
| V _{HYS} | Input hysteresis voltage | 50 | | | mV | |
| I _I | Input current at each IO pin with an input voltage between 0.1 × v _{dd} to 0.9 × v _{dd} | –10 | | 10 | μA | |
| C _I | Input capacitance | | | 10 | pF | |
| V _{OH} | Output high-level threshold (I _{OH} = 4 mA) | 0.75 × v _{ddsx} ⁽¹⁾ | | | V | |

Table 4-19. I²C DC Electrical Characteristics (continued)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--------------------------------|--|----------------------------|-----|-----------------------------|------|
| V _{OL} | Output low-level threshold (I _{OL} = 4 mA) | | | 0.25 × vddsx ⁽¹⁾ | V |
| t _{OT} | Output transition time (t _R or t _F) at 40-pF load, evaluated between 10% to 90% V _{PAD} | | | 10 | ns |
| 1.8-V Mode | | | | | |
| V _{IH} ⁽⁵⁾ | Input high-level threshold | 0.7 × vddsx ⁽¹⁾ | | vddsx ⁽¹⁾ + 0.5 | V |
| V _{IL} ⁽⁵⁾ | Input low-level threshold | −0.5 | | 0.3 × vddsx ⁽¹⁾ | V |
| V _{HYS} | Input hysteresis voltage | 130 | | | mV |
| I _I | Input current at each IO pin with an input voltage between 0.1 × vdd to 0.9 × vdd | −10 | | 10 | μA |
| C _I | Input capacitance | | | 10 | pF |
| V _{OH} | Output high-level threshold (I _{OH} = 4 mA) | vddsx ⁽¹⁾ −0.45 | | | |
| V _{OL} | Output low-level threshold (I _{OL} = 4 mA) | | | 0.45 | V |
| t _{OT} | Output transition time (t _R or t _F) at 40-pF load, evaluated between 10% to 90% of V _{PAD} | | | 6 | ns |

(1) Depending on the I²C ball, vddsx can have the value: vdds_bank8, vdds_bank10, vdds_bank16, vdds_bank18, vdds_bank26, or vdds_hdmi. For more information, see [Table 3-1](#), POWER NAME [9] column.

(2) V_{OL} specification is not applicable in the standard mode.

(3) The pullup versus load settings of I²C fast mode also apply to I²C standard mode.

(4) This mode is only available through multiplexing modes 2 through 6. For more information, see or . In the normal mode (non-I²C mode), the pullup or pulldown nominal strength is 100 μA.

(5) Input voltage level could be in an undefined state (between V_{IL} and V_{IH}) for a maximum of 1 second without causing any damage.

4.4.5 USB DC Electrical Characteristics

NOTE

The following interfaces are not available in the device:

- USB (Port D0) – ULPI 8-bit
- USB (Port B1) – HSIC1
- USB (Port B2) – ULPI 8-bit
- USB (Port B2) – Full Speed / Low Speed

For more information, see the Device TRM.

4.4.5.1 USB2 PHY DC Electrical Characteristics

[Table 4-20](#) summarizes the USB2 PHY dc electrical characteristics in multiplexing mode 0.

Table 4-20. USB2 PHY DC Electrical Characteristics

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|-----|-----|-----|------|
| Signal Names in Mode 0: usbd0_hs_dp, usbd0_hs_dm | | | | | |
| Bottom Balls: AM20 / AL20 | | | | | |
| USB2 PHY in USB LS / FS Single-Ended Receiver | | | | | |
| V _{IH} | Input high-level threshold | 2 | | | V |
| V _{IL} | Input low-level threshold | | | 0.8 | V |
| Z _{INP} | Input impedance exclusive of a pullup or pulldown resistor (pullup and pulldown resistors are disabled, DP and DM are in Hi-Z state). | 300 | | | kΩ |
| USB2 PHY in USB GPI LS / FS Receiver⁽¹⁾ | | | | | |
| V _{IH} | Input high-level threshold | 2 | | | V |
| V _{IL} | Input low-level threshold | | | 0.8 | V |
| USB2 PHY in USB LS / FS Differential Receiver | | | | | |
| V _{CM} | Differential common-mode range ⁽²⁾ | 0.8 | | 2.5 | V |

Table 4-20. USB2 PHY DC Electrical Characteristics (continued)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|-------|------|------|------|
| V _{DI} | Differential Input sensitivity | 0.2 | | | V |
| V _{HYS} | Differential receiver hysteresis | 0 | | 0 | mV |
| USB2 PHY in USB HS Differential Receiver | | | | | |
| V _{HSSQ} | HS squelch detection threshold (differential signal amplitude) | 100 | 125 | 150 | mV |
| V _{HSDISC} | HS disconnect detection threshold (differential signal amplitude) | 525 | 600 | 625 | mV |
| V _{HSCM} | HS data signaling common mode voltage range ⁽²⁾ | -50 | 200 | 500 | mV |
| Z _{HSDRCV} | Input impedance in HS receive mode (or termination impedance) | 40.5 | | 49.5 | Ω |
| USB2 PHY in USB LS / FS Differential Transmitter | | | | | |
| V _{OH} | Output high-level threshold (pulldown R = 15 kΩ on both DP and DM) | 2.8 | 3.3 | 3.6 | V |
| V _{OL} | Output low-level threshold (pullup R = 1.5 kΩ at 3.6 V on both DP and DM) | 0 | 0.1 | 0.3 | V |
| V _{CRS} | Output signal crossover voltage (pulldown R = 15 kΩ on both DP and DM, pullup R = 1.5 kΩ at 3.6 V on DM only) | 1.3 | | 2 | Ω |
| Z _{DRV} | Driver output resistance | 28 | 45 | 49.5 | Ω |
| t _{LSOT} | Output transition time (t _R or t _F), evaluated between 10% to 90% of V _{PAD} , C _L = [200 to 600] pF on both DP and DM, pullup R = 1.5 kΩ at 3.6 V for DM only | 75 | | 300 | ns |
| t _{FSOT} | Output transition time (t _R or t _F), evaluated between 10% to 90% of V _{PAD} , C _L = 50 pF on both DP and DM | 4 | | 20 | ns |
| USB2 PHY in GPO LS / FS Driver⁽¹⁾ | | | | | |
| V _{OH} | Output high-level threshold (I _{OH} = 4 mA) | 2.8 | 3.3 | 3.6 | V |
| V _{OL} | Output low-level threshold (I _{OL} = 4 mA) | 0 | 0.1 | 0.4 | V |
| USB2 PHY in USB HS Differential Transmitter | | | | | |
| V _{HDOI} | HS output idle level | -10.0 | 0.0 | 10.0 | mV |
| V _{HDOH} | HS output data signaling high | 360 | 400 | 440 | mV |
| V _{HDOH} | HS output data signaling low | -10.0 | 0.0 | 10.0 | mV |
| V _{CHIRPJ} | Chirp J level | 700 | 900 | 1100 | mV |
| V _{CHIRPK} | Chirp K level | -900 | -700 | -500 | mV |
| t _{OT} | Output transition time (t _R or t _F) evaluated between 10% to 90% of V _{PAD} | 500 | | | ps |
| Z _{HSDRV} | Driver output resistance | 40.5 | 45 | 49.5 | Ω |
| Signal Name: usbphy_ce | | | | | |
| Bottom Ball: AL19 | | | | | |
| USB2 PHY in USB LS / FS Differential Transmitter | | | | | |
| V _{OH} | Output high-level threshold (pulldown R = 15 kΩ on both DP and DM) | 2.8 | 3.3 | 3.6 | V |
| V _{OL} | Output low-level threshold (pullup R = 1.5 kΩ at 3.6 V on both DP and DM) | 0 | 0.1 | 0.3 | V |
| V _{CRS} | Output signal crossover voltage (pulldown R = 15 kΩ on both DP and DM, pullup R = 1.5 kΩ at 3.6 V on DM only) | 1.3 | | 2 | Ω |
| Z _{DRV} | Driver output resistance | 28 | 45 | 49.5 | Ω |
| t _{LSOT} | Output transition time (t _R or t _F), evaluated between 10% to 90% of V _{PAD} , C _L = [200 to 600] pF on both DP and DM, pullup R = 1.5 kΩ at 3.6 V for DM only | 75 | | 300 | ns |
| t _{FSOT} | Output transition time (t _R or t _F), evaluated between 10% to 90% of V _{PAD} , C _L = 50 pF on both DP and DM | 4 | | 20 | ns |
| USB2 PHY in GPO LS / FS Driver⁽¹⁾ | | | | | |
| V _{OH} | Output high-level threshold (I _{OH} = 4 mA) | 2.8 | 3.3 | 3.6 | V |
| V _{OL} | Output low-level threshold (I _{OL} = 4 mA) | 0 | 0.1 | 0.4 | V |
| USB2 PHY in USB HS Differential Transmitter | | | | | |
| V _{HDOI} | HS output idle level | -10.0 | 0.0 | 10.0 | mV |
| V _{HDOH} | HS output data signaling high | 360 | 400 | 440 | mV |
| V _{HDOH} | HS output data signaling low | -10.0 | 0.0 | 10.0 | mV |
| V _{CHIRPJ} | Chirp J level | 700 | 900 | 1100 | mV |

Table 4-20. USB2 PHY DC Electrical Characteristics (continued)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---------------------|---|------|------|------|------|
| V _{CHIRPK} | Chirp K level | –900 | –700 | –500 | mV |
| t _{OT} | Output transition time (t _R or t _F) evaluated between 10% to 90% of V _{PAD} | 500 | | | ps |
| Z _{HSDRV} | Driver output resistance | 40.5 | 45 | 49.5 | Ω |

(1) The GPIO modes are only available through multiplexing mode 4. For more information, see or .

(2) Common mode is defined as the average voltage level of DP and DM: $V_{CM} = (V_{DP} + V_{DM}) / 2$.

4.4.5.2 USB HSIC DC Electrical Characteristics

Table 4-21 summarizes the USB HSIC dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (i[2:0], sr[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the Device TRM.

Table 4-21. USB HSIC DC Electrical Characteristics

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--|--|---|-------|---|------|
| Signal Names in Mode 0 (Single-Ended Signals): usbb1_hsic_strobe, usbb1_hsic_data, usbb2_hsic_strobe, usbb2_hsic_data, usbb3_hsic_strobe, usbb3_hsic_data | | | | | |
| Top Balls: B26 / C26 / B25 / C25 / D29 / D30 | | | | | |
| Driver Mode | | | | | |
| V _{OH} | High-level output threshold (I _{OH} = 0.1 mA) | 0.9 x vdds_hsic | | | V |
| V _{OL} | Low-level output threshold (I _{OL} = 0.1 mA) | | | 0.1 x vdds_hsic | V |
| C _{PAD} | Pad capacitance | | | 3 | pF |
| Z _O | Output impedance (drive strength) | | | | Ω |
| | | I[2:0] = 000 (Imp80) | 80 | | |
| | | I[2:0] = 001 (Imp60) | 60 | | |
| | | I[2:0] = 010 (Imp48) | 48 | | |
| | | I[2:0] = 011 (Imp40) | 40 | | |
| | | I[2:0] = 100 (Imp34) | 34 | | |
| t _{OT} | Output transition time (t _R or t _F evaluated between 10% and 90% of V _{PAD}) for drive strength = 40 Ω and C _{LOAD} = 5 pF ⁽²⁾ | | | | ns |
| | | sr[2:0] = 000 (Fastest) | 0.162 | 0.325 | |
| | | sr[2:0] = 001 (Faster) | 0.162 | 0.33 | |
| | | sr[2:0] = 010 (Fast) | 0.162 | 0.34 | |
| | | sr[2:0] = 011 (Slow) | 0.168 | 0.35 | |
| | | sr[2:0] = 100 (Slower) | 0.168 | 0.35 | |
| | | sr[2:0] = 101 (Slowest-1) | 0.168 | 0.36 | |
| | | sr[2:0] = 110 (Slowest-2) | 0.168 | 0.36 | |
| | | sr[2:0] = 111 (Slowest-3) | 0.175 | 0.36 | |
| Single-Ended Receiver Mode | | | | | |
| V _{IH} | High-level input threshold | vddy_vref_lpddr2 ⁽¹⁾ + 0.13 | | vdds_hsic + 0.2 | V |
| V _{IL} | Low-level input threshold | –0.2 | | vddy_vref_lpddr2 ⁽¹⁾ – 0.13 | V |
| V _{CM} | Input common-mode voltage | vddy_vref_lpddr2 ⁽¹⁾ – 0.1 x vdds_hsic | | vddy_vref_lpddr2 ⁽¹⁾ + 0.1 x vdds_hsic | V |

- (1) vddy_vref_lpddr2 can have the value vddca_vref_lpddr2ch1, vddca_vref_lpddr2ch2, vddq_vref_ddrch1, or vddq_vref_ddrch2 depending on the ball used. For more information of the power supply name and the corresponding pin, ball, see [Table 3-1, POWER NAME \[9\]](#) column.
- (2) Output transition time/turn on time is measured with the measurement setup (see [Figure 4-1](#)) with $Z_O = 40 \Omega$ and $C_{LOAD} = 5 \text{ pF}$ (lumped, no transmission line model).

4.4.5.3

NOTE

The USB3 RX PHY module is compliant with the receiver electrical parameters specified in the *Universal Serial Bus 3.0 Specification*, Revision 1.0, November 12, 2008.

NOTE

The USB3 TX PHY module is compliant with the transmitter electrical parameters and LFPS electrical parameters specified in the *Universal Serial Bus 3.0 Specification*, Revision 1.0, November 12, 2008.

NOTE

For more information regarding the USB3 pin name (or ball name) and corresponding signal name, see [Table 3-22, USB Signal Descriptions](#).

4.4.6 SD Card DC Electrical Characteristics

[Table 4-22](#) summarizes the SD Card dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (IC[1:0], UHS104 or UHS50 modes) see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the Device TRM.

Table 4-22. SD Card DC Electrical Characteristics

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|--------------------------------|-----|------|----------|
| Signal Names in Mode 0: sdc card_clk, sdc card_cmd, sdc card_data[3:0] | | | | | |
| Bottom Balls: E3 / E2 / F3 / F2 / G2 / G3 | | | | | |
| 1.8-V Mode | | | | | |
| $V_{IH}^{(3)}$ | Input high-level threshold | 1.27 | | | V |
| $V_{IL}^{(3)}$ | Input low-level threshold | | | 0.58 | V |
| V_{HYS} | Input hysteresis voltage ⁽¹⁾ | 50 | | | mV |
| C_{PAD} | Pad capacitance (including package capacitance) | | | 5 | pF |
| V_{OH} | Output high-level threshold ($I_{OH} = 2 \text{ mA}$) | 1.4 | | | V |
| V_{OL} | Output low-level threshold ($I_{OL} = 2 \text{ mA}$) | | | 0.45 | V |
| Z_O | Output impedance (drive strength) | IC[1:0] = 00 (driver type B) | | 44 | Ω |
| | | IC[1:0] = 01 (driver type A) | | 33 | |
| | | IC[1:0] = 10 (driver type C) | | 58 | |
| | | IC[1:0] = 11 (driver type D) | | 100 | |
| t_{OT} | Output transition time (t_R or t_F evaluated between V_{OL} and V_{OH}) for driver type B | UHS104 mode (104 MB/s maximum) | 0.4 | 1.32 | ns |
| | | UHS50 mode (50 MB/s maximum) | 0.7 | 2.75 | |

Table 4-22. SD Card DC Electrical Characteristics (continued)

| PARAMETER | | MIN | NOM | MAX | UNIT | |
|---|--|--------------------------------------|--------------------------------|---------------------|------|----|
| C _{LOAD} | Load capacitance (at which the t _{OT} are measured) | IC[1:0] = 00 (driver type B) | UHS104 mode (104 MB/s maximum) | | 15 | pF |
| | | | UHS50 mode (50 MB/s maximum) | | 30 | |
| | | IC[1:0] = 01 (driver type A) | UHS104 mode (104 MB/s maximum) | | 21 | |
| | | | UHS50 mode (50 MB/s maximum) | | 43 | |
| | | IC[1:0] = 10 (driver type C) | UHS104 mode (104 MB/s maximum) | | 11 | |
| | | | UHS50 mode (50 MB/s maximum) | | 23 | |
| IC[1:0] = 11 (driver type D) ⁽²⁾ | UHS104 mode (104 MB/s maximum) | | - | | | |
| | UHS50 mode (50 MB/s maximum) | | - | | | |
| R _{RF} | t _R / t _F ratio | 0.7 | 1.00 | 1.4 | - | |
| 3.3-V Mode | | | | | | |
| V _{IH} ⁽³⁾ | Input high-level threshold | 0.625 × vdds_sdcard | | | V | |
| V _{IL} ⁽³⁾ | Input low-level threshold | | | 0.25 × vdds_sdcard | V | |
| V _{HYS} | Input hysteresis voltage | 40 | | | mV | |
| C _{PAD} | Pad capacitance (including package capacitance) | | | 5 | pF | |
| V _{OH} | Output high-level threshold (I _{OH} = 2 mA) | 0.75 × vdds_sdcard | | | V | |
| V _{OL} | Output low-level threshold (I _{OL} = 2 mA) | | | 0.125 × vdds_sdcard | V | |
| Z _O | Output impedance (drive strength) | IC[1:0] = 01 (driver type A) | | 33 | Ω | |
| | | IC[1:0] = 10 (driver type C) | | 58 | | |
| t _{OT} | Output transition time (t _R or t _F evaluated between V _{IHmin} and V _{ILmax}) | HS mode (25 MB/s maximum) | | 3 | ns | |
| | | Default speed mode (12 MB/s maximum) | | 10 | | |
| C _{LOAD} | Load capacitance (at which the t _{OT} are measured) | HS mode (25 MB/s maximum) | | 40 | pF | |
| | | Default speed mode (12 MB/s maximum) | | 40 | | |

(1) The hysteresis of the input buffer is programmable with the hyst_en register bit. For more information, see the Device TRM.

(2) The load capacitance specification does not exist for driver type D. It will be the maximum load that the host can support.

(3) Input voltage level could be in an undefined state (between V_{IL} and V_{IH}) for a maximum of 1 second without causing any damage.

4.4.7 SATA PHY DC Electrical Characteristics

NOTE

The SATA RX PHY module is compliant with the electrical specifications of SATA up to Gen2m.

NOTE

The SATA TX PHY module is compliant with the electrical specifications of SATA up to Gen2m.

NOTE

For more information regarding the SATA PHY pin name (or ball name) and corresponding signal name, see [Table 3-23, SATA Signal Descriptions](#).

4.4.8 System DC Electrical Characteristics

NOTE

Slicer functionality is not supported in the device.

Table 4-23 summarizes the System dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (DS[1:0], SC[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the Device TRM.

Table 4-23. System DC Electrical Characteristics

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--|---|---------------------------|-----|---------------------------|------|
| Signal Names in Mode 0: sys_nrespwron, sys_nreswarm | | | | | |
| Bottom Balls: F31 / F29 | | | | | |
| 1.8-V Mode | | | | | |
| V _{IH} | Input high-level threshold | 0.65 × vdds_bank24 | | | V |
| V _{IL} | Input low-level threshold | | | 0.35 × vdds_bank24 | V |
| V _{HYS} | Input hysteresis voltage | 135 | | | mV |
| V _{OH} | Output high-level threshold (I _{OH} = 2 mA) | vdds_bank24—0.45 | | | V |
| V _{OL} | Output low-level threshold (I _{OL} = 2 mA) | | | 0.45 | V |
| Z _O | Output impedance (drive strength) | DS[1:0] = 00 | | 120 | Ω |
| | | DS[1:0] = 01 | | 60 | |
| | | DS[1:0] = 10 | | 40 | |
| | | DS[1:0] = 11 | | 30 | |
| Signal Names in Mode 0: freq_xtal_in, freq_xtal_out | | | | | |
| Bottom Balls: E32 / D32 | | | | | |
| V _{IH} | Input high-level threshold | 0.65 × vdds_osc | | | V |
| V _{IL} | Input low-level threshold | | | 0.35 × vdds_osc | V |
| V _{HYS} | Input hysteresis voltage | 150 | | | mV |
| C _{IN} | Input capacitance | 1.25 | 1.4 | 1.55 | pF |
| t _{IT} | Input transition time (t _R or t _F evaluated between 10% and 90% of V _{PAD}) | | | 5 | ns |
| C _{OUT} | Load capacitance (C _{L1} = C _{L2}) | 12 | | 24 | pF |
| Signal Name in Mode 0: freq_xtal_clk | | | | | |
| Bottom Ball: D31 | | | | | |
| V _{OH} | Output high-level threshold (I _{OH} = 2 mA) | 0.7 × vdds_osc | | | V |
| V _{OL} | Output low-level threshold (I _{OL} = 2 mA) | | | 0.3 × vdds_osc | V |
| f _{OUT} | Output frequency, freq_xtal_clk | | | 100 | MHz |
| t _{WOUT} | Output pulse duration, freq_xtal_clk low or high | 0.45 × 1/f _{OUT} | | 0.55 × 1/f _{OUT} | ns |
| t _{OT} | Output transition time (t _R or t _F evaluated between 20% and 80% of V _{PAD}), freq_xtal_clk | | | 0.5 | ns |
| C _{OUT} | Load capacitance | | | 5 | pF |
| Signal Name in Mode 0: freq_slicer_in | | | | | |
| Bottom Ball: B28 | | | | | |
| Single-ended Application Mode | | | | | |

Table 4-23. System DC Electrical Characteristics (continued)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--|--|--------------------|------|--------------------|------|
| V _{SWING} | Input voltage swing ⁽¹⁾ | 500 | | 1600 | mV |
| R _{IN} | Input resistance | | 18.3 | | kΩ |
| C _{IN} | Input capacitance | | | 2.5 | pF |
| Single-ended High-Voltage CMOS Application Mode | | | | | |
| V _{IH} | Input high-level voltage | 0.65 × vdda_slicer | | 2 | V |
| V _{IL} | Input low-level voltage | −0.2 | | 0.35 × vdda_slicer | V |
| R _{IN} | Input resistance | | 18.3 | | kΩ |
| C _{IN} | Input capacitance | | | 2.5 | pF |
| t _T | Input transition time (t _R or t _F) evaluated between 10% to 90% of V _{PAD} | 1.5 | | 10 | ns |

(1) The input voltage swing is the peak-peak input voltage.

Minimum input common mode voltage—input voltage swing / 2 > 0 V

Maximum input common mode voltage + input voltage swing / 2 < 1.6 V

4.4.9 Other Balls DC Electrical Characteristics

Table 4-24 summarizes the dc electrical characteristics in multiplexing mode 0 for balls (using the SMART IO) other than the ones described in through Section 4.4.8.

Table 4-24. Other Balls⁽³⁾ DC Electrical Characteristics

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--------------------------------|--|-----------------------------|-----|-----------------------------|------|
| 1.8-V Mode | | | | | |
| V _{IH} ⁽²⁾ | Input high-level threshold | 0.65 × vddsx ⁽¹⁾ | | | V |
| V _{IL} ⁽²⁾ | Input low-level threshold | | | 0.35 × vddsx ⁽¹⁾ | V |
| V _{HYS} | Input hysteresis voltage | 130 | | | mV |
| V _{OH} | Output high-level threshold (I _{OH} = 2 mA) | vddsx ⁽¹⁾ −0.45 | | | V |
| V _{OL} | Output low-level threshold (I _{OL} = 2 mA) | | | 0.45 | V |
| C _{PAD} | Pad capacitance (including package capacitance) | | | 3 | pF |
| Z _O | Output impedance (drive strength) | DS[1:0] = 00 | 120 | | Ω |
| | | DS[1:0] = 01 | 60 | | |
| | | DS[1:0] = 10 | 40 | | |
| | | DS[1:0] = 11 | 30 | | |
| 1.2-V Mode | | | | | |
| V _{IH} | Input high-level threshold | 0.65 × vddsx ⁽¹⁾ | | | V |
| V _{IL} | Input low-level threshold | | | 0.35 × vddsx ⁽¹⁾ | V |
| V _{HYS} | Input hysteresis voltage | 60 | | | mV |
| V _{OH} | Output high-level threshold (I _{OH} = 2 mA) | 0.75 × vddsx ⁽¹⁾ | | | V |
| V _{OL} | Output low-level threshold (I _{OL} = 2 mA) | | | 0.25 × vddsx ⁽¹⁾ | V |
| C _{PAD} | Pad capacitance (including package capacitance) | | | 3 | pF |
| Z _O | Output impedance (drive strength) | DS[1:0] = 00 | 120 | | Ω |
| | | DS[1:0] = 01 | 60 | | |
| | | DS[1:0] = 10 | 40 | | |
| | | DS[1:0] = 11 | 30 | | |

- (1) For more information regarding the corresponding power supply (vddsx) for each ball described in the section, see [Table 3-1](#), POWER NAME [9] column.
- (2) Input voltage level could be in an undefined state (between V_{IL} and V_{IH}) for a maximum of 1 second without causing any damage.
- (3) Other balls using the SMART IO.

4.5 Handling Ratings

[Table 4-25](#) presents the Device Handling Rating requirements.

Table 4-25. Handling Ratings

| PARAMETER | | Limits |
|--|--|--|
| Electrostatic Discharge (ESD) Performance(1) | ESD-HBM (Human Body Model)(2) | ± 1000 V |
| | ESD-CDM (Charged Device Model)(3) | ± 250 V |
| T_{STG} (4) | Storage temperature range after soldered onto PC board | -65°C to 150°C |

- (1) Electrostatic discharge (ESD) to measure device sensitivity or immunity to damage caused by electrostatic discharges into the device.
- (2) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500-V HBM is possible if necessary precautions are taken. Pins listed as 1000 V may actually have higher performance.
- (3) Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250-V CDM is possible if necessary precautions are taken. Pins listed as 250 V may actually have higher performance.
- (4) For tape and reel the storage temperature range is [-10°C to 50°C] with a maximum relative humidity of 70%. It is recommended returning to ambient room temperature before usage.

4.6 Thermal Characteristics

For reliability and operability concerns, the maximum junction temperature of Device has to be at or below the T_J value identified in [Section 4.2, Recommended Operating Conditions](#).

Depending on the thermal mechanical design and worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level with the power worst use case.

The OMAP level thermal policy relies on a PCB sensor. Therefore, it is recommended to have such sensors located on the PCB; for more information, see [PCB Temperature Sensor](#). In addition, it is recommended to avoid having another significant thermal source near the Device.

The risks of not managing this junction temperature are hazardous heating, power supply clamping, reliability issues, and malfunction.

4.6.1 Package Thermal Characteristics

[Table 4-26](#) provides the thermal resistance characteristics for the package used on this device.

NOTE

Power dissipation of 4 W and an ambient temperature of 85°C is assumed for AAN package.

Table 4-26. Thermal Resistance Characteristics (AAN Package)

| NO. | PARAMETER | DESCRIPTION | °C/W(1) | AIR FLOW (m/s)(2) |
|-----|-------------------|-------------------------|---------|-------------------|
| T1 | $R_{\theta_{JC}}$ | Junction-to-case | 1.55 | N/A |
| T2 | $R_{\theta_{JB}}$ | Junction-to-board | 5.53 | N/A |
| T3 | $R_{\theta_{JA}}$ | Junction-to-free air | 15.5 | 0 |
| T4 | | Junction-to-moving air | 14.4 | 1 |
| T5 | | | 13.0 | 2 |
| T6 | | | 12.2 | 3 |
| T7 | ψ_{JT} | Junction-to-package top | 1.71 | 0 |
| T8 | | Junction-to-package top | 1.69 | 1 |
| T9 | | | 1.66 | 2 |
| T10 | | | 1.64 | 3 |
| T11 | ψ_{JB} | Junction-to-board | 5.79 | 0 |
| T12 | | Junction-to-board | 5.69 | 1 |
| T13 | | | 5.62 | 2 |
| T14 | | | 5.52 | 3 |

(1) These measurements were conducted in a JEDEC defined 2S2P system (with the exception of the Theta JC [$R_{\theta_{JC}}$] measurement, which was conducted in a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

Power dissipation of 4 W and an ambient temperature of 85°C is assumed.

(2) m/s = meters per second

4.7 Power-On Hours

The information in the section below is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

NOTE

POH is a functional of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH to achieve the same reliability performance. For assessment of alternate use cases, contact your local TI representative.

Table 4-27. Non-Automotive POH Limits

| Usage condition | (POH) | (POH) | (POH) |
|---|---------|---------|--------|
| Device Lifetime at Max Junction Temp (Tj) | 90°C | 100°C | 105°C |
| No HDMI; No VD_MPU OPP_HIGH_MPU | 100 000 | 100 000 | 58 000 |
| HDMI enabled; No VD_MPU OPP_HIGH_MPU | 100 000 | 63 000 | 45 000 |
| No HDMI; All VD_MPU OPP's | 65 000 | 55 000 | 50 000 |
| Unrestricted | 65 000 | 55 000 | 45 000 |

4.8 Power Supply Sequences

NOTE

Slicer functionality is not supported in the device.

4.8.1 Power-Up Sequence

NOTE

For more information, see Power, Reset and Clock Management / Reset Management Functional Description / Reset Sequences of the Device TRM.

Figure 4-2 shows the power-up sequence.

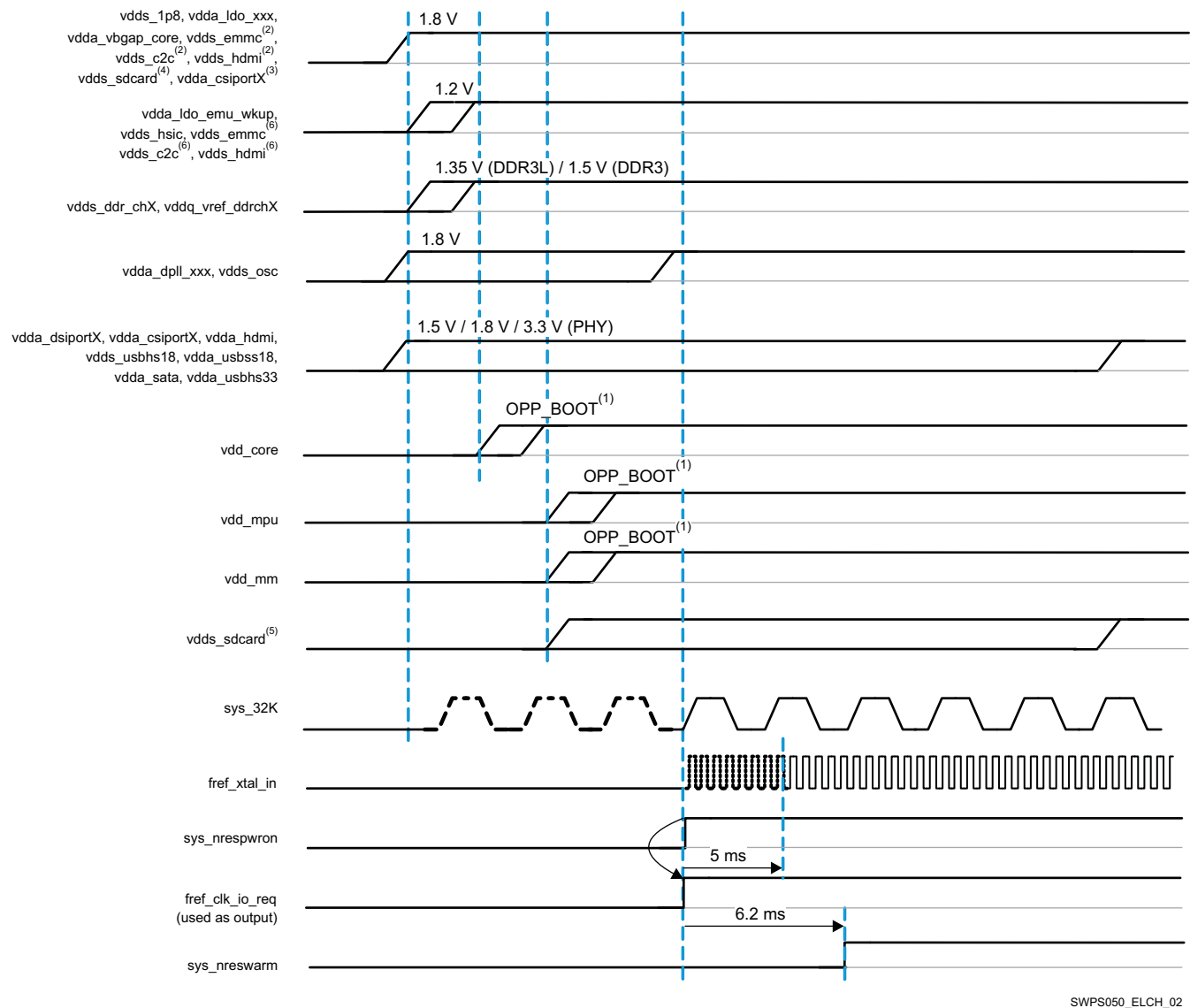


Figure 4-2. Power-Up Sequence

- (1) The device boots up with vdd_core, vdd_mpu, and vdd_mm @OPP_BOOT. See the operating condition addendum for values. OPP voltage values may change following the silicon characterization result.
- (2) In case the corresponding interfaces are used at 1.8 V.

- (3) In case the MIPI CSI-2 interface is used as GPIO or CPI (function different from Muxmode 0).
- (4) In case the SDCARD interface is used at 1.8 V only (function different from Muxmode 0).
- (5) In case the SDCARD functional signals are used at 1.8 V or 3.0 V (Muxmode 0).
- (6) In case the corresponding interfaces are used at 1.2 V.

NOTE

The DPLLs voltage supplies (vdda_dpll_xxx) and the system clock IOs voltage supplies (vdds_osc) can be turned on at the same time as the other 1.8-V voltage supplies or only before sys_nrespwron release.

The 1.5-V, 1.8-V, and 3.3-V PHY voltage supplies can be turned on at the same time as the other 1.8-V voltage supplies or only when the corresponding applications are needed.

Once vdda_ldo_emu_wkup is turned on, vdd_core can be turned on. Once vdd_core is turned on, vdd_mpu and vdd_mm can be turned on.

If the SDCARD functional signals are used at 1.8-V or 3.0-V, the vdds_sdc card voltage supply can be turned on any time after vdd_core ramp-up or only when the applications are needed.

sys_32k can be turned on any time after vdds_1p8 ramp-up and before sys_nrespwron release.

Once the sys_nrespwron is released, device activates the fref_clk_ioreq signal. Therefore, the fref_xtal_in clock can be turned on. (Nevertheless, the system can turn on the fref_xtal_in or clock before the fref_clk_ioreq activation provided the voltage supplies of the system clock IOs are turned on.)

5 ms after the sys_nrespwron release, the system clock is considered as stabilized on the device oscillator input. The clock may be supplied later provided it is perfectly stabilized when supplied.

1.2 ms (about 40 additional 32-kHz clock cycles) after the system clock is considered as stabilized, device releases its sys_nreswrm.

NOTE

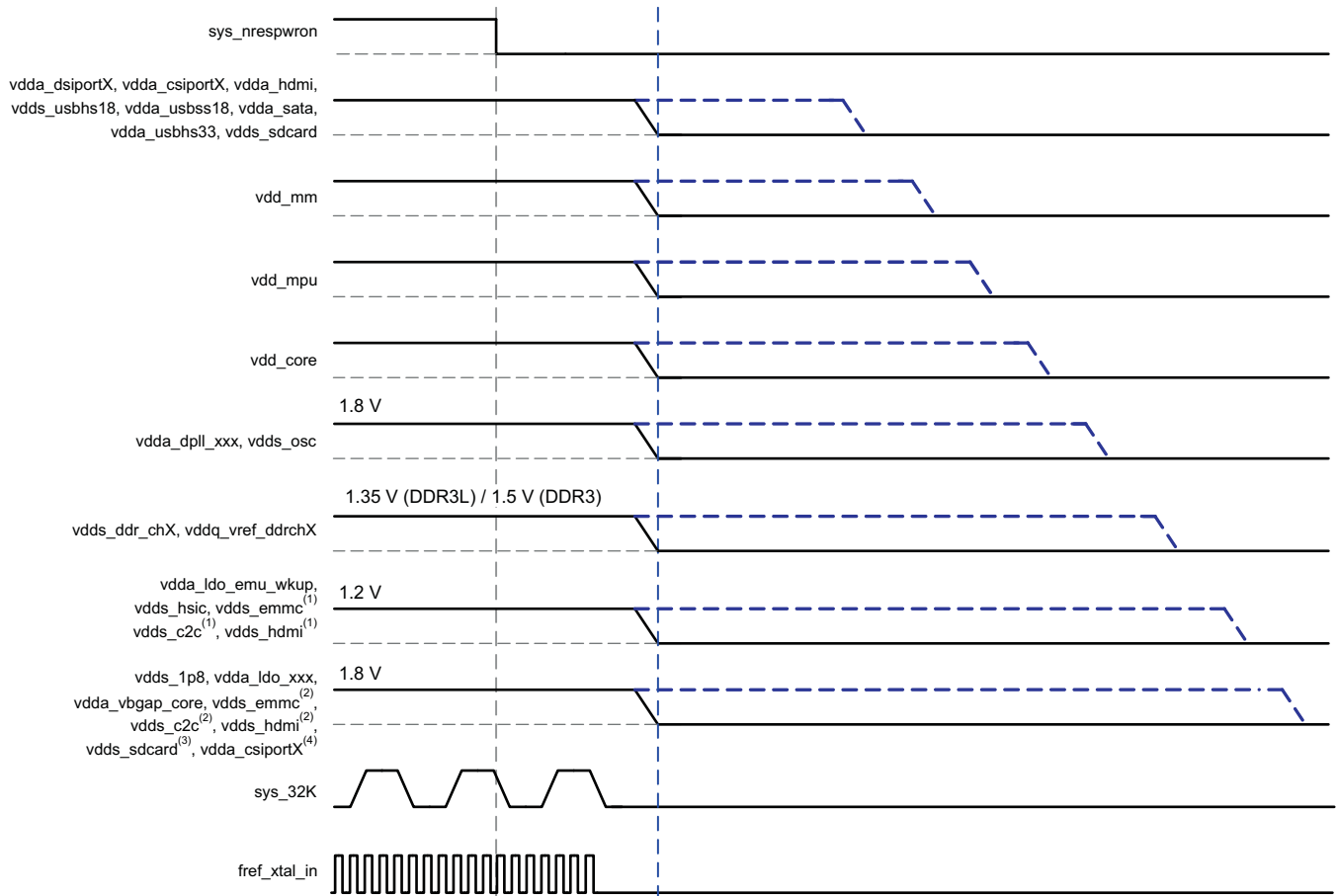
Customer designs may optionally power-up only the boot interfaces (eMMC, uSD card, USB, and SATA) that their particular design needs to use. For example, if only eMMC is required then uSD card, USB, and SATA supplies do not need to be powered up. The TWL6037 PMIC is programmed to power up all the possible interfaces in order to be able to boot on any possible interface.

4.8.2 Power-Down Sequence

The following steps give two examples of power-down sequence supported by the device:

1. Put the device under reset (sys_nrespwron).
2. Stop all signals driven to its balls (sys_32k or fref_xtal_in).
3. Either:
 - (a) Shutdown all voltage supplies at once. This sequence is described in black color in [Figure 4-3](#).
 - (b) Or, if the shutdown is sequenced, described in dashed blue color in [Figure 4-3](#):
 - (i) Turn off all PHY voltage supplies and SDCARD voltage supply.
 - (ii) Turn off the multimedia (IVA, DSP, GPU) voltage domain supply (vdd_mm).
 - (iii) Turn off the MPU voltage domain supply (vdd_mpu).
 - (iv) Turn off the core voltage domain supply (vdd_core).
 - (v) Turn off all DPLL and system clock IO voltage supplies.
 - (vi) Turn off all 1.2-V IO voltage supplies.
 - (vii) Turn off all remaining 1.8-V IO voltage supplies.

Figure 4-3 shows both power-down sequences: one of them is described in black color, and the other one in dashed blue color.



SWPS050_ELCH_03

Figure 4-3. Power-Down Sequence

- (1) In case the corresponding interfaces are used at 1.2 V.
- (2) In case the corresponding interfaces are used at 1.8 V.
- (3) In case the SDCARD interface is used at 1.8 V only (function different from Muxmode 0).
- (4) In case the MIPI CSI-2 interface is used as GPIO or CPI (function different from Muxmode 0).

NOTE

sys_32k can be turned off any time after sys_nrespwron assertion and before vdds_1p8 shutdown.

The fref_xtal_in clock can be turned off any time after sys_nrespwron assertion and before the system clock IOs voltage supplies shutdown (vdds_osc).

5 Clock Specifications

NOTE

For more information, see Power Reset and Clock Management / PRCM Environment / External Clock Signal and Power Reset / PRCM Functional Description / PRCM Clock Manager Functional Description section of the Device TRM.

The device operation requires the following clocks:

- The 32-kHz frequency clock is used for low frequency operation. It supplies the wake-up (WKUP) domain for operation in the lowest power mode, the clock source for the DPLL of the audio back-end module.
- The system clock signal with the following possible frequencies: 12, 16.8, 19.2, 26, or 38.4 MHz) is the main source clock of the device. It supplies the reference clock to the DPLLs as well as the functional clock to several OMAP modules.

The system clock source could be either:

- A CMOS square clock that enters on the `fref_xtal_in` pin (signal is IO voltage level) with `fref_xtal_out` left unconnected.
- A crystal oscillator clock managed by `fref_xtal_in` and `fref_xtal_out`. In this situation, the crystal clock frequency must be between 12 and 19.2 MHz (other values must be checked case by case). The crystal is oscillating on the fundamental frequency (oscillation on third harmonic is not supported).

The system clock source are configurable on `sys_boot[5:4]`. For more information, see the Device TRM.

The device delivers two clock signals (`fref_clk[1:0]_out`) to external devices:

- The clocks are configurable and can be managed by software or by hardware thanks to the `fref_clk_ioreq` (when in input direction) pin.
- When `fref_clk_ioreq` is configured as output, the signal is used to request an external clock source for the device. When configured as input (oscillator enabled), this `fref_clk_ioreq` pin can be used as an additional clock request `fref_clk0_req`.
- Output `fref_clk[1:0]_out` clocks come from:
 - Either the input system clock and alternate clock (`fref_xtalin`)
 - Or, a core clock (from DPLL_CORE output)
 - Or, a 192-MHz clock (from PER DPLL output)

Each of this clock can be divided and independantly controlled by software. For more information, see the Device TRM.

- Each of the output clocks can be gated or enabled independently by activation of the associated clock request signals, `fref_clk_ioreq` pin.

The `fref_clk_ioreq` pin can be used as `fref_clk0_req` signal when configured as input pin (oscillator enabled).

By default:

- The `fref_clk0_req` auxiliary clock request (`fref_clk_ioreq` as input pin) is mapped on the `fref_clk0_out` auxiliary clock.

A re-mapping is possible to map the `fref_clk0_req` clock request on the `fref_clky_out` clock ($y = [1:0]$).

The polarity of `fref_clk_ioreq` pins is programmable (active High by default after reset).

- `fref_clk_ioreq` is an open-drain output (driving a low-level when requesting clock, else output driver is in Hi-Z and line must have a pullup to maintain it inactive) or open-source (driving a high-level when requesting clock, else output driver is in Hi-Z and line must have a pulldown to maintain it inactive) for requesting the clock to an external clock source device when the SYS.CLK clock is not provided by the crystal oscillator (that is, when `SYS_BOOT[5:4] ≠ 2b'00`).

The device also embeds an internal free-running 32-kHz oscillator that is always active as long as the the wake-up (WKUP) domain is supplied.

Figure 5-1 shows the external input clock sources and the output clocks to peripherals.

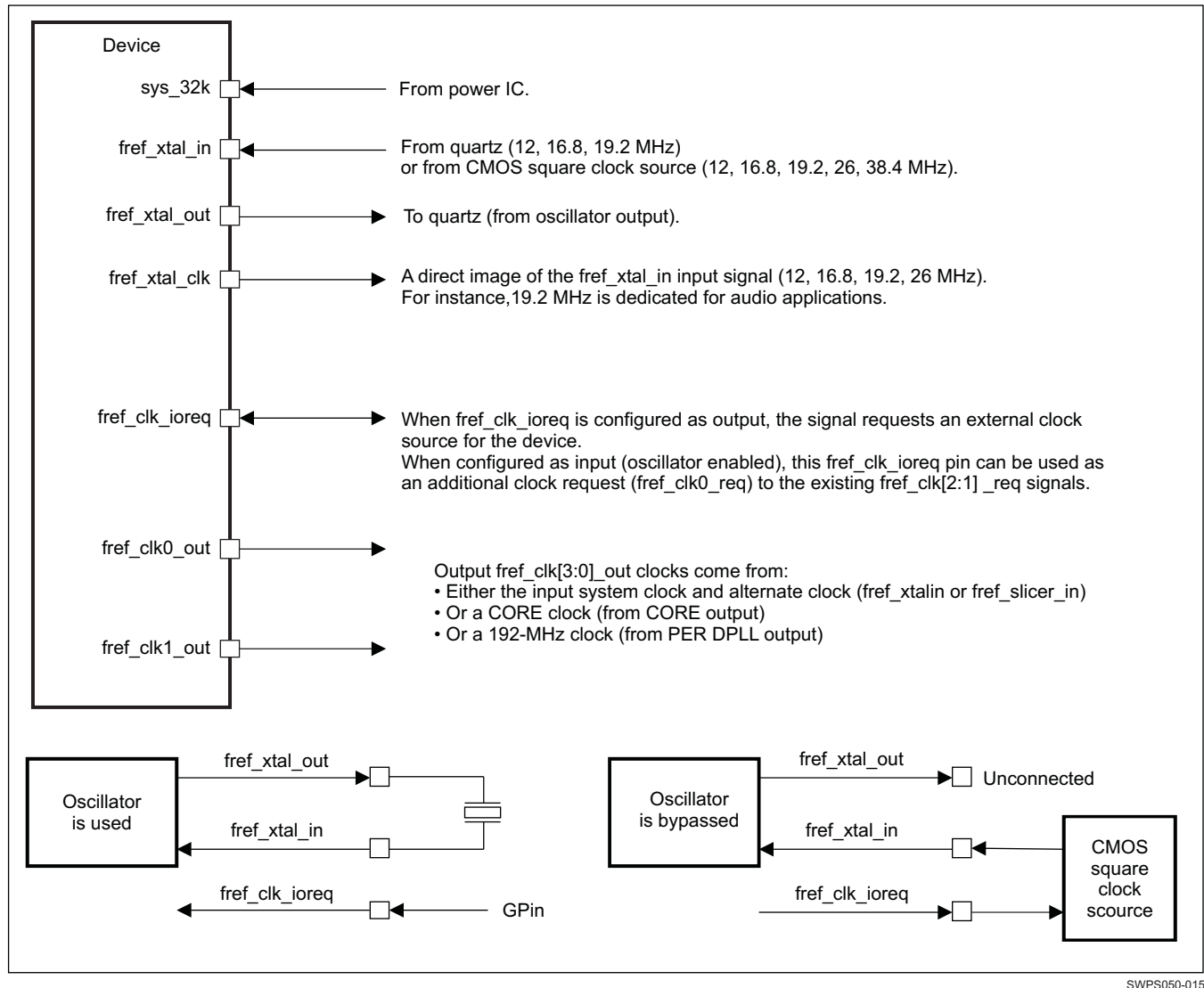


Figure 5-1. Clock Interface

5.1 Input Clock Specifications

5.1.1 Input Clock Requirements

The source of the internal system clock (SYS.CLK) could be either:

- A CMOS square clock that enters on the fref_xtal_in ball (with fref_xtal_out left unconnected on the CMOS square clock case).
- A crystal oscillator clock managed by fref_xtal_in and fref_xtal_out (oscillating in the fundamental 10-MHz to 20-MHz frequency range).

Table 5-1 illustrates the requirements to supply an input clock to the device.

Table 5-1. Input Clock Requirements⁽⁴⁾

| PAD | CLOCK FREQUENCY | STABILITY | DUTY CYCLE | JITTER | TRANSITION |
|---------|-----------------|-----------|------------|--------|------------|
| sys_32k | 32.768 kHz | ± 200 ppm | NA | NA | < 30 ns |

Table 5-1. Input Clock Requirements⁽⁴⁾ (continued)

| PAD | CLOCK FREQUENCY | | STABILITY | DUTY CYCLE | JITTER | TRANSITION |
|-------------------------------|---------------------------------|---------------|------------------------------|------------|--|------------|
| fref_xtal_in fref_xtal_out | 12, 16.8, or 19.2 MHz | Crystal clock | ± 50 (±5) ppm ⁽³⁾ | NA | NA | NA |
| | 12, 16.8, 19.2, 26, or 38.4 MHz | Square clock | ± 50 (±5) ppm ⁽³⁾ | 45% to 55% | $0.5\% \times t_{c(XTALIN)}^{(2)} \times X_{DIV}^{(1)}$ (ps) | < 5 ns |

- (1) In X_{DIV} , X_{DIV} represents the internal DSS DPLLs dividers. [$t_{c(XTALIN)}$ (ps) $\times X_{DIV}$] represents the input clock cycle coming to the DSS DPLLs (this means after dividing). For the other internal DPLLs, the X_{DIV} value is equal to 1. This input jitter limitation comes from the DPLL constraints shifted at ball level. To clarify this formula, please consider a maximum jitter of 1% of the clock period coming to the internal DPLL (input DPLL). For more information, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / PRM Clock Source section of the Device TRM.
- (2) $t_{c(XTALIN)}$ is the fref_xtal_in cycle time of the clock coming to fref_xtal_in ball.
- (3) ±50 ppm is the clock frequency stability/accuracy and ±5 ppm takes into account the aging effects.
- (4) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding OMAP5 VDD5 power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

5.1.1.1 sys_32k CMOS Input Clock

Table 5-2 summarizes the electrical characteristics of the sys_32k input clock.

Table 5-2. sys_32k Input Clock Electrical Characteristics

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|----------------|--------------------|-----|--------|-----|------|
| f | Frequency, sys_32k | | 32.768 | | kHz |
| C _I | Input capacitance | | | 3 | pF |
| R _I | Input resistance | 3 | | 10 | GΩ |

Table 5-3 details the input requirements of the sys_32k input clock.

Table 5-3. sys_32k Input Clock Timing Requirements⁽¹⁾⁽²⁾

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|------|------------------|------------------------------|-----|--------|-----|------|
| CK0 | 1 / $t_{c(32k)}$ | Frequency, sys_32k | | 32.768 | | kHz |
| | $t_{R(32k)}$ | Rise time, sys_32k | | | 30 | ns |
| | $t_{F(32k)}$ | Fall time, sys_32k | | | 30 | ns |
| | $t_{j(32k)}$ | Frequency stability, sys_32k | | | 200 | ppm |

- (1) See Section 4.4.8, System DC Electrical Characteristics, SYS (clk32k ...) part for sys_32k V_{IH} /V_{IL} parameters.
- (2) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding OMAP5 VDD5 power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

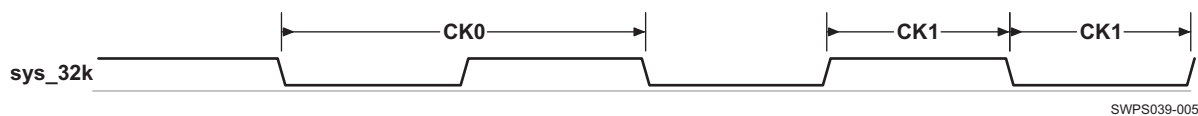
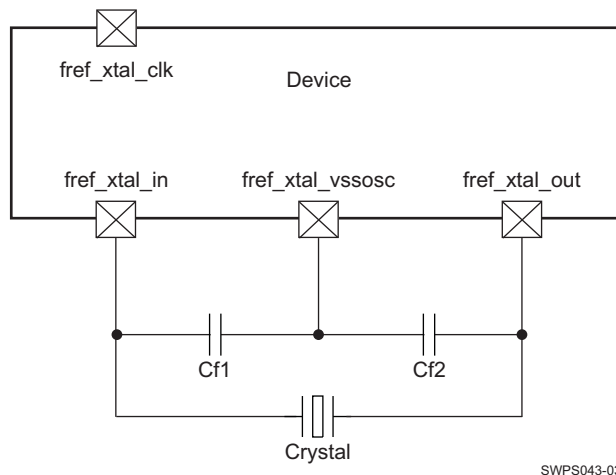


Figure 5-2. sys_32k Input Clock

5.1.1.2 fref_xtalin CMOS Input Clock

5.1.1.2.1 fref_xtal_in / fref_xtal_out External Crystal

An external crystal is connected to the device pins. Figure 5-3 describes the crystal implementation.

Figure 5-3. Crystal Implementation⁽¹⁾

(1) When the oscillator is bypassed, the fref_xtal_in ball is connected to a square clock source, the fref_xtal_out ball is not connected and the fref_xtal_vssosc ball is connected to the ground.

When the oscillator is not used, the fref_xtal_in and fref_xtal_out balls can be connected to the ground, or not connected and the fref_xtal_vssosc ball is connected to the ground.

The crystal must be in the fundamental mode of operation and parallel resonant. Table 5-4 summarizes the required electrical constraints.

Table 5-4. Crystal Electrical Characteristics⁽²⁾

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|--------------------------------------|---|-------------------|-------|-----|----------|
| f_p | Parallel resonance crystal frequency | 12, 16.8, or 19.2 | | | MHz |
| C_{f1} | C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | 12 | | 24 | pF |
| C_{f2} | C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | 12 | | 24 | pF |
| $ESR(C_{f1}, C_{f2})$ ⁽¹⁾ | Frequency 12 MHz, Negative resistor at nominal 500 Ω , Negative resistor at worst case 300 Ω | | | 100 | Ω |
| | Frequency 16.8 MHz and 19.2 MHz, Negative resistor at nominal 300 Ω , Negative resistor at worst case 180 Ω | | | 60 | |
| C_O | Crystal shunt capacitance | | | 4.5 | pF |
| L_M | Crystal motional inductance for $f_p = 12$ MHz | | 16 | | mH |
| C_M | Crystal motional capacitance | | 10.87 | | fF |
| D_L | Crystal drive level | | | 0.5 | mW |

(1) Measured with the load capacitance specified by the crystal manufacturer. This load is defined by the foot capacitances tied in series. If $C_L = 20$ pF, then both foot capacitors will be $C_{f1} = C_{f2} = 40$ pF. Parasitic capacitance from package and board must also be taken in account.

(2) The crystal motional resistance R_M is related to the equivalent series resistance (ESR) by the following formula:

$$ESR = R_M \times (1 + (C_O \times C_{f1} \times C_{f2} / (C_{f1} + C_{f2})))^2.$$

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 5-5 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 5-5. Oscillator Switching Characteristics—Crystal Mode

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|----------|---------------------------------|-------------------|-----|-----|------|
| f_p | Oscillation frequency | 12, 16.8, or 19.2 | | | MHz |
| t_{sX} | Start-up time ⁽¹⁾⁽²⁾ | | | 1.2 | ms |

- (1) Start-up time is defined as the time the oscillator takes to gain $f_{ref_xtal_in}$ amplitude enough to have 45% to 55% duty cycle at the core input from the time power down (PWRDN) is released. Start-up time is a strong function of crystal parameters. At power-on reset, the time is adjustable using the pin itself. The reset must be released when the oscillator or clock source is stable. To switch from bypass mode to crystal or from crystal mode to bypass mode, there is a waiting time about 100 μ s; however, if the chip comes from bypass mode to crystal mode the crystal will start-up after time mentioned in the t_{sX} parameter.
- (2) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a square wave. The switching time in this case is about 100 μ s.

5.1.1.2.2 $f_{ref_xtal_in}$ Squarer Input Clock

Table 5-6 summarizes the $f_{ref_xtal_in}$ input square clock electrical characteristics.

Table 5-6. $f_{ref_xtal_in}$ Input Square Clock Electrical Characteristics—Bypass Mode

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------------|------------------------------|-----------------------------|------|------|------------|
| f | Frequency | 12, 16.8, 19.2, 26, or 38.4 | | | MHz |
| C _I | Input capacitance | 1.00 | 1.15 | 1.35 | pF |
| R _I | Input resistance | 3.1 | 132 | 1100 | M Ω |
| t _{sX} | Start-up time ⁽¹⁾ | See ⁽²⁾ | | | ms |

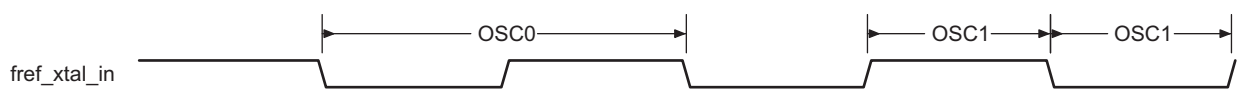
- (1) To switch from bypass mode to crystal or from crystal mode to bypass mode, there is a waiting time about 100 μ s; however, if the chip comes from bypass mode to crystal mode the crystal will start-up after time mentioned in Table 5-5, t_{sX} parameter.
- (2) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a square wave. The switching time in this case is about 100 μ s.

Table 5-7 details the $f_{ref_xtal_in}$ input square clock timing requirements.

Table 5-7. $f_{ref_xtal_in}$ Input Square Clock Timing Requirements—Bypass Mode⁽³⁾

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------|---|-------------------------------|-----|--|------|
| OCS0 | 1 / t _{c(xtalin)} Frequency, $f_{ref_xtal_in}$ | 12, 16.8, 19.2, 26, or 38.4 | | | MHz |
| OCS1 | t _{w(xtalin)} Pulse duration, $f_{ref_xtal_in}$ low or high | 0.45 × t _{c(XTALIN)} | | 0.55 × t _{c(XTALIN)} | ns |
| | t _{j(xtalin)} Peak-to-peak jitter ⁽¹⁾ , $f_{ref_xtal_in}$ | | | 0.5% × t _{c(XTALIN)} × X _{DIV} ⁽⁴⁾ (ps) × | ps |
| | t _{R(xtalin)} Rise time, $f_{ref_xtal_in}$ | | | 5 | ns |
| | t _{F(xtalin)} Fall time, $f_{ref_xtal_in}$ | | | 5 | ns |
| | t _{j(xtalin)} Frequency stability, $f_{ref_xtal_in}$ | | | 50 (±5) ⁽²⁾ | ppm |

- (1) Peak-to-peak jitter is meant here as follows:
 - The maximum value is the difference between the longest measured clock period and the expected clock period
 - The minimum value is the difference between the shortest measured clock period and the expected clock period
 Maximum and minimum are obtained on a statistical population of 300 period samples and expressed relative to the expected clock period.
- (2) ±50 ppm is the clock frequency stability/accuracy and ± 5 ppm takes into account the aging effects.
- (3) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding OMAP5 VDD5 power supply name, see Table 3-1, POWER NAME [9] column with the ball name.
- (4) In X_{DIV}, X_{DIV} represents the internal DSS DPLLs dividers. [t_{c(XTALIN)} (ps) × X_{DIV}] represents the input clock cycle coming to the DSS DPLLs (this means after dividing). For the other internal DPLLs, the X_{DIV} value is equal to 1. For more information, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / PRM Clock Source section of the Device TRM.
- (5) t_{c(XTALIN)} is the $f_{ref_xtal_in}$ cycle time of the clock coming to $f_{ref_xtal_in}$ ball.



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Figure 5-4. $f_{ref_xtal_in}$ Input Square Clock

5.1.1.2.3 *fref_xtal_clk* Output Clock

The signal on the *fref_xtal_clk* output pad is a direct image of the signal on the *fref_xtal_in* input pad. It is available when oscillator is active or bypassed.

Table 5-8 summarizes the *fref_xtal_clk* output clock electrical characteristics.

Table 5-8. *fref_xtal_clk* Output Clock Electrical Characteristics

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|----------------|--|-----------------------|-----|-----|------|
| f | Frequency, <i>fref_xtal_clk</i> | 12, 16.8, 19.2, or 26 | | | MHz |
| C _L | Load capacitance (Transmission line load + Far-end load) | | | 5 | pF |

Table 5-9 details the *fref_xtal_clk* output switching characteristics.

Table 5-9. *fref_xtal_clk* Output Switching Characteristics⁽³⁾

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|------|-----------------------------|---|--------------------------------|-----|--|------|
| OCS0 | 1 / t _{c(xtalclk)} | Frequency, <i>fref_xtal_clk</i> | 12, 16.8, 19.2, or 26 | | | MHz |
| OCS1 | t _{w(xtalclk)} | Pulse duration, <i>fref_xtal_clk</i> low or high | 0.45 × t _{c(XTALCLK)} | | 0.55 × t _{c(XTALCLK)} | ns |
| | t _{j(xtalclk)} | Peak-to-peak jitter ⁽¹⁾ , <i>fref_xtal_clk</i> | | | t _{J(XTALIN)} ⁽⁴⁾ + 150 (ps) | ps |
| | t _{R(xtalclk)} | Rise time, <i>fref_xtal_clk</i> | | | 0.5 | ns |
| | t _{F(xtalclk)} | Fall time, <i>fref_xtal_clk</i> | | | 0.5 | ns |
| | t _{j(xtalclk)} | Frequency stability, <i>fref_xtal_clk</i> | | | 50 (±5) ⁽²⁾ | ppm |

(1) Peak-to-peak jitter is meant as follows:

- The maximum value is the difference between the longest measured clock period and the expected clock period.
- The minimum value is the difference between the shortest measured clock period and the expected clock period.

Maximum and minimum are obtained on a statistical population of 300 period samples and expressed relative to the expected clock period.

(2) ±50 ppm is the clock frequency stability/accuracy and ± 5 ppm takes into account the aging effects.

(3) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding OMAP5 VDD5 power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

(4) t_{J(xtal_in)} corresponds to the external jitter coming to the *fref_xtal_in* input PAD.

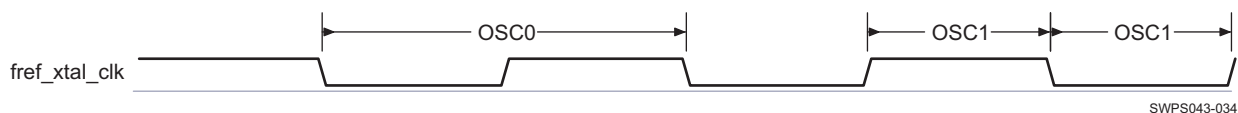


Figure 5-5. *fref_xtal_clk* Squarer Input Clock

5.2 Output Clock Specifications

5.2.1 FREF Output Clocks

Four configurable clock output signals are available on *fref_clk[1:0]_out* pins. The clocks are configurable and can be managed by software and/or by hardware with the *fref_clk_ioreq* (when in input direction) pin.

When *fref_clk_ioreq* is configured as output, the signal is used to request an external clock source for the device. When configured as input (oscillator enabled), this *fref_clk_ioreq* pin can be used as an additional clock request *fref_clk0_req*.

Each of the output clocks can be gated or enabled independently by activation of the associated clock request signals, *fref_clk_ioreq* pin.

The *fref_clk_ioreq* pin can be used as the *fref_clk0_req* signal when configured as input pin (oscillator enabled).

By default:

- The `fref_clk0_req` auxiliary clock request (`fref_clk_ioreq` as input pin) is mapped on the `fref_clk0_out` auxiliary clock.

A re-mapping is possible to map the `fref_clk0_req` clock request on the `fref_clkx_out` clock ($y = [1:0]$)

Output `fref_clk[1:0]_out` clocks come from either:

- The input system clock and alternate clock (`fref_xtalin`)
- Or, a CORE clock (from DPLL_CORE output)
- Or, a 192-MHz clock (from PER DPLL output)

Each of these clocks can be divided and independently controlled by software. For more information, see the Device TRM.

`fref_clk_ioreq` is an open-drain output (driving a low-level when requesting clock, else output driver is in Hi-Z and line must have a pullup to maintain it inactive) or open-source (driving a high-level when requesting clock, else output driver is in Hi-Z and line must have a pulldown to maintain it inactive) for requesting the clock to an external clock source device when the system clock is not provided by the crystal oscillator

For more information, see the System Clock and Reset Manager section of the Device TRM.

Table 5-10 summarizes the electrical characteristics of the `fref_clk1_out` output clock (especially targeted for the primary camera sensor functional input clock), `fref_clk2_out` output clock (targeted for the secondary camera sensor functional input clock), and `fref_clk0_out`, `fref_clk3_out`, `fref_clk4_out`, and `fref_clk5_out` output clocks (input clocks for the other peripherals).

Table 5-10. `fref_clkx_out` Output Clock Electrical Characteristics⁽¹⁾⁽²⁾

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|--|---|-----|-----|----------|
| f | Frequency, <code>fref_clkx_out</code> | <code>fref_xtal_in</code> ⁽³⁾ clock frequency, or <code>fref_slicer_in</code> ⁽³⁾ clock frequency, or DPLL_CORE ⁽³⁾ , or DPLL_PER ⁽³⁾ | | | MHz |
| Drive Strength, output impedance: DS[1:0] = 01 for $Z_O = 51$ to 65Ω Drive Strength, output impedance: DS[1:0] = 10 for $Z_O = 41$ to 50Ω Drive Strength, output impedance: DS[1:0] = 11 for $Z_O = 30$ to 40Ω | | | | | |
| Slew-rate Control: SC[1:0] = 10 | | | | | |
| C_L | Load capacitance (Transmission line load + Far-end load) | 5 | | 25 | pF |
| Z_T | Transmission line impedance | 30 | | 65 | Ω |
| L_T | Transmission line length | 1 | | 10 | cm |
| D_T | Transmission line delay time | | 67 | | ps |

(1) In `fref_clkx_out`, $x = 0, 1, 2,$ or 3 .

(2) The modes are configured by 4 bits, DS[1:0] and SC[1:0], of the IO cell. For more details, see the Device TRM.

(3) A divide factor from 1 to 16 can be applied on this clock frequency.

For more information, see the SCRM.AUXCLK[0:3] register, CLKDIV bitfield in the Device TRM.

Table 5-11 details the `fref_clk0_out`, `fref_clk1_out`, `fref_clk2_out`, and `fref_clk3_out` output clock switching characteristics.

Table 5-11. `fref_clkx_out` Output Clock Switching Characteristics⁽¹⁾⁽⁵⁾⁽⁷⁾⁽⁹⁾

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-------|--|--|-----|-----|------|
| f | Frequency, <code>fref_clkx_out</code> | <code>fref_xtal_in</code> clock frequency ⁽⁶⁾ , or <code>fref_slicer_in</code> clock frequency ⁽⁶⁾ , or DPLL_CORE clock frequency ⁽⁶⁾ , or DPLL_PER clock frequency ⁽⁶⁾ | | | MHz |
| FREF0 | $t_{c(\text{clkx_out})}$ Period, <code>fref_clkx_out</code> | 1 / f | | | ns |

Table 5-11. freq_clkx_out Output Clock Switching Characteristics⁽¹⁾⁽⁵⁾⁽⁷⁾⁽⁹⁾ (continued)

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT | |
|--|------------------------------------|---|--|---|--|---|----|
| $t_{j(\text{clkx_out})}$ | Peak-to-peak jitter, freq_clkx_out | From freq_xtal_in CORE DPLL or PER DPLL bypassed | | | $t_{j(\text{freq_xtal_in})} \times (1 + \text{CLKDIV}^{(6)}) + 0.400$ | ns | |
| | | From freq_xtal_in CORE DPLL or PER DPLL used | | | $2.5\% \times t_{(\text{dpll_out})} \times (1 + \text{CLKDIV}^{(6)}) + 0.125$ | | |
| | | From freq_slicer_in CORE DPLL or PER DPLL bypassed | | | $t_{j(\text{freq_slicer_in})} \times (1 + \text{CLKDIV}^{(6)}) + 0.440$ | | |
| | | From freq_slicer_in CORE DPLL or PER DPLL used | | | $2.5\% \times t_{(\text{dpll_out})} \times (1 + \text{CLKDIV}^{(6)}) + 0.125$ | | |
| Stability, freq_clkx_out | | 50 ⁽⁸⁾ | | | | ppm | |
| FREF1 | $t_{w(\text{clkx_out})}$ | Pulse duration, freq_clkx_out low or high | CLKDIV ⁽⁶⁾ value is even | From freq_xtal_in CORE DPLL or PER DPLL bypassed | | $[0.50 \times t_{c(\text{clkx_out})}] + t_{j(\text{clkx_out})}$ | ns |
| | | | | From freq_xtal_in CORE DPLL or PER DPLL used | | $[0.50 \times t_{c(\text{clkx_out})}] + t_{j(\text{clkx_out})}$ | |
| | | | | From freq_slicer_in CORE DPLL or PER DPLL bypassed | | $[0.50 \times t_{c(\text{clkx_out})}] + t_{j(\text{clkx_out})}$ | |
| | | | | From freq_slicer_in CORE DPLL or PER DPLL used | | $[0.50 \times t_{c(\text{clkx_out})}] + t_{j(\text{clkx_out})}$ | |
| | | | CLKDIV ⁽⁶⁾ value is odd | From freq_xtal_in CORE DPLL or PER DPLL bypassed | | $[(\text{CLKDIV}) / (2 \times \text{CLKDIV} + 2)] \times t_{c(\text{clkx_out})} + t_{j(\text{clkx_out})}$ | |
| | | | | From freq_xtal_in CORE DPLL or PER DPLL used | | $[(\text{CLKDIV}) / (2 \times \text{CLKDIV} + 2)] \times t_{c(\text{clkx_out})} + t_{j(\text{clkx_out})}$ | |
| | | | | From freq_slicer_in CORE DPLL or PER DPLL bypassed | | $[(\text{CLKDIV}) / (2 \times \text{CLKDIV} + 2)] \times t_{c(\text{clkx_out})} + t_{j(\text{clkx_out})}$ | |
| | | | | From freq_slicer_in CORE DPLL or PER DPLL used | | $[(\text{CLKDIV}) / (2 \times \text{CLKDIV} + 2)] \times t_{c(\text{clkx_out})} + t_{j(\text{clkx_out})}$ | |
| Drive Strength, output impedance: DS[1:0] = 01 for Z_O = 51 to 65 Ω | | | | | | | |
| Drive Strength, output impedance: DS[1:0] = 10 for Z_O = 41 to 50 Ω | | | | | | | |
| Drive Strength, output impedance: DS[1:0] = 11 for Z_O = 30 to 40 Ω | | | | | | | |
| Slew-rate Control: SC[1:0] = 10 | | | | | | | |
| | $t_{R(\text{clkx_out})}$ | Rise time, freq_clkx_out | 0.907 ⁽²⁾⁽⁴⁾ | | 1.931 ⁽³⁾ | ns | |
| | $t_{F(\text{clkx_out})}$ | Fall time, freq_clkx_out | 0.910 ⁽²⁾⁽⁴⁾ | | 2.225 ⁽³⁾ | ns | |

(1) In freq_clkx_out, x = 0, 1, 2, or 3

(2) At minimum load

(3) At maximum load

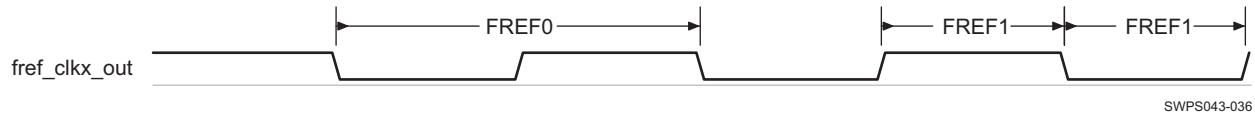
(4) **Caution:** this creates EMI parasitics up to 1.2 ns.(5) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding OMAP5 VDD5 power supply name, see [Table 3-1, POWER NAME \[9\]](#) column with the ball name.

(6) A divide factor from 1 to 16 can be applied on this clock frequency. For more information, see the SCRM.AUXCLK[0:3] register, CLKDIV bitfield in the Device TRM.

(7) clkx_out is the external clock signal at the freq_clkx_out output pin. dpll_out is the internal clock signal at the dpll output, before the clock divider controlled by CLKDIV.

(8) ±50 ppm is the clock frequency stability/accuracy and ±5 ppm takes into account the aging effects.

(9) $t_{j(\text{freq_xtal_in})}$ or $t_{j(\text{freq_slicer_in})}$ corresponds to the external jitter coming to the freq_xtal_in or freq_slicer_in input PAD.


Figure 5-6. fref_clkx_out Output Clocks⁽¹⁾

(1) In fref_clkx_out, x = 0, 1, 2, or 3.

5.2.2 DPLLs, DLLs Specifications

NOTE

For more information, see:

- Power, Reset and Clock Management / Clock Management Functional / Internal Clock Sources / Generators / Generic DPLL Overview Section and
- Display Subsystem / Display Subsystem Overview section of the Device TRM.

To generate high frequency clocks, the OMAP5430 device embeds 14 DPLLs. They all have the following common features:

- They have their own independent power domain (each one embeds its own switch and can be controlled as an independent functional power domain)
- They are fed with ALWAYS ON system clock, with independent control per DPLL
- Their analog part is supplied through dedicated power supply (1.8 V) and an embedded LDO.

The different DPLLs managed by the PRCM are listed below:

- DPLL_MPU: It supplies the MPU subsystem clocking internally.
- DPLL_IVA: It feeds the IVA and DSP subsystem clocking.
- DPLL_CORE: It supplies all interface clocks and also few module functional clocks. It generates clocks for EMIF and LPDDR2 PHYs. It can be also direct source of fref_clk[3:0]_out and emulation trace clock.
- DPLL_PER: It supplies several clock sources: a 192-MHz clock for the display functional clock and the ISS functional clock, a 96-MHz functional clock to subsystems and peripherals, fref_clk[3:0]_out and emulation trace clock.
- DPLL_ABE: This is the DPLL for the interface clock of Audio Back-End, the functional clock of ABE peripherals (McBSP1-3, and so on) and MPU, plus IVA subsystem bypass clock (this allows to clock these subsystems at ULP consumption, as only DPLL_ABE is active, DPLL_MPU and DPLL_IVA can be inactive). DPLL_ABE is optimized to produce up to 100-MHz clock from 32.768-kHz clock with a very low-power consumption.
- DPLL_USB: The USB_PHY contains one DPLL that feeds the USB_HOST_HS link, the USB_TLL_HS, and the USB2PHY module.

NOTE

The following DPLLs are controlled by the clock manager located in the always-on Core power domain (CM_CORE_AON):

- DPLL_MPU, DPLL_IVA, DPLL_CORE, and DPLL_ABE.

And the following DPLLs are managed by the clock manager in the Core power domain (CM_CORE):

- DPLL_PER and DPLL_USB.

For more information on CM_CORE_AON and CM_CORE or PRCM DPLLs, see the Power Reset Controller Manager (PRCM) chapter of the Device TRM.

The following DPLLs are not managed by the PRCM:

- DPLL_USB_OTG_SS: The USB SS DRD controller manages this DPLL. It supplies the functional clock of the USB SS DRD and associated PHYs.
- DPLL_SATA: The SATA PHY controller manages this DPLL. It supplies the functional clock of the SATA module and the PHYs.
- DPLL_DSI1_A, DPLL_DSI1_C and DPLL_HDMI: The display subsystem contains three DPLLs, which are directly managed by this subsystem. For more information, see the DSS (DSI, HDMI) section of the Device TRM.
- DPLL_DEBUGSS: The DEBUGSS manages this DPLL. It supplies the functional clock of the debug subsystem.

5.2.2.1 DPLL Characteristics

The DPLL has three relevant input clocks. One of them is the reference clock (CLKINP) used to generate the synthesized clock but can also be used as the bypass clock whenever the DPLL enters a bypass mode. It is therefore mandatory. The second one is a fast bypass clock (CLKINPULOW) used when selected as the bypass clock and is optional. The third clock (CLKINPHIF) is explained in the next paragraph.

The DPLL has three output clocks (namely CLKOUT, CLKOUTX2, and CLKOUTHIF). CLKOUT and CLKOUTX2 run at the bypass frequency whenever the DPLL enters a bypass mode. Both of them are generated from the lock frequency divided by a post-divider (namely M2 post-divider). The third clock, CLKOUTHIF, has no automatic bypass capability. It is an output of a post-divider (M3 post-divider) with the input clock selectable between the internal lock clock (Fdpll) and CLKINPHIF input of the PLL through an asynchronous multiplexing.

For more information, see the Power Reset Controller Management chapter of the Device TRM.

Table 5-12 summarizes DPLL type described in Section 5.2.2, *DPLLs, DLLs Specifications* introduction.

Table 5-12. DPLL Control Type

| DPLL NAME | TYPE | CONTROLLED BY PRCM |
|-----------------|---------------------|--------------------|
| DPLL_ABE | Table 5-13 (Type A) | Yes ⁽¹⁾ |
| DPLL_CORE | Table 5-13 (Type A) | Yes ⁽¹⁾ |
| DPLL_DSI1_A | Table 5-13 (Type A) | No ⁽²⁾ |
| DPLL_DSI1_C | Table 5-13 (Type A) | No ⁽²⁾ |
| DPLL_HDMI | Table 5-14 (Type B) | No ⁽²⁾ |
| DPLL_PER | Table 5-13 (Type A) | Yes ⁽¹⁾ |
| DPLL_SATA | Table 5-14 (Type B) | No ⁽²⁾ |
| DPLL_USB | Table 5-14 (Type B) | Yes |
| DPLL_USB_OTG_SS | Table 5-14 (Type B) | No ⁽²⁾ |
| DPLL_DEBUGSS | Table 5-13 (Type A) | No ⁽²⁾ |
| DPLL_IVA | Table 5-13 (Type A) | Yes ⁽¹⁾ |
| DPLL_MPU | Table 5-13 (Type A) | Yes ⁽¹⁾ |

(1) DPLL is in the always-on domain.

(2) DPLL is not controlled by the PRCM.

Table 5-13 and Table 5-14 summarize the DPLL characteristics and assume testing over recommended operating conditions.

Table 5-13. DPLL_CORE / DPLL_PER / DPLL_MPU / DPLL_IVA / DPLL_ABE / DPLL_DEBUGSS / DPLL_DSI1_A / DPLL_DSI1_C Characteristics—Type A

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT | COMMENTS |
|-------------------------|--|-------------------|------|---------------------|------|---|
| vdda_dpll_mpu | Supply voltage for DPLL MPU | 1.71 | 1.80 | 1.89 | V | |
| vdda_dpll_mm_l4per | Supply voltage for DPLL IVA | 1.71 | 1.80 | 1.89 | V | |
| vdda_dpll_core_emu_abe | Supply voltage for DPLL CORE | 1.71 | 1.80 | 1.89 | V | |
| vdda_dpll_mm_l4per | Supply voltage for DPLL PER | 1.71 | 1.80 | 1.89 | V | |
| vdda_dpll_core_emu_abe | Supply voltage for DPLL ABE | 1.71 | 1.80 | 1.89 | V | |
| vdda_dsiportA | Supply voltage for DPLL DSI Port A, DSI1_A | 1.71 | 1.80 | 1.89 | V | |
| vdda_dsiportC | Supply voltage for DPLL DSI Port C, DSI1_C | 1.71 | 1.80 | 1.89 | V | |
| vdda_dpll_core_emu_abe | Supply voltage for DPLL DEBUGSS | 1.71 | 1.80 | 1.89 | V | |
| f _{input} | CLKINP input frequency | 0.032 | | 52 | MHz | F _{INP} |
| f _{internal} | Internal reference frequency | 0.032 | | 52 | MHz | REFCLK |
| f _{CLKINPHIF} | CLKINPHIF input frequency | 20 | | 1400 | MHz | F _{INPHIF} |
| f _{CLKINPULOW} | CLKINPULOW input frequency | 0.001 | | 600 | MHz | Bypass mode: f _{CLKOUT} = f _{CLKINPULOW} / (M1 + 1) if ulowclken = 1 ⁽⁶⁾ |
| f _{CLKOUT} | CLKOUT output frequency | 20 ⁽¹⁾ | | 1400 ⁽²⁾ | MHz | [M / (N + 1)] × F _{INP} × [1 / M2] (in locked condition) |
| f _{CLKOUTx2} | CLKOUTx2 output frequency | 40 ⁽¹⁾ | | 2800 ⁽²⁾ | MHz | 2 × [M / (N + 1)] × F _{INP} × [1 / M2] (in locked condition) |
| f _{CLKOUTHIF} | CLKOUTHIF output frequency | 20 ⁽³⁾ | | 1400 ⁽⁴⁾ | MHz | F _{INPHIF} / M3 if clkinphifsel = 1 |
| | | 40 ⁽³⁾ | | 2800 ⁽⁴⁾ | | 2 × [M / (N + 1)] × F _{INP} × [1 / M3] if if clkinphifsel = 0 |
| f _{CLKDCOLDO} | DCOCLKLDO output frequency | 40 | | 2400 | MHz | 2 × [M / (N + 1)] × F _{INP} (in locked condition) |
| t _{lock} | Frequency lock time | | | 5 + 350 × REFCLK | μs | |
| p _{lock} | Phase lock time | | | 5 + 500 × REFCLK | μs | |
| t _{relock-L} | Relock time—Frequency lock ⁽⁵⁾ (LP relock time from bypass) | | | 5 + 70 × REFCLK | μs | DPLL in LP relock time: lowcurrstdby = 1 |
| p _{relock-L} | Relock time—Phase lock ⁽⁵⁾ (LP relock time from bypass) | | | 5 + 120 × REFCLK | μs | DPLL in LP relock time: lowcurrstdby = 1 |
| t _{relock-F} | Relock time—Frequency lock ⁽⁵⁾ (fast relock time from bypass) | | | 2.55 + 70 × REFCLK | μs | DPLL in fast relock time: lowcurrstdby = 0 |
| p _{relock-F} | Relock time—Phase lock ⁽⁵⁾ (fast relock time from bypass) | | | 2.55 + 120 × REFCLK | μs | DPLL in fast relock time: lowcurrstdby = 0 |

(1) The minimum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

For M2 > 1, the minimum frequency on these clocks will further scale down by factor of M2.

(2) The maximum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

(3) The minimum frequency on CLKOUTHIF is assuming M3 = 1. For M3 > 1, the minimum frequency on this clock will further scale down by factor of M3.

(4) The maximum frequency on CLKOUTHIF is assuming M3 = 1.

(5) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

(6) Bypass mode: f_{CLKOUT} = F_{INP} if ulowclken = 0. For more information, see the Device TRM.

Table 5-14. DPLL_USB / DPLL_USB_OTG_SS / DPLL_SATA / DPLL_HDMI Characteristics—Type B

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT | COMMENTS |
|-------------------------|--|------------------------|------|------------------------|------|---|
| vdds_usbhs18 | Supply voltage for DPLL USB | 1.71 | 1.80 | 1.89 | V | |
| vdda_dpll_hdmi | Supply voltage for DPLL HDMI | 1.71 | 1.80 | 1.89 | V | |
| vdda_usbss18 | Supply voltage for DPLL USB SS | 1.71 | 1.80 | 1.89 | V | |
| vdda_sata | Supply voltage for DPLL SATA | 1.71 | 1.80 | 1.89 | V | |
| f _{input} | CLKINP input clock frequency | 0.62 | | 60 | MHz | F _{INP} |
| f _{internal} | REFCLK internal reference clock frequency | 0.62 | | 2.5 | MHz | [1 / (N + 1)] × F _{INP} |
| f _{CLKINPULOW} | CLKINPULOW bypass input clock frequency | 0.001 | | 600 | MHz | Bypass mode: f _{CLKOUT} = f _{CLKINPULOW} / (M1 + 1) if ulowclken = 1 ⁽⁴⁾ |
| f _{CLKLDOOUT} | CLKOUTLDO output clock frequency | 750 ⁽¹⁾⁽⁵⁾ | | 1500 ⁽²⁾⁽⁵⁾ | MHz | M / (N + 1)] × F _{INP} × [1 / M2] (in locked condition) |
| | | 1250 ⁽¹⁾⁽⁵⁾ | | 2500 ⁽²⁾⁽⁵⁾ | MHz | |
| f _{CLKOUT} | CLKOUT output clock frequency | 750 ⁽¹⁾⁽⁵⁾ | | 1500 ⁽²⁾⁽⁵⁾ | MHz | [M / (N + 1)] × F _{INP} × [1 / M2] (in locked condition) |
| | | 1250 ⁽¹⁾⁽⁵⁾ | | 2500 ⁽²⁾⁽⁵⁾ | MHz | |
| f _{CLKDCOLDO} | Internal oscillator (DCO) output clock frequency | 750 ⁽⁵⁾ | | 1500 ⁽⁵⁾ | MHz | [M / (N + 1)] × F _{INP} (in locked condition) |
| | | 1250 ⁽⁵⁾ | | 2500 ⁽⁵⁾ | | |
| t _j | CLKOUTLDO period jitter | –2.5% | | 2.5% | | The period jitter at the output clocks is ± 2.5% peak to peak |
| | CLKOUT period jitter | | | | | |
| | CLKDCOLDO period jitter | | | | | |
| t _{lock} | Frequency lock time | | | 350 × REFCLKs | μs | |
| p _{lock} | Phase lock time | | | 500 × REFCLKs | μs | |
| t _{relock-L} | Relock time—Frequency lock ⁽³⁾ (LP relock time from bypass) | | | 9 + 30 × REFCLKs | μs | |
| p _{relock-L} | Relock time—Phase lock ⁽³⁾ (LP relock time from bypass) | | | 9 + 125 × REFCLKs | μs | |

(1) The minimum frequency on CLKOUT is assuming M2 = 1.

For M2 > 1, the minimum frequency on this clock will further scale down by factor of M2.

(2) The maximum frequency on CLKOUT is assuming M2 = 1.

(3) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

(4) Bypass mode: f_{CLKOUT} = F_{INP} if ULOWCLKEN = 0. For more information, see the Device TRM.

(5) For output clocks, there are two frequency ranges according to the SELFREQDCO setting. For more information, see the Device TRM.

5.2.2.2 DLL Characteristics

Table 5-15 summarizes the DLL characteristics and assumes testing over recommended operating conditions.

Table 5-15. DLL Characteristics

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|--------------|--|-----|-----|-----|--------|
| f_{input} | Input clock frequency | | | 266 | MHz |
| t_{lock} | Lock time | | | 50k | cycles |
| t_{relock} | Relock time (a change of the DLL frequency implies that DLL must relock) | | | 50k | cycles |

(1) See Section 4.3 for values. OPP voltage values may change following the silicon characterization result.

5.2.2.3 DPLL and DLL Noise Isolation

NOTE

For more information on DPLL and DLL decoupling capacitor requirements, see the External Capacitors / Voltage Decoupling Capacitors / I/O and Analog Voltage Decoupling / VDDA Power Domain section.

5.2.3 DPLLs Preferred Settings

5.2.3.1 DPLL_PER Preferred Settings

In the following tables preferred settings for DPLL_PER are presented for different frequencies of SYS_CLK clock.

For SYS_CLK = 38.4 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x7), the DPLL_PER preferred settings are:

Table 5-16. DPLL_PER Preferred Settings for SYS_CLK = 38.4 MHz

| CORE OPPs | | PER DPLL (ADPLL M) | | | Peripheral clocks | | | | | | | | | |
|-----------|------------------------|--------------------|---|----|---------------------|-----------------|----|------------------------------|-------|-----------------------------|-------|-----------------------|-------|---------------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | FUNC_96M_A ON (MHz) | FUNC_192M (MHz) | M3 | PER_DPLL_SCRM Max Freq (MHz) | H11+1 | FUNC_256M Actual Freq (MHz) | H12+1 | DSS Actual Freq (MHz) | H14+1 | PER_GPU Actual Freq (MHz) |
| NOM | 768 | 10 | 0 | 4 | 96 | 192 | 3 | 256 | 3 | 256 | 4 | 192 | 2 | 384 |

For SYS_CLK = 26 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x5), the DPLL_PER preferred settings are:

Table 5-17. DPLL_PER Preferred Settings for SYS_CLK = 26 MHz

| CORE OPPs | | PER DPLL (ADPLL M) | | | Peripheral clocks | | | | | | | | | |
|-----------|------------------------|--------------------|----|----|---------------------|-----------------|----|-------------------------------|-------|-----------------------------|-------|-----------------------|-------|---------------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | FUNC_96M_A ON (MHz) | FUNC_192M (MHz) | M3 | PER_DPLL_S CRM Max Freq (MHz) | H11+1 | FUNC_256M Actual Freq (MHz) | H12+1 | DSS Actual Freq (MHz) | H14+1 | PER_GPU Actual Freq (MHz) |
| NOM | 768 | 192 | 12 | 4 | 96 | 192 | 3 | 256 | 3 | 256 | 4 | 192 | 2 | 384 |

For SYS_CLK = 19.2 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x4), the DPLL_PER preferred settings are:

Table 5-18. DPLL_PER Preferred Settings for SYS_CLK = 19.2 MHz

| CORE OPPs | | PER DPLL (ADPLL M) | | | Peripheral clocks | | | | | | | | | |
|-----------|------------------------|--------------------|---|----|---------------------|-----------------|----|------------------------------|-------|-----------------------------|-------|-----------------------|-------|---------------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | FUNC_96M_A ON (MHz) | FUNC_192M (MHz) | M3 | PER_DPLL_SCRM Max Freq (MHz) | H11+1 | FUNC_256M Actual Freq (MHz) | H12+1 | DSS Actual Freq (MHz) | H14+1 | PER_GPU Actual Freq (MHz) |
| NOM | 768 | 20 | 0 | 4 | 96 | 192 | 3 | 256 | 3 | 256 | 4 | 192 | 2 | 384 |

For SYS_CLK = 16.8 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x3), the DPLL_PER preferred settings are:

Table 5-19. DPLL_PER Preferred Settings for SYS_CLK = 16.8 MHz

| CORE OPPs | PER DPLL (ADPLL M) | | | Peripheral clocks | | | | | | | | | | |
|-----------|------------------------|-----|---|-------------------|---------------------|-----------------|----|-------------------------------|--------|-----------------------------|--------|-----------------------|-------|---------------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | FUNC_96M_A ON (MHz) | FUNC_192M (MHz) | M3 | PER_DPLL_SCR M Max Freq (MHz) | H11+ 1 | FUNC_256M Actual Freq (MHz) | H12+ 1 | DSS Actual Freq (MHz) | H14+1 | PER_GPU Actual Freq (MHz) |
| NOM | 768 | 160 | 6 | 4 | 96 | 192 | 3 | 256 | 3 | 256 | 4 | 192 | 2 | 384 |

For SYS_CLK = 12 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x1), the DPLL_PER preferred settings are:

Table 5-20. DPLL_PER Preferred Settings for SYS_CLK = 12 MHz

| CORE OPPs | PER DPLL (ADPLL M) | | | Peripheral clocks | | | | | | | | | | |
|-----------|------------------------|----|---|-------------------|---------------------|-----------------|----|-------------------------------|--------|-----------------------------|--------|-----------------------|--------|---------------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | FUNC_96M_AO N (MHz) | FUNC_192M (MHz) | M3 | PER_DPLL_S CRM Max Freq (MHz) | H11+ 1 | FUNC_256M Actual Freq (MHz) | H12+ 1 | DSS Actual Freq (MHz) | H14+ 1 | PER_GPU Actual Freq (MHz) |
| NOM | 768 | 32 | 0 | 4 | 96 | 192 | 3 | 256 | 3 | 256 | 4 | 192 | 2 | 384 |

5.2.3.2 DPLL_CORE Preferred Settings

Regarding DPLL_CORE settings for all SYS_CLK frequencies, following notes are valid:

1. DPLL may also be used in bypass mode (ex: MP3 usecase)

For SYS_CLK = 38.4 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x7), the DPLL_CORE preferred settings are:

Table 5-21. DPLL_CORE Preferred Settings for SYS_CLK = 38.4 MHz (Table 1)

| CORE OPPs | CORE DPLL (ADPLL M) | | | CORE clocks | | | | | | |
|-----------|------------------------|-----|---|-------------|----------------------------|----|-------------------------------|-------|----------------------------|--|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | EMIF_PHY Actual Freq (MHz) | M3 | CORE_DPLL_SCRM Max Freq (MHz) | H11+1 | CORE_DLL Actual Freq (MHz) | |
| NOM | 2127,4 | 277 | 9 | 2 | 531,8 | 5 | 425,5 | 8 | 265,9 | |

Table 5-22. DPLL_CORE Preferred Settings for SYS_CLK = 38.4 MHz (Table 2)

| CORE OPPs | CORE clocks | | | | | | | | | | | | | |
|-----------|-------------|---------------------------|-------|--------------------------------|---------------|----------------------------|-------|--------------------------------|-------|--------------------------------------|-------|------------------------------|-------|------------------------------|
| OPPs | H12+1 | CORE_X2 Actual Freq (MHz) | H13+1 | CORE_USB_OTG_SS Max Freq (MHz) | H14+1 | CORE_GPU Actual Freq (MHz) | H21+1 | CORE_C2C_CLK Actual Freq (MHz) | H22+1 | CORE_IPU_ISS_BOOST Actual Freq (MHz) | H23+1 | CORE_ISS_MAIN Max Freq (MHz) | H24+1 | BB2D_GFCLK Actual Freq (MHz) |
| NOM | 4 | 531,8 | 62 | 34,3 | 63(1) or 2(2) | 425.6(1) or 532(2) | 6 | 354,6 | 5 | 425,5 | 7 | 303,9 | 6 | 354,6 |

(1) When VD_MM at OPP_NOM

(2) When VD_MM at OPP_OD

For SYS_CLK = 26 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x5), the DPLL_CORE preferred settings are:

Table 5-23. DPLL_CORE Preferred Settings for SYS_CLK = 26 MHz (Table 1)

| CORE OPPs | CORE DPLL (ADPLLM) | | | CORE clocks | | | | | | |
|-----------|------------------------|-----|---|-------------|----------------------------|----|-------------------------------|-------|----------------------------|--|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | EMIF_PHY Actual Freq (MHz) | M3 | CORE_DPLL_SCRM Max Freq (MHz) | H11+1 | CORE_DLL Actual Freq (MHz) | |
| NOM | 2126,2 | 368 | 8 | 2 | 5316 | 5 | 425,2 | 8 | 265,8 | |

Table 5-24. DPLL_CORE Preferred Settings for SYS_CLK = 26 MHz (Table 2)

| CORE OPPs | CORE clocks | | | | | | | | | | | | | |
|-----------|-------------|---------------------------|-------|--------------------------------|---------------|----------------------------|-------|--------------------------------|-------|--------------------------------------|-------|------------------------------|-------|------------------------------|
| OPPs | H12+1 | CORE_X2 Actual Freq (MHz) | H13+1 | CORE_USB_OTG_SS Max Freq (MHz) | H14+1 | CORE_GPU Actual Freq (MHz) | H21+1 | CORE_C2C_CLK Actual Freq (MHz) | H22+1 | CORE_IPU_ISS_BOOST Actual Freq (MHz) | H23+1 | CORE_ISS_MAIN Max Freq (MHz) | H24+1 | BB2D_GFCLK Actual Freq (MHz) |
| NOM | 4 | 531,6 | 62 | 34,3 | 63(1) or 2(2) | 425.6(1) or 532(2) | 6 | 354,4 | 5 | 425,2 | 7 | 303,7 | 6 | 354,4 |

(1) When VD_MM at OPP_NOM

(2) When VD_MM at OPP_OD

For SYS_CLK = 19.2 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x4) the DPLL_CORE preferred settings are:

Table 5-25. DPLL_CORE Preferred Settings for SYS_CLK = 19.2 MHz (Table 1)

| CORE OPPs | CORE DPLL (ADPLL M) | | | CORE clocks | | | | | |
|-----------|------------------------|-----|---|-------------|----------------------------|----|-------------------------------|-------|----------------------------|
| | DPLL locked Freq (MHz) | M | N | M2 | EMIF_PHY Actual Freq (MHz) | M3 | CORE_DPLL_SCRM Max Freq (MHz) | H11+1 | CORE_DLL Actual Freq (MHz) |
| NOM | 2127,4 | 277 | 4 | 2 | 531,8 | 5 | 425,5 | 8 | 265,92 |

Table 5-26. DPLL_CORE Preferred Settings for SYS_CLK = 19.2 MHz (Table 2)

| CORE OPPs | CORE clocks | | | | | | | | | | | | | |
|-----------|-------------|---------------------------|-------|--------------------------------|---------------|----------------------------|-------|--------------------------------|-------|--------------------------------------|-------|------------------------------|-------|------------------------------|
| | H12+1 | CORE_X2 Actual Freq (MHz) | H13+1 | CORE_USB_OTG_SS Max Freq (MHz) | H14+1 | CORE_GPU Actual Freq (MHz) | H21+1 | CORE_C2C_CLK Actual Freq (MHz) | H22+1 | CORE_IPU_ISS_BOOST Actual Freq (MHz) | H23+1 | CORE_ISS_MAIN Max Freq (MHz) | H24+1 | BB2D_GFCLK Actual Freq (MHz) |
| NOM | 4 | 531,8 | 62 | 34,3 | 63(1) or 2(2) | 425,6(1) or 532(2) | 6 | 354,6 | 5 | 425,5 | 7 | 303,9 | 6 | 354,6 |

(1) When VD_MM at OPP_NOM

(2) When VD_MM at OPP_OD

For SYS_CLK = 16.8 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x3), the DPLL_CORE preferred settings are:

Table 5-27. DPLL_CORE Preferred Settings for SYS_CLK = 16.8 MHz (Table 1)

| CORE OPPs | CORE DPLL (ADPLL M) | | | CORE clocks | | | | | | |
|-----------|------------------------|-----|---|-------------|----------------------------|----|-------------------------------|-------|----------------------------|--|
| | DPLL locked Freq (MHz) | M | N | M2 | EMIF_PHY Actual Freq (MHz) | M3 | CORE_DPLL_SCRM Max Freq (MHz) | H11+1 | CORE_DLL Actual Freq (MHz) | |
| NOM | 2126,4 | 443 | 6 | 2 | 531,6 | 5 | 425,3 | 8 | 265,8 | |

Table 5-28. DPLL_CORE Preferred Settings for SYS_CLK = 16.8 MHz (Table 2)

| CORE OPPs | CORE clocks | | | | | | | | | | | | | |
|-----------|-------------|---------------------------|-------|--------------------------------|---------------|----------------------------|-------|--------------------------------|-------|--------------------------------------|-------|------------------------------|-------|------------------------------|
| | H12+1 | CORE_X2 Actual Freq (MHz) | H13+1 | CORE_USB_OTG_SS Max Freq (MHz) | H14+1 | CORE_GPU Actual Freq (MHz) | H21+1 | CORE_C2C_CLK Actual Freq (MHz) | H22+1 | CORE_IPU_ISS_BOOST Actual Freq (MHz) | H23+1 | CORE_ISS_MAIN Max Freq (MHz) | H24+1 | BB2D_GFCLK Actual Freq (MHz) |
| NOM | 4 | 531,6 | 62 | 34,3 | 63(1) or 2(2) | 425,6(1) or 532(2) | 6 | 354,4 | 5 | 425,3 | 7 | 303,8 | 6 | 354,4 |

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- (1) When VD_MM at OPP_NOM
 (2) When VD_MM at OPP_OD

For SYS_CLK = 12 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x1), the DPLL_CORE preferred settings are:

Table 5-29. DPLL_CORE Preferred Settings for SYS_CLK = 12 MHz (Table 1)

| CORE OPPs | CORE DPLL (ADPLL_M) | | | CORE clocks | | | | | |
|-----------|------------------------|-----|---|-------------|----------------------------|----|-------------------------------|-------|----------------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | EMIF_PHY Actual Freq (MHz) | M3 | CORE_DPLL_SCRM Max Freq (MHz) | H11+1 | CORE_DLL Actual Freq (MHz) |
| NOM | 2128 | 266 | 2 | 2 | 532 | 5 | 425,6 | 8 | 266 |

Table 5-30. DPLL_CORE Preferred Settings for SYS_CLK = 12 MHz (Table 2)

| CORE OPPs | CORE clocks | | | | | | | | | | | | | | | |
|-----------|-------------|-----------------------------|--------|----------------------------|--------|---------------------------------|---------------|-----------------------------|-------|---------------------------------|-------|--------------------------------------|--------|------------------------------|-------|------------------------------|
| OPPs | H1 1+1 | CORE_DL L Actual Freq (MHz) | H12+ 1 | CORE_X 2 Actual Freq (MHz) | H13+ 1 | CORE_US B_OTG_SS Max Freq (MHz) | H14+ 1 | CORE_GP U Actual Freq (MHz) | H21+1 | CORE_C2 C_CLK Actual Freq (MHz) | H22+1 | CORE_IPU_ISS_BOOST Actual Freq (MHz) | H23+ 1 | CORE_ISS_MAIN Max Freq (MHz) | H24+1 | BB2D_GFCLK Actual Freq (MHz) |
| NOM | 8 | 266 | 4 | 532 | 62 | 34,3 | 63(1) or 2(2) | 425.6(1) or 532(2) | 6 | 354,7 | 5 | 425,6 | 7 | 304 | 6 | 354,7 |

- (1) When VD_MM at OPP_NOM
 (2) When VD_MM at OPP_OD

NOTE

To provide 532MHz clock frequency to GPU module with DPLL_CORE locked at 2128 MHz, it must configure value of 0x3F in CM_DIV_H14_DPLL_CORE[0:5] DIVHS bitfield. For other ratio, it must program ratio divided by 2 compared to other HSDIVIDER.

5.2.3.3 DPLL_ABE Preferred Settings

Regarding DPLL_ABE settings for all SYS_CLK frequencies, following notes are valid:

1. This DPLL uses SYS_32K clock as clock input (32768 Hz) and REGM4XEN=1

The following [Table 5-31](#) represents the preferred settings identical for all SYS_CLK frequencies as follows:

1. For SYS_CLK = 38.4 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x7)

2. For SYS_CLK = 26 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x5)
3. For SYS_CLK = 19.2 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x4)
4. For SYS_CLK = 16.8 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x3)
5. For SYS_CLK = 12 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x1)

Table 5-31. DPLL_ABE Preferred Settings for SYS_CLK = 38.4, 26, 19.2, 16.8 & 12 MHz

| CORE OPPs | ABE DPLL (ADPLL M) | | | ABE clocks | | | |
|-----------|------------------------|-----|---|------------|--|----|--------------------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | DPLL_ABE_X2 Actual Freq (MHz) - M2X2 o/p | M3 | CORE_DPLL_HS Actual Freq (MHz) |
| NOM | 196,608 | 750 | 0 | 1 | 196,608 | 1 | 196,608 |

5.2.3.4 DPLL_MPU Preferred Settings

Regarding DPLL_MPU settings for all SYS_CLK frequencies, following notes are valid:

1. BLOCKID5 = 1 when MPU required frequency is > 1.4GHz (Controlled through CM_CLKSEL_DPLL_MPU.DCC_EN).
2. DPLL may also be used in bypass mode (ex: boot, MP3 usecase).

For SYS_CLK = 38.4 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x7), the DPLL_MPU preferred settings are:

Table 5-32. DPLL_MPU Preferred Settings for SYS_CLK = 38.4 MHz

| MPU OPPs | MPU DPLL (ADPLL M) | | | MPU | |
|----------|------------------------|-----|----|-----|-----------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | MPU Actual Freq (MHz) |
| HIGH | 1500 | 625 | 15 | 1 | 1500 |
| NOM | 2000 | 625 | 23 | 1 | 1000 |

For SYS_CLK = 26 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x5), the DPLL_MPU preferred settings are:

Table 5-33. DPLL_MPU Preferred Settings for SYS_CLK = 26 MHz

| MPU OPPs | MPU DPLL (ADPLL M) | | | MPU | |
|----------|------------------------|-----|----|-----|-----------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | MPU Actual Freq (MHz) |
| HIGH | 1499,3 | 173 | 2 | 1 | 1499,3 |
| NOM | 2000 | 500 | 12 | 1 | 1000 |

For SYS_CLK = 19.2 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x4), the DPLL_MPU preferred settings are:

Table 5-34. DPLL_MPU Preferred Settings for SYS_CLK = 19.2 MHz

| MPU OPPs | MPU DPLL (ADPLL M) | | | MPU | |
|----------|------------------------|-----|----|-----|-----------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | MPU Actual Freq (MHz) |
| HIGH | 1500 | 625 | 7 | 1 | 1500 |
| NOM | 2000 | 625 | 11 | 1 | 1000 |

For SYS_CLK = 16.8 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x3), the DPLL_MPU preferred settings are:

Table 5-35. DPLL_MPU Preferred Settings for SYS_CLK = 16.8 MHz

| MPU OPPs | MPU DPLL (ADPLL M) | | | MPU | |
|----------|------------------------|------|----|-----|-----------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | MPU Actual Freq (MHz) |
| HIGH | 1499,4 | 357 | 3 | 1 | 1499,4 |
| NOM | 2000 | 1250 | 20 | 1 | 1000 |

For SYS_CLK = 12 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x1), the DPLL_MPU preferred settings are:

Table 5-36. DPLL_MPU Preferred Settings for SYS_CLK = 12 MHz

| MPU OPPs | MPU DPLL (ADPLL M) | | | MPU | |
|----------|------------------------|-----|---|-----|-----------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | MPU Actual Freq (MHz) |
| HIGH | 1500 | 125 | 0 | 1 | 1500 |
| NOM | 2000 | 250 | 2 | 1 | 1000 |

5.2.3.5 DPLL_IVA Preferred Settings

Regarding DPLL_IVA settings for all SYS_CLK frequencies, following notes are valid:

1. DPLL may also be used in bypass mode (ex: boot, MP3 usecase).

For SYS_CLK = 38.4 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x7), the DPLL_IVA preferred settings are:

Table 5-37. DPLL_IVA Preferred Settings for SYS_CLK = 38.4 MHz

| MM OPPs | IVA DPLL (ADPLL M) | | | MM clocks | | | | |
|---------|--------------------|------------------------|----|-----------|-------|-----------------------|-------|-----------------------|
| | OPPs | DPLL locked Freq (MHz) | M | N | H11+1 | DSP Actual Freq (MHz) | H12+1 | IVA Actual Freq (MHz) |
| OD | | 1062,4 | 83 | 5 | 2 | 531,2 | 2 | 531,2 |
| NOM | | 2330 | 91 | 2 | 5 | 465,9 | 6 | 388,3 |

For SYS_CLK = 26 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x5), the DPLL_IVA preferred settings are:

Table 5-38. DPLL_IVA Preferred Settings for SYS_CLK = 26 MHz

| MM OPPs | IVA DPLL (ADPLL M) | | | MM clocks | | | | |
|---------|--------------------|------------------------|-----|-----------|-------|-----------------------|-------|-----------------------|
| | OPPs | DPLL locked Freq (MHz) | M | N | H11+1 | DSP Actual Freq (MHz) | H12+1 | IVA Actual Freq (MHz) |
| OD | | 1062,3 | 143 | 6 | 2 | 531,1 | 2 | 531,1 |
| NOM | | 2330 | 224 | 4 | 5 | 465,92 | 6 | 388,3 |

For SYS_CLK = 19.2 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x4), the DPLL_IVA preferred settings are:

Table 5-39. DPLL_IVA Preferred Settings for SYS_CLK = 19.2 MHz

| MM OPPs | IVA DPLL (ADPLL M) | | | MM clocks | | | | |
|---------|--------------------|------------------------|-----|-----------|-------|-----------------------|-------|-----------------------|
| | OPPs | DPLL locked Freq (MHz) | M | N | H11+1 | DSP Actual Freq (MHz) | H12+1 | IVA Actual Freq (MHz) |
| OD | | 1062,4 | 83 | 2 | 2 | 531,2 | 2 | 531,2 |
| NOM | | 2330 | 182 | 2 | 5 | 465,9 | 6 | 388,3 |

For SYS_CLK = 16.8 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x3), the DPLL_IVA preferred settings are:

Table 5-40. DPLL_IVA Preferred Settings for SYS_CLK = 16.8 MHz

| MM OPPs | IVA DPLL (ADPLL M) | | | MM clocks | | | | |
|---------|--------------------|------------------------|-----|-----------|-------|-----------------------|-------|-----------------------|
| | OPPs | DPLL locked Freq (MHz) | M | N | H11+1 | DSP Actual Freq (MHz) | H12+1 | IVA Actual Freq (MHz) |
| OD | | 1062,6 | 253 | 7 | 2 | 531,3 | 2 | 531,3 |
| NOM | | 2330 | 208 | 2 | 5 | 465,9 | 6 | 388,3 |

For SYS_CLK = 12 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x1), the DPLL_IVA preferred settings are:

Table 5-41. DPLL_IVA Preferred Settings for SYS_CLK = 12 MHz

| MM OPPs | IVA DPLL (ADPLLM) | | | MM clocks | | | |
|---------|------------------------|------|----|-----------|-----------------------|-------|-----------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | H11+1 | DSP Actual Freq (MHz) | H12+1 | IVA Actual Freq (MHz) |
| OD | 1064 | 133 | 2 | 2 | 532 | 2 | 532 |
| NOM | 2330 | 1165 | 11 | 5 | 466 | 6 | 388,3 |

5.2.3.6 DPLL_USB Preferred Settings

Regarding DPLL_USB settings for all SYS_CLK frequencies, following notes are valid:

1. SELFREQDCO[2:0] = 010, required frequency is < 1.5GHz

For SYS_CLK = 38.4 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x7), the DPLL_USB preferred settings are:

Table 5-42. DPLL_USB Preferred Settings for SYS_CLK = 38.4 MHz

| CORE OPPs | USB DPLL (ADPLLLJM) | | | USB | |
|-----------|------------------------|-----|----|-----|-------------------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | L3INIT_480M Actual Freq (MHz) |
| NOM | 960 | 400 | 15 | 2 | 480 |

For SYS_CLK = 26 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x5), the DPLL_USB preferred settings are:

Table 5-43. DPLL_USB Preferred Settings for SYS_CLK = 26 MHz

| CORE OPPs | USB DPLL (ADPLLLJM) | | | USB | |
|-----------|------------------------|-----|----|-----|-------------------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | L3INIT_480M Actual Freq (MHz) |
| NOM | 960 | 480 | 12 | 2 | 480 |

For SYS_CLK = 19.2 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x4), the DPLL_USB preferred settings are:

Table 5-44. DPLL_USB Preferred Settings for SYS_CLK = 19.2 MHz

| CORE OPPs | USB DPLL (ADPLLLJM) | | | USB | |
|-----------|------------------------|-----|---|-----|-------------------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | L3INIT_480M Actual Freq (MHz) |
| NOM | 960 | 400 | 7 | 2 | 480 |

For SYS_CLK = 16.8 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x3), the DPLL_USB preferred settings are:

Table 5-45. DPLL_USB Preferred Settings for SYS_CLK = 16.8 MHz

| CORE OPPs | USB DPLL (ADPLLLJM) | | | USB | |
|-----------|------------------------|-----|---|-----|-------------------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | L3INIT_480M Actual Freq (MHz) |
| NOM | 960 | 400 | 6 | 2 | 480 |

For SYS_CLK = 12 MHz (configured in CM_CLKSEL_SYS[2:0] SYS_CLKSEL = 0x1), the DPLL_USB preferred settings are:

Table 5-46. DPLL_USB Preferred Settings for SYS_CLK = 12 MHz

| CORE OPPs | USB DPLL (ADPLLLJM) | | | USB | |
|-----------|------------------------|-----|---|-----|-------------------------------|
| OPPs | DPLL locked Freq (MHz) | M | N | M2 | L3INIT_480M Actual Freq (MHz) |
| NOM | 960 | 400 | 4 | 2 | 480 |

5.2.4 Internal 32-kHz Oscillator

An internal 32-kHz oscillator is implemented in the wake-up domain. [Table 5-47](#) gives the internal 32-kHz oscillator characteristics.

Table 5-47. Internal 32-kHz Oscillator Characteristic

| PARAMETER | MIN | TYP | MAX | UNIT |
|--------------------------------------|-----|-----|-----|------|
| Internal 32-kHz oscillator frequency | 16 | 32 | 60 | kHz |

6 Timing Requirements and Switching Characteristics

NOTE

The OPP (operating performance point) described in this chapter correspond to the OPP of the core domain. The operating point for MPU and multimedia are not described in this section. For more information, see [Section 4.3](#).

6.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.

6.2 Interface Clock Specifications

6.2.1 Interface Clock Terminology

The interface clock is used at the system level to sequence the data and/or to control transfers accordingly with the interface protocol.

6.2.2 Interface Clock Frequency

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the device IC and does not take into account any system consideration (PCB, peripherals).

The system designer will have to consider these system considerations and the device IC timing characteristics as well to define properly the maximum operating frequency that corresponds to the maximum frequency supported to transfer the data on this interface.

6.2.3 Clock Jitter Specifications

Jitter is a phase noise, which may alter different characteristics of a clock signal. The jitter specified in this document is the time difference between the typical cycle period and the actual cycle period affected by noise sources on the clock. The cycle (or period) jitter terminology will be used to identify this type of jitter.

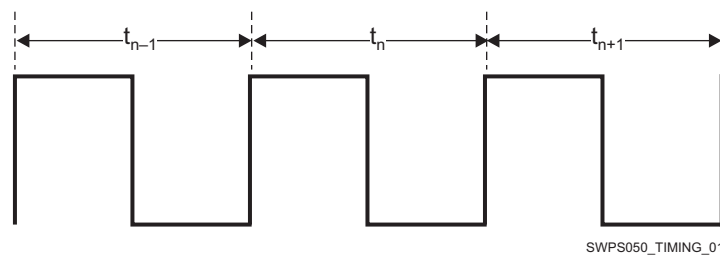


Figure 6-1. Cycle (or Period) Jitter

Jitter values are defined as follows:

- Ideal clock period = t_p
- Maximum Cycle/Period Jitter = $\text{Max} (|t_i - t_p|)$, with $i = n - 1, n, n + 1, \dots$
- Minimum Cycle/Period Jitter = $\text{Min} (|t_i - t_p|)$
- Jitter Standard Deviation (or RMS Jitter) = Standard Deviation ($|t_i - t_p|$)

Unless otherwise specified, the jitter probability density can be approximated by a Gaussian function and peak-to-peak jitter is defined over a ± 7 sigma distribution of this function.

6.2.4 Clock Duty Cycle Error

The maximum duty cycle error is the difference between the absolute value of the maximum high-level pulse duration or the maximum low-level pulse duration and the typical pulse duration value:

- Maximum pulse duration = typical pulse duration + maximum duty cycle error
- Minimum pulse duration = typical pulse duration – maximum duty cycle error

In this document, the clock duty cycle can be documented as maximum pulse duration or as maximum duty cycle error. In this case, you can consider:

- Maximum duty cycle error = maximum [(maximum pulse duration – typical pulse duration) or (typical pulse duration – minimum pulse duration)]

6.3 Timing Parameters

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of pin names and other related terminologies have been abbreviated as follows:

Table 6-1. Timing Parameters

| SUBSCRIPTS | |
|------------|---|
| SYMBOL | PARAMETER |
| c | Cycle time (period) |
| d | Delay time |
| dis | Disable time |
| en | Enable time |
| h | Hold time |
| su | Setup time |
| START | Start bit |
| t | Transition time |
| v | Valid time |
| w | Pulse duration (width) |
| X | Unknown, changing, or do not care level |
| F | Fall time |
| H | High |
| L | Low |
| R | Rise time |
| V | Valid |
| IV | Invalid |
| AE | Active Edge |
| FE | First Edge |
| LE | Last Edge |
| Z | High impedance |

NOTE

The OPP (operating performance point) described in this chapter correspond to the OPP of the core domain. The operating point for MPU and multimedia are not described in this section. For more information, see the DM [Section 4.3](#).

6.4 External Memory Interface

The Device includes the following external memory interfaces:

- General-purpose memory controller (GPMC)
- External memory interface controller (EMIF)

6.4.1 General-Purpose Memory Controller (GPMC), 1.8 V

NOTE

For more information, see the Memory Subsystem and General-Purpose Memory Controller sections of the Device TRM.

The GPMC is the OMAP-unified memory controller that interfaces the following types of external memory devices:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous, synchronous burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

6.4.1.1 NOR Flash, 1.8 V

6.4.1.1.1 NOR Flash, Read synchronous mode, 88.6 MHz

Table 6-2. NOR Flash Timing Conditions — Read Synchronous Mode

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|-------------------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 0.30 | 1.79 | ns |
| t_F | Input signal fall time | 0.33 | 1.84 | ps |
| PCB Conditions⁽¹⁾ | | | | |

(1) See [Table 7-4](#).

(2) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-3](#) and [Table 6-4](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-3. NOR Flash Timing Requirements — Read Synchronous Mode⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| F12 | $t_{SU(dV-clkH)}$ | Setup time, input data gpmc_ad[15:0] valid before output gpmc_clk high | 2.4 | | ns |
| F13 | $t_{H(clkH-dV)}$ | Hold time, input data gpmc_ad[15:0] valid after output gpmc_clk high | 1.1 | | ns |
| F21 | $t_{SU(waitV-clkH)}$ | Setup time, input wait gpmc_waitx ⁽¹⁾ valid before output gpmc_clk high | 2.4 | | ns |
| F22 | $t_{H(clkH-waitV)}$ | Hold time, input wait gpmc_waitx ⁽¹⁾ valid after output gpmc_clk high | 1.1 | | ns |

(1) In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) See [Section 4.3](#) for CORE OPP voltages.

Table 6-4. NOR Flash Switching Characteristics — Read Synchronous Mode⁽¹⁵⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|------------------|--|-----------------------|------|------|
| | | | MIN | MAX | |
| F0 | $1 / t_{C(CLK)}$ | Frequency ⁽¹²⁾ , output gpmc_clk | | 88.6 | MHz |
| F1 | $t_{W(CLKH)}$ | Typical Pulse duration, output gpmc_clk high | 0.5 P ⁽¹⁰⁾ | | ns |

Table 6-4. NOR Flash Switching Characteristics — Read Synchronous Mode⁽¹⁵⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|-----------------------|--|--|-------------------------|------------------------|
| | | | MIN | MAX | |
| F1 | $t_{W(CLKL)}$ | Typical Pulse duration, output gpmc_clk low | 0.5 P ⁽¹⁰⁾ | | ns |
| | $t_{DC(CLK)}$ | Duty cycle error, output gpmc_clk | | 565 | ps |
| | $t_{J(CLK)}$ | Jitter standard deviation ⁽¹³⁾ , output gpmc_clk | | 73.1 | ps |
| | $t_{R(CLK)}$ | Rise time, output gpmc_clk | 0.5 | 1.1 | ns |
| | $t_{F(CLK)}$ | Fall time, output gpmc_clk | 0.5 | 1.1 | ns |
| | $t_{R(DO)}$ | Rise time, output data gpmc_ad[15:0] | 0.5 | 1.4 | ns |
| | $t_{F(DO)}$ | Fall time, output data gpmc_ad[15:0] | 0.5 | 1.4 | ns |
| | F2 | $t_{D(CLKH-nCSV)}$ | Delay time, gpmc_clk rising edge to gpmc_ncsx ⁽⁹⁾ valid | F ⁽⁶⁾ – 0.8 | F ⁽⁶⁾ + 3.1 |
| F3 | $t_{D(CLKH-nCSIV)}$ | Delay time, gpmc_clk rising edge to gpmc_ncsx ⁽⁹⁾ invalid | E ⁽⁵⁾ – 0.8 | E ⁽⁵⁾ + 3.1 | ns |
| F4 | $t_{D(ADDV-CLK)}$ | Delay time, gpmc_a[25:16] address bus valid to gpmc_clk first edge | B ⁽²⁾ – 3.1 | B ⁽²⁾ + 0.8 | ns |
| F5 | $t_{D(CLKH-ADDIV)}$ | Delay time, gpmc_clk rising edge to gpmc_a[25:16] gpmc address bus invalid | -0.8 | | ns |
| F8 | $t_{D(CLKH-nADV)}$ | Delay time, gpmc_clk rising edge to gpmc_nadv_ale valid | G ⁽⁷⁾ – 0.8 | G ⁽⁷⁾ + 3.1 | ns |
| F9 | $t_{D(CLKH-nADVIV)}$ | Delay time, gpmc_clk rising edge to gpmc_nadv_ale invalid | D ⁽⁴⁾ – 0.8 | D ⁽⁴⁾ + 3.1 | ns |
| F10 | $t_{D(CLKH-nOE)}$ | Delay time, gpmc_clk rising edge to gpmc_noe valid | H ⁽⁸⁾ – 0.8 | H ⁽⁸⁾ + 2.1 | ns |
| F11 | $t_{D(CLKH-nOEIV)}$ | Delay time, gpmc rising edge to gpmc_noe invalid | E ⁽⁵⁾ – 0.8 | E ⁽⁵⁾ + 2.1 | ns |
| F18 | $t_{W(nCSV)}$ | Pulse duration, gpmc_ncsx ⁽⁹⁾ low | A ⁽¹⁾ | | ns |
| F19 | $t_{W(nBEV)}$ | Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 low | C ⁽³⁾ | | ns |
| F20 | $t_{W(nADV)}$ | Pulse duration, gpmc_nadv_ale low | K ⁽¹¹⁾ | | ns |
| F23 | $t_{D(CLKH-IODIR)}$ | Delay time, gpmc_clk rising edge to gpmc_io_dir high (IN direction) | H ⁽⁸⁾ – 0.8 | H ⁽⁸⁾ + 2.1 | ns |
| F24 | $t_{D(CLKH-IODIRIV)}$ | Delay time, gpmc rising edge to gpmc_io_dir low (OUT direction) | M ⁽¹⁴⁾ – 0.8 | M ⁽¹⁴⁾ + 2.1 | ns |

(1) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period.

For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period with n the page burst access number.

(2) B = ClkActivationTime * GPMC_FCLK

(3) For single read: C = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK

For burst read: C = (RdCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n the page burst access number.

(4) For single read: D = (RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

For burst read: D = (RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(5) For single read: E = (CSRdOffTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

For burst read: E = (CSRdOffTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(6) For nCS falling edge (CS activated):

Case GpmcFCLKDivider = 0:

F = 0.5 * CSExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:

F = 0.5 * CSExtraDelay * GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)

F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK

otherwise

Case GpmcFCLKDivider = 2:

F = 0.5 * CSExtraDelay * GPMC_FCLK if ((CSOnTime - ClkActivationTime) is a multiple of 3)

F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)

F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):

Case GpmcFCLKDivider = 0:

G = 0.5 * ADVExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:

G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)

G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK

otherwise

Case GpmcFCLKDivider = 2:

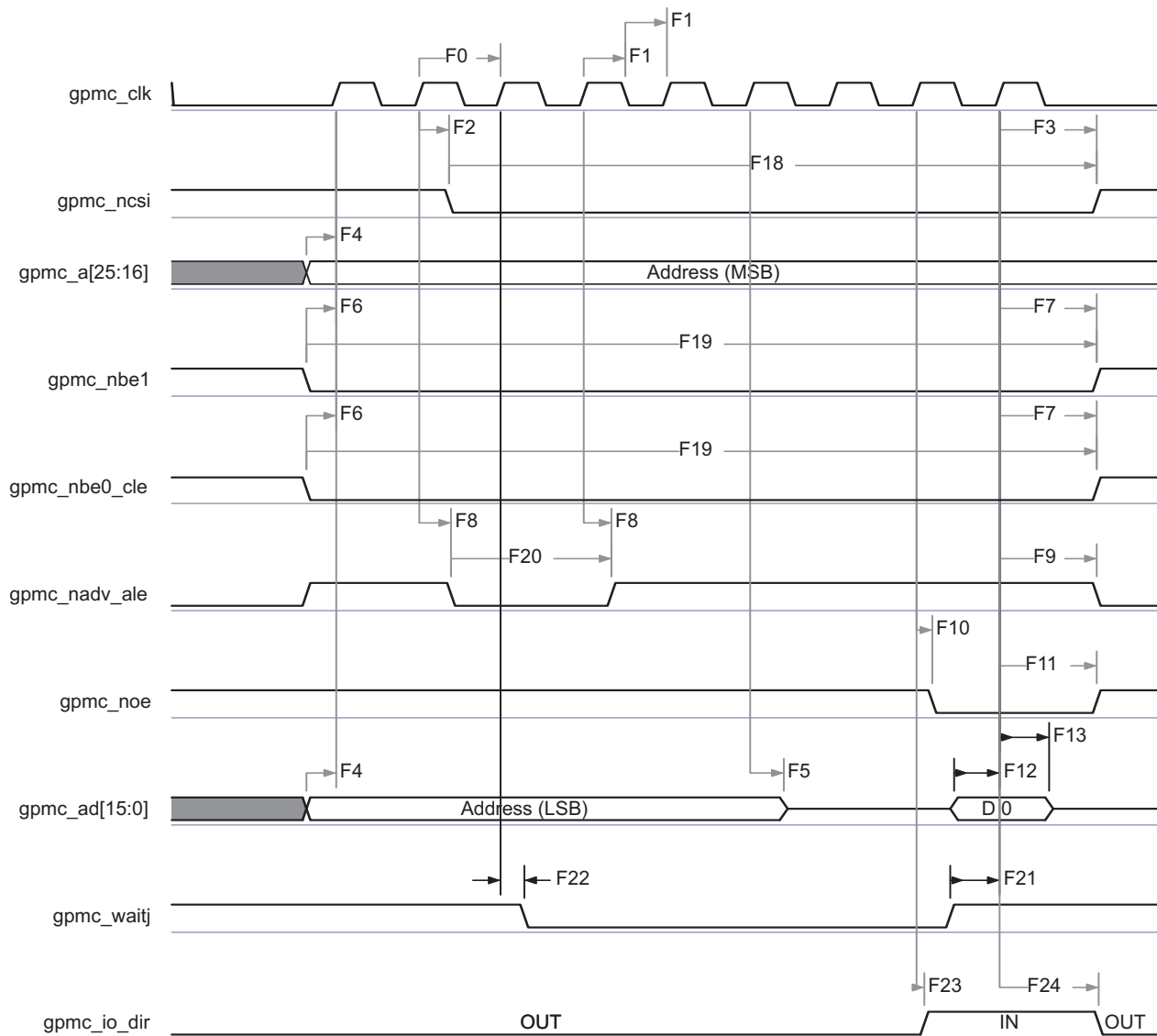
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVOnTime - ClkActivationTime) is a multiple of 3)

G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)

G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

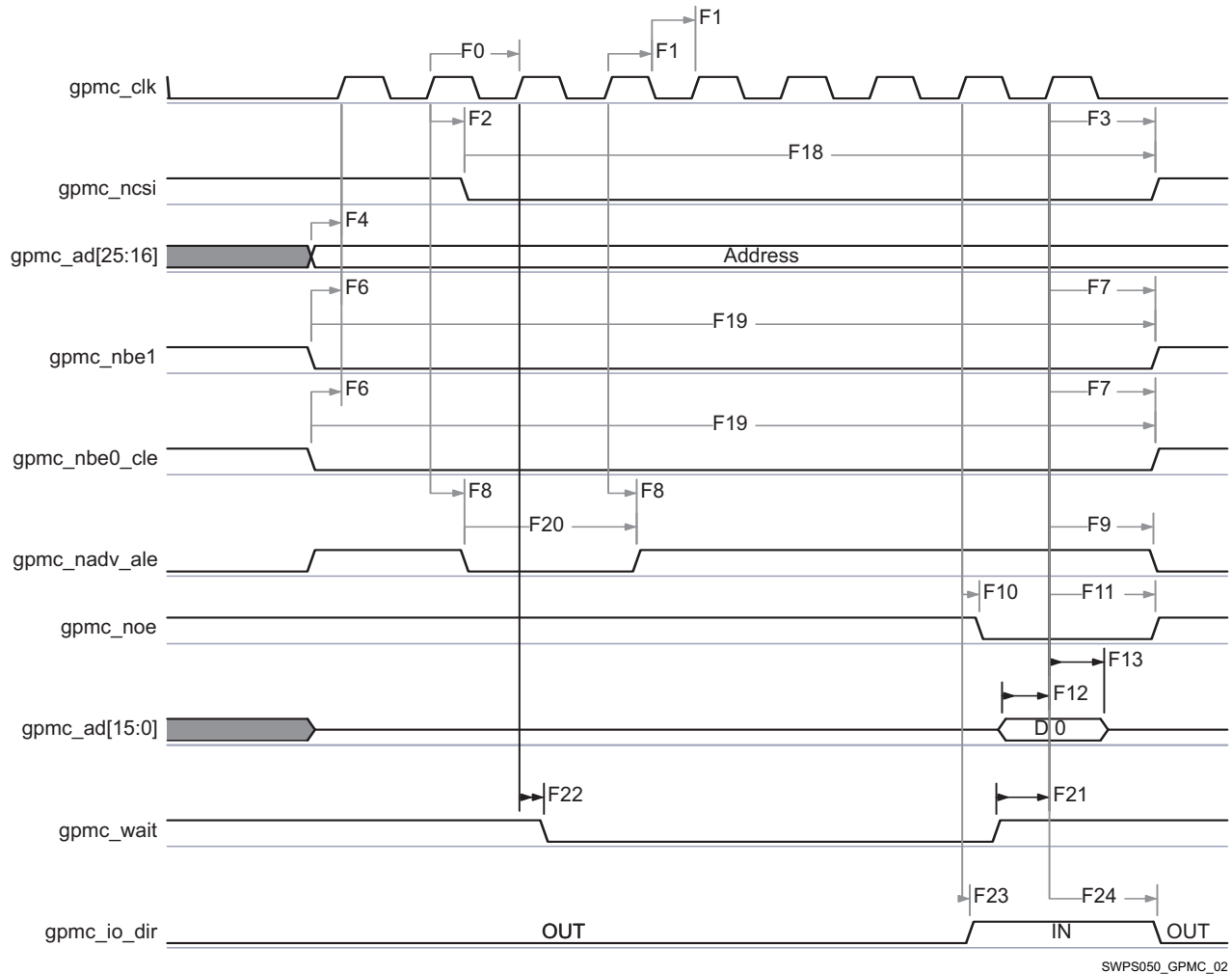
- Case GpmcFCLKDivider = 0:
 $G = 0.5 * ADVExtraDelay * GPMC_FCLK$ Case GpmcFCLKDivider = 1:
 $G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
 $G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ otherwise
 Case GpmcFCLKDivider = 2:
 $G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
 $G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
 $G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)
- (8) For OE falling edge (OE activated) / IO DIR rising edge (IN direction):
 Case GpmcFCLKDivider = 0:
 $H = 0.5 * OEEExtraDelay * GPMC_FCLK$
 Case GpmcFCLKDivider = 1:
 $H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
 $H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ otherwise
 Case GpmcFCLKDivider = 2:
 $H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if ((OEOnTime – ClkActivationTime) is a multiple of 3)
 $H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
 $H = (2 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)
 For OE rising edge (OE deactivated):
 Case GpmcFCLKDivider = 0:
 $H = 0.5 * OEEExtraDelay * GPMC_FCLK$
 Case GpmcFCLKDivider = 1:
 $H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
 $H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ otherwise
 Case GpmcFCLKDivider = 2:
 $H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if ((OEOffTime – ClkActivationTime) is a multiple of 3)
 $H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
 $H = (2 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)
- (9) In “gpmc_ncsx”, x is equal to 0, 1, 2, 3, 4, 5, 6, 7. In “gpmc_waitx”, x is equal to 0, 1, 2, or 3
- (10) P = gpmc_clk period
- (11) For read: $K = (ADVRdOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
- (12) Related to the gpmc_clk output clock Maximum and minimum frequency programmable in I/F module by setting the GPMC_CONFIG1_CSx configuration register bit fields GpmcFCLKDivider
- (13) The jitter probability density can be approximated by a Gaussian function.
- (14) $M = (RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$ Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behaviour of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or non/multiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behaviour is automatically handled by GPMC controller
- (15) See the [Section 4.3](#) for CORE OPP voltages.



SWPS050_GPMC_01

Figure 6-2. GPMC / Multiplexed 16bits NOR Flash – Synchronous Single Read⁽¹⁾⁽²⁾

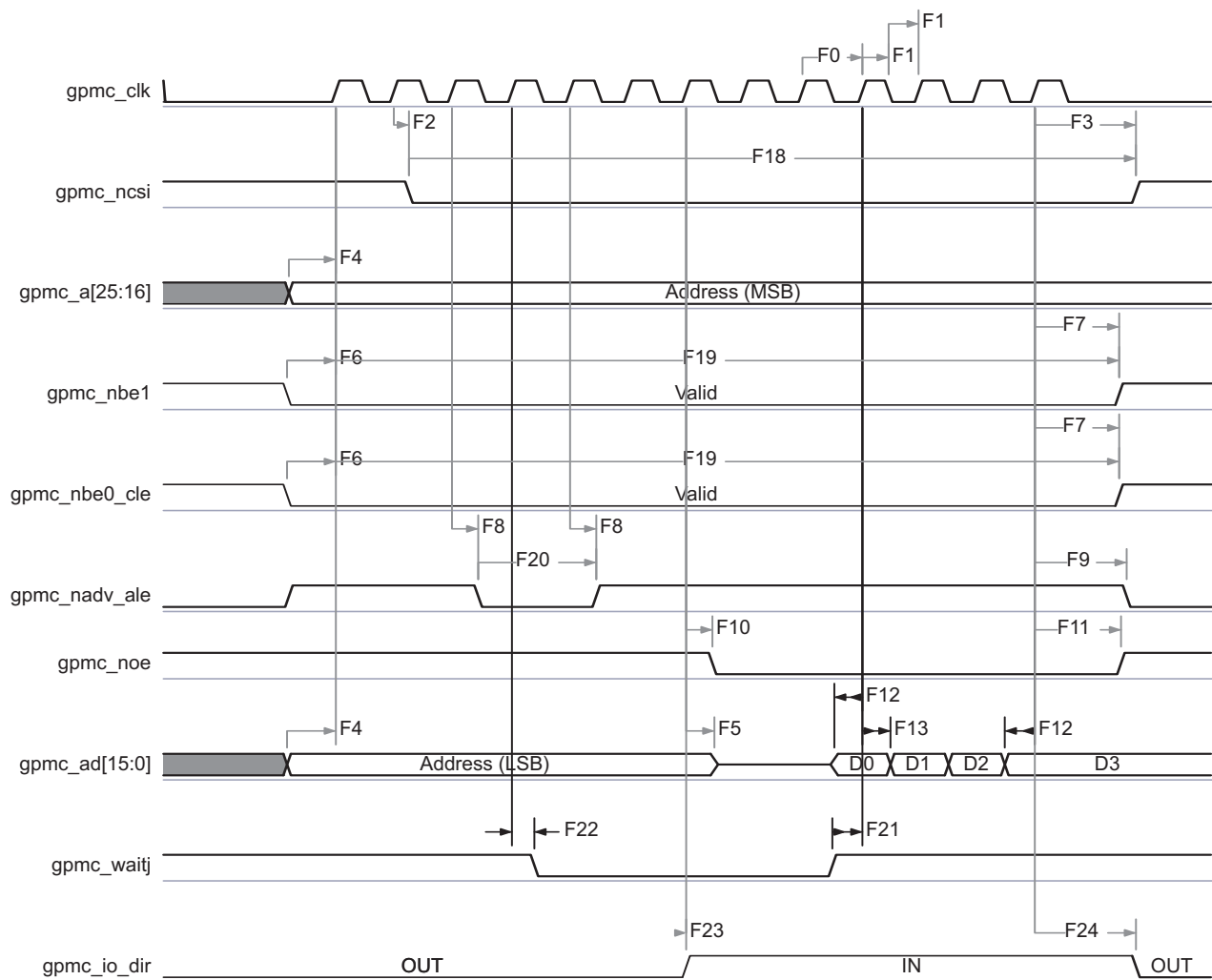
- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.



SWPS050_GPMC_02

Figure 6-3. GPMC / Non-Multiplexed 16bits NOR Flash – Synchronous Single Read⁽¹⁾⁽²⁾⁽³⁾

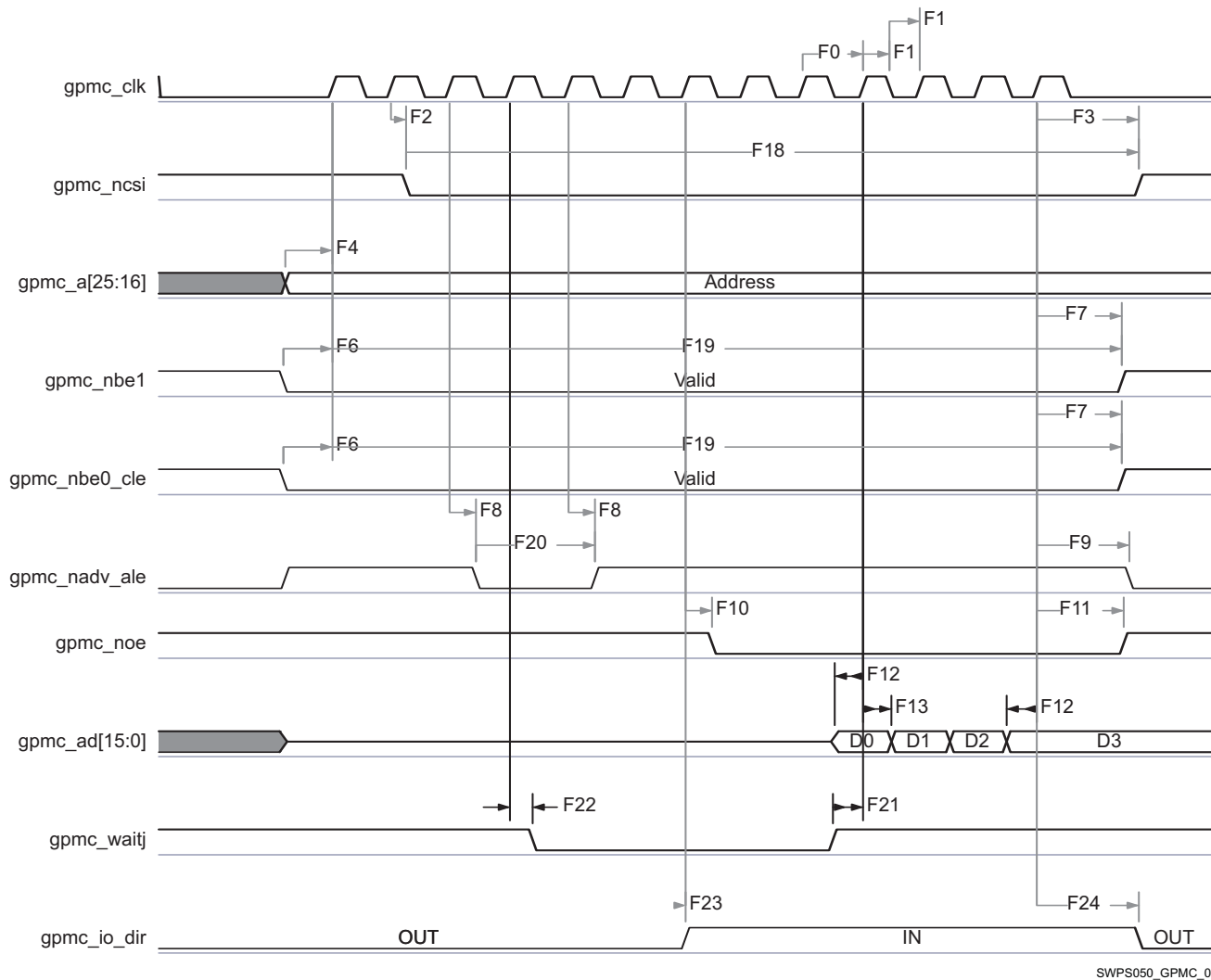
- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.
- (3) Non Multiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.



SWPS050_GPMC_03

Figure 6-4. GPMC / Multiplexed 16bits NOR Flash – Synchronous Burst Read 4*16 Bits⁽¹⁾⁽²⁾

- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
 (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.



SWPS050_GPMC_04

Figure 6-5. GPMC / Non-Multiplexed 16bits NOR Flash – Synchronous Burst Read 4*16 Bits⁽¹⁾⁽²⁾⁽³⁾

- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.
- (3) Non Multiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

6.4.1.1.2 NOR Flash, Asynchronous Mode

Table 6-5 and Table 6-6 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Table 6-5 through Figure 6-13).

Table 6-5. NOR Flash Interface Timing Requirements – Asynchronous Mode

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|------|-------------------------------|--|-----|------------------|--------|
| FA5 | t _{acc(DAT)} | Data Maximum Access Time (GPMC_FCLK cycles) | | H ⁽¹⁾ | cycles |
| FA20 | t _{acc1-pgmode(DAT)} | Page Mode Successive Data Maximum Access Time (GPMC_FCLK cycles) | | P ⁽²⁾ | cycles |
| FA21 | t _{acc2-pgmode(DAT)} | Page Mode First Data Maximum Access Time (GPMC_FCLK cycles) | | H ⁽¹⁾ | cycles |
| | t _{su(DV-OEH)} | Setup time. read gpmc_ad[15:0] valid before gpmc_noe high | 1.9 | | ns |
| | t _{h(OEH-DV)} | Hold time, read gpmc_ad[15:0] valid after gpmc_noe high | 1 | | ns |

- (1) H = Access Time * (TimeParaGranularity + 1)
 (2) P = PageBurstAccessTime * (TimeParaGranularity + 1)

Table 6-6. NOR Flash Switching Characteristics — Write Asynchronous Mode

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|------------------------|---|-------------------------|------------------------|------|
| | | | MIN | MAX | |
| FA0 | $t_{W(nBEV)}$ | Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 valid time | N | | ns |
| FA1 | $t_{W(nCSV)}$ | Pulse duration, gpmc_ncsx low | A | | ns |
| FA3 | $t_{D(nCSV-nADVIV)}$ | Delay time, gpmc_ncsx valid to gpmc_nadv_ale invalid | B - 0.2 | B + 2 | ns |
| FA4 | $t_{d(nCSV-nOEIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren invalid (Single read) | C ⁽³⁾ - 0.2 | C ⁽³⁾ + 2 | ns |
| FA9 | $t_{D(AV-nCSV)}$ | Delay time, address bus valid to gpmc_ncsx valid | J - 0.2 | J + 2 | ns |
| FA10 | $t_{D(nBEV-nCSV)}$ | Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_ncsx valid | J - 0.2 | J + 2 | ns |
| FA12 | $t_{D(nCSV-nADVIV)}$ | Delay time, gpmc_ncsx valid to gpmc_nadv_ale valid | K - 0.2 | K + 2 | ns |
| FA13 | $t_{d(nCSV-nOEIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren valid | L ⁽¹¹⁾ - 0.2 | L ⁽¹¹⁾ + 2 | ns |
| FA16 | $t_{W(AIV)}$ | Pulse duration, address invalid between 2 successive R/W accesses | G ⁽⁷⁾ | | ns |
| FA18 | $t_{d(nCSV-nOEIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren invalid (Burst read) | I ⁽⁸⁾ - 0.2 | I ⁽⁸⁾ + 2 | ns |
| FA20 | $t_{W(AV)}$ | Pulse duration, address valid : 2nd, 3rd and 4th accesses | D ⁽⁴⁾ | | ns |
| FA25 | $t_{D(nCSV-nWEV)}$ | Delay time, gpmc_ncsx valid to gpmc_nwe valid | E - 0.2 | E + 2 | ns |
| FA27 | $t_{D(nCSV-nWEIV)}$ | Delay time, gpmc_ncsx valid to gpmc_nwe invalid | F - 0.2 | F + 2 | ns |
| FA28 | $t_{D(nCSV-DV)}$ | Delay time, gpmc_ncsx valid to data bus valid | W ⁽¹⁸⁾ -0.2 | W ⁽¹⁸⁾ +2.0 | ns |
| FA29 | $t_{D(DV-nCSV)}$ | Delay time, data bus valid to gpmc_ncsx valid | J - 0.2 | J + 2 | ns |
| | $t_{R(DO)}$ | Rise time, output data gpmc_ad[15:0] | | 1.4 | ns |
| | $t_{F(DO)}$ | Fall time, output data gpmc_ad[15:0] | | 1.4 | ns |
| FA37 | $t_{d(nOEIV-AIV)}$ | Delay time, gpmc_oen_ren valid to gpmc_ad[15:0] multiplexed address bus phase end | | 2 | ns |
| FA38 | $t_{d-w(nCSV-nADVIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale first invalid (write mode) | V ⁽¹⁵⁾ | | ns |
| FA39 | $t_{d-r(nCSV-nADVIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale first invalid (read mode) | Q ⁽¹⁴⁾ | | ns |
| FA40 | $t_{d(nCSV-nADVIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale first valid | R ⁽¹³⁾ | | ns |
| FA41 | $t_{d(nCSV-nOEIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren first invalid | S ⁽¹⁶⁾ | | ns |
| FA42 | $t_{d(nCSV-nOEIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren first valid | U ⁽¹⁷⁾ | | ns |

- (1) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
 For single write: A = (CSWrOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
 For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
 For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
 with n the page burst access number.
- (2) For reading: B = ((ADVrOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSEExtraDelay)) * GPMC_FCLK period
 For writing: B = ((ADVWrOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSEExtraDelay)) * GPMC_FCLK period
- (3) C = ((OEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSEExtraDelay)) * GPMC_FCLK
 For single read: C = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK period
- (4) D = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC_FCLK
- (5) E = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSEExtraDelay)) * GPMC_FCLK period
- (6) F = ((WEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSEExtraDelay)) * GPMC_FCLK period
- (7) G = Cycle2CycleDelay * GPMC_FCLK * (TimeParaGranularity + 1)
- (8) I = ((OEOffTime + (n - 1) * PageBurstAccessTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSEExtraDelay)) * GPMC_FCLK period
- (9) J = (CSOnTime * (TimeParaGranularity + 1) + 0.5 * CSEExtraDelay) * GPMC_FCLK period
- (10) K = ((ADVOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSEExtraDelay)) * GPMC_FCLK period
- (11) L = ((OEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSEExtraDelay)) * GPMC_FCLK period
- (12) For single read: N = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK period
 For single write: N = WrCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK period

- For burst read: $N = (RdCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK \text{ period}$
 For burst write: $N = (WrCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK \text{ period}$
- (13) $R = ((ADVNTIME - CSNTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK \text{ period}$
- (14) $Q = ((ADVAADRDOFFTIME - CSNTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK \text{ period}$
- (15) $V = ((ADVAADWROFFTIME - CSNTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK \text{ period}$
- (16) $S = ((OEADMUXOFFTIME - CSNTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK \text{ period}$
- (17) $U = ((OEADMUXONTIME - CSNTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY - CSEXTRADELAY)) * GPMC_FCLK \text{ period}$
- (18) $W = ((WRDATAONADMUXBUS - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSEExtraDelay)) * GPMC_FCLK \text{ period}$

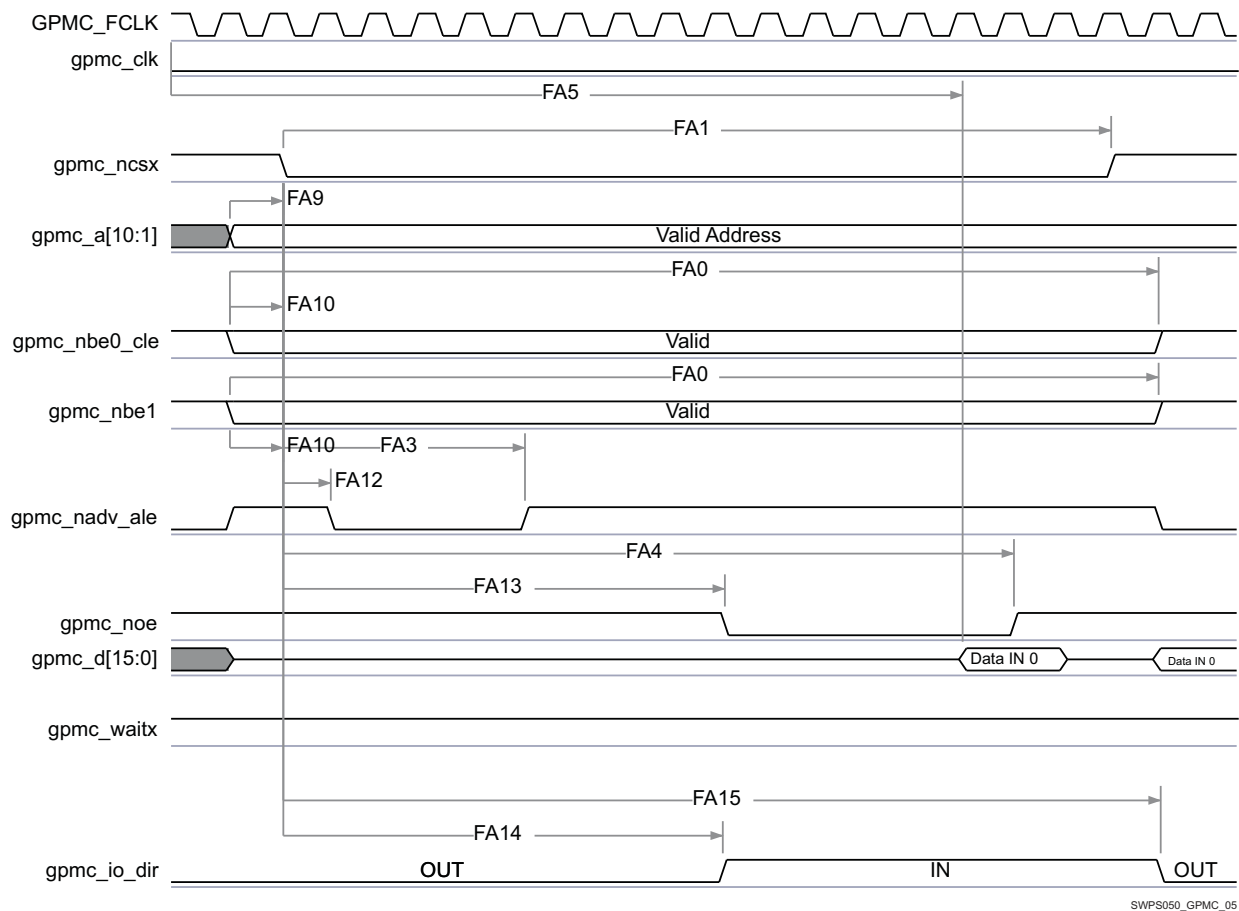
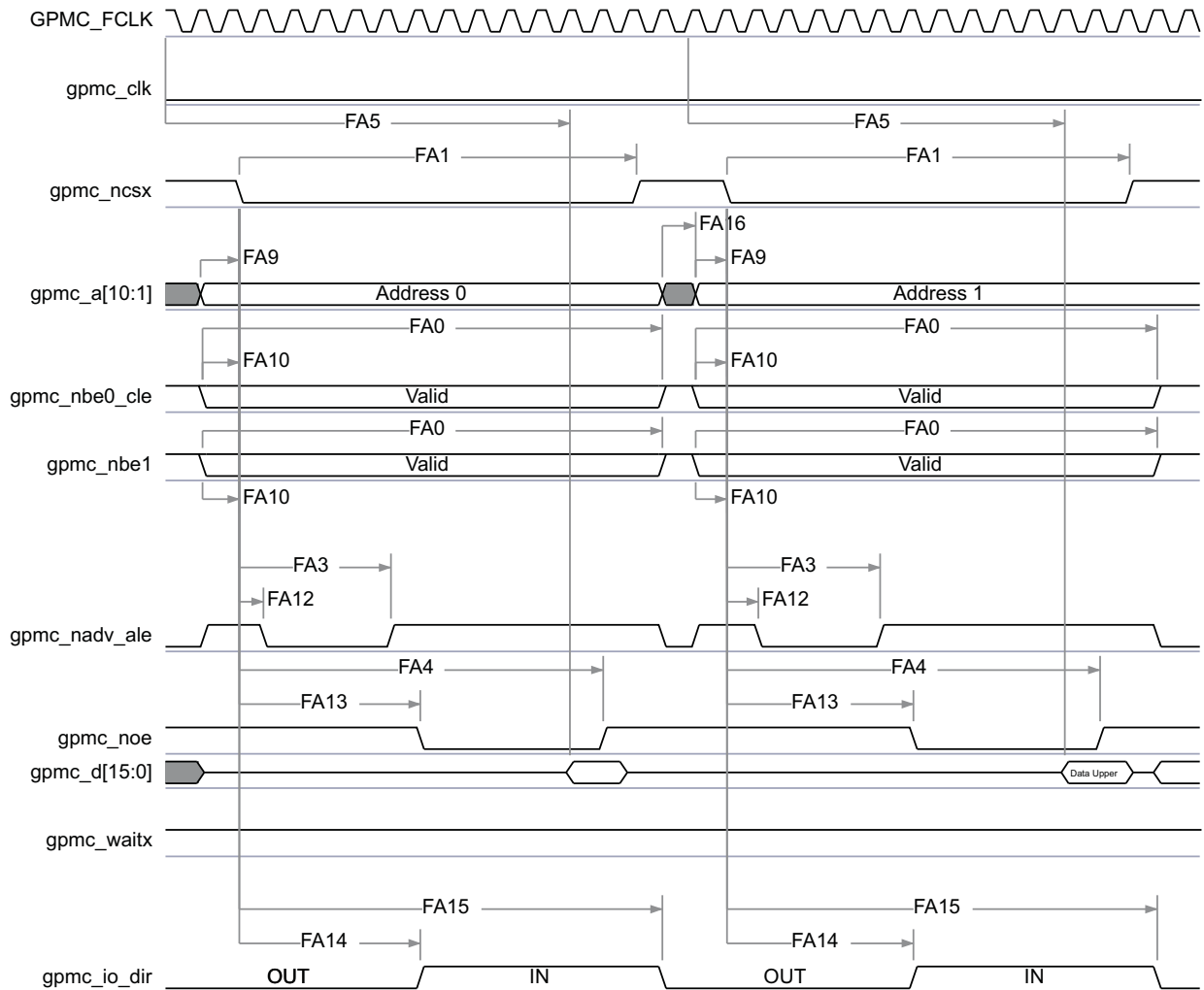


Figure 6-6. GPMC / NOR Flash - Asynchronous Read - Single Word Timing⁽¹⁾⁽²⁾⁽³⁾

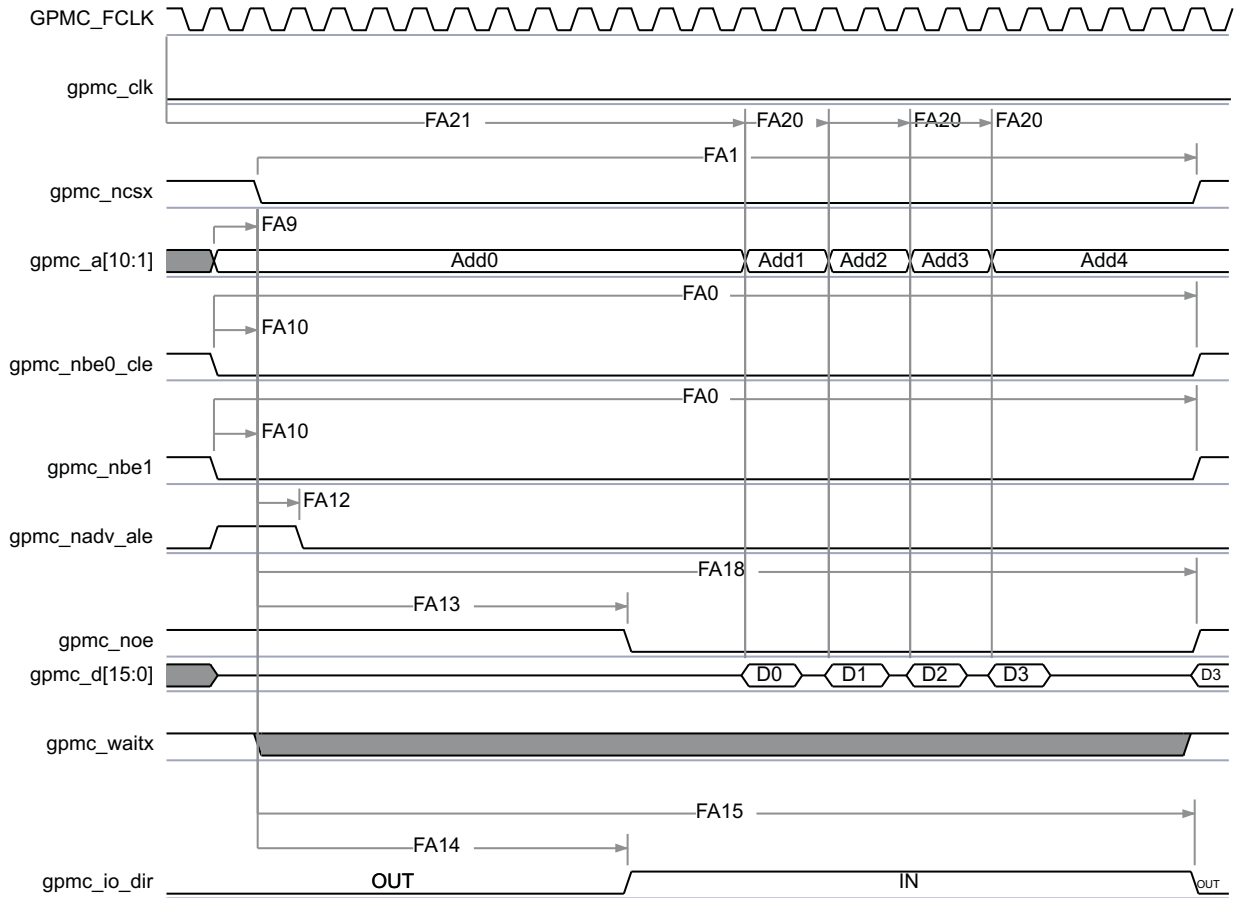
- (1) In gpmc_ncsx, x = 0 to 7. In gpmc_waitx, x = 0 to 3.
- (2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- (3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.



SWPS050_GPMC_06

Figure 6-7. GPMC / NOR Flash - Asynchronous Read - 32-bit Timing⁽¹⁾⁽²⁾⁽³⁾

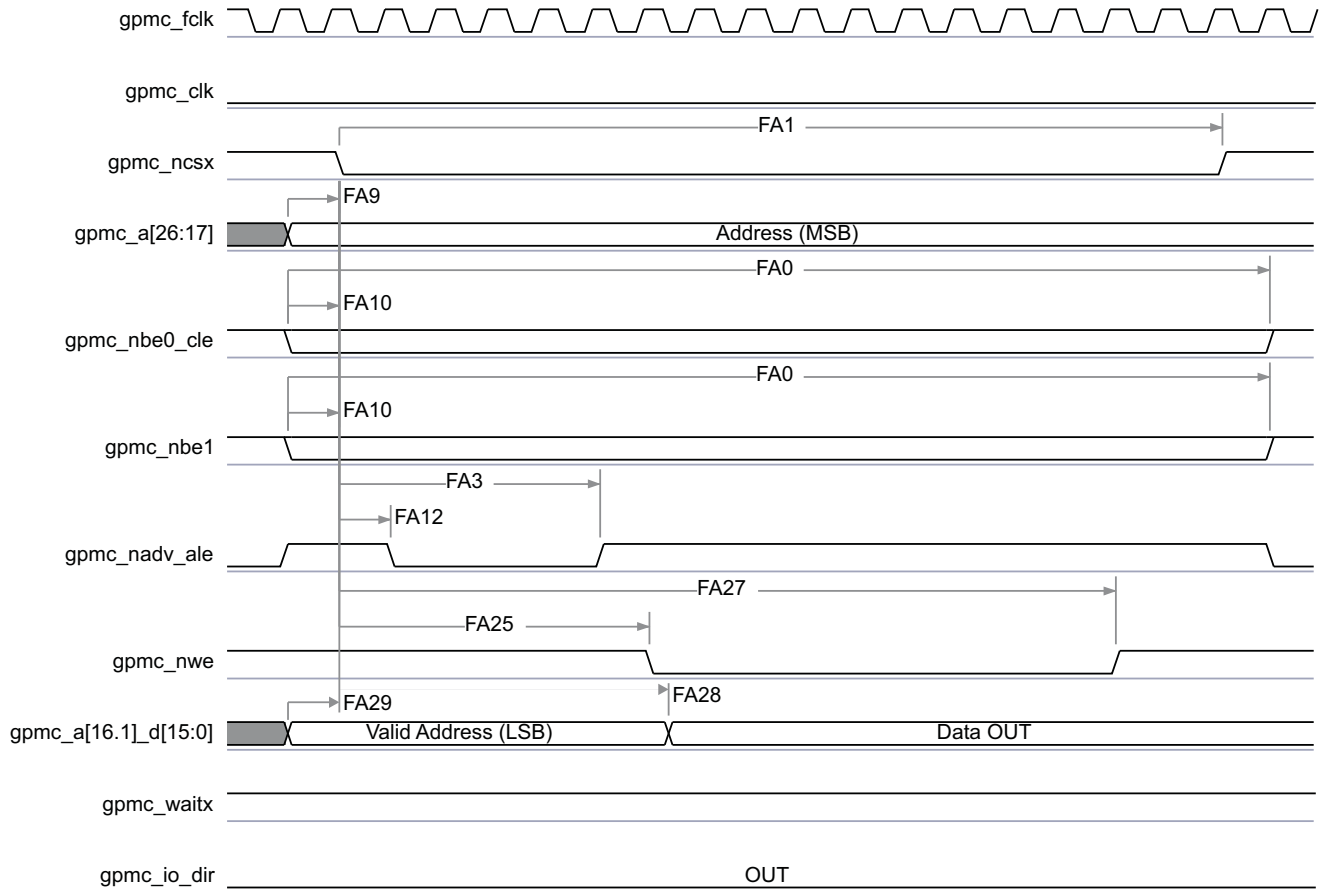
- (1) In "gpmc_ncsx", x = 0 to 7. In "gpmc_waitx", x = 0 to 3.
- (2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value should be stored inside AccessTime register bits field
- (3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally



SWPS050_GPMC_07

Figure 6-8. GPMC / NOR Flash - Asynchronous Read - Page Mode 4x16-bit Timing⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

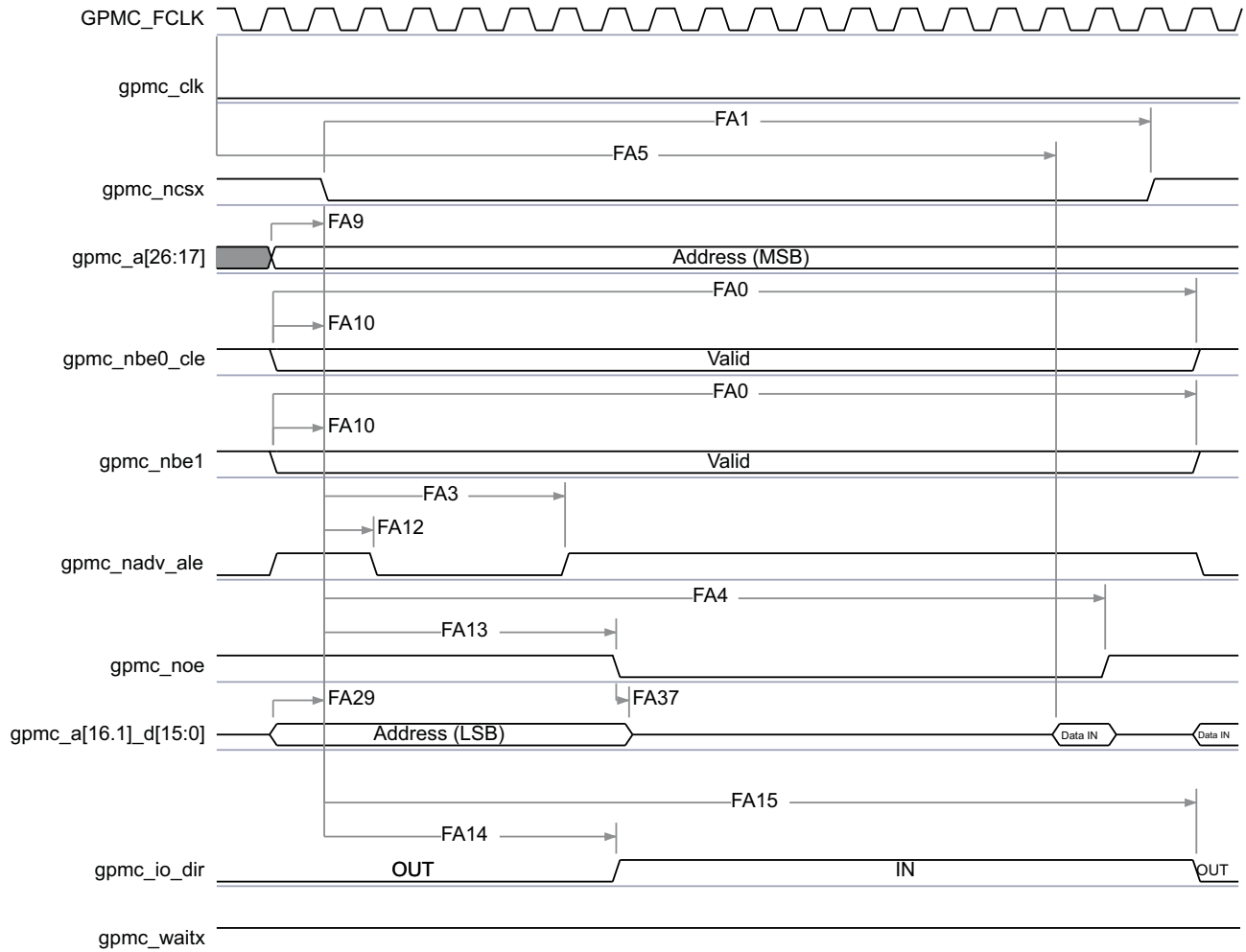
- (1) In “gpmc_ncsx”, x = 0 to 7. In “gpmc_waitx”, x = 0 to 3
- (2) FA21 parameter illustrates amount of time required to internally sample first input Page Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, First input Page Data will be internally sampled by active functional clock edge. FA21 calculation is detailed in a separated application note (ref ...) and should be stored inside AccessTime register bits field.
- (3) FA20 parameter illustrates amount of time required to internally sample successive input Page Data. It is expressed in number of GPMC functional clock cycles. After each access to input Page Data, next input Page Data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input Page Data (excluding first input Page Data). FA20 value should be stored in PageBurstAccessTime register bits field.
- (4) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally



SWPS050_GPMC_08

Figure 6-9. GPMC / Multiplexed 16bits NOR Flash – Asynchronous Single Write⁽¹⁾⁽²⁾

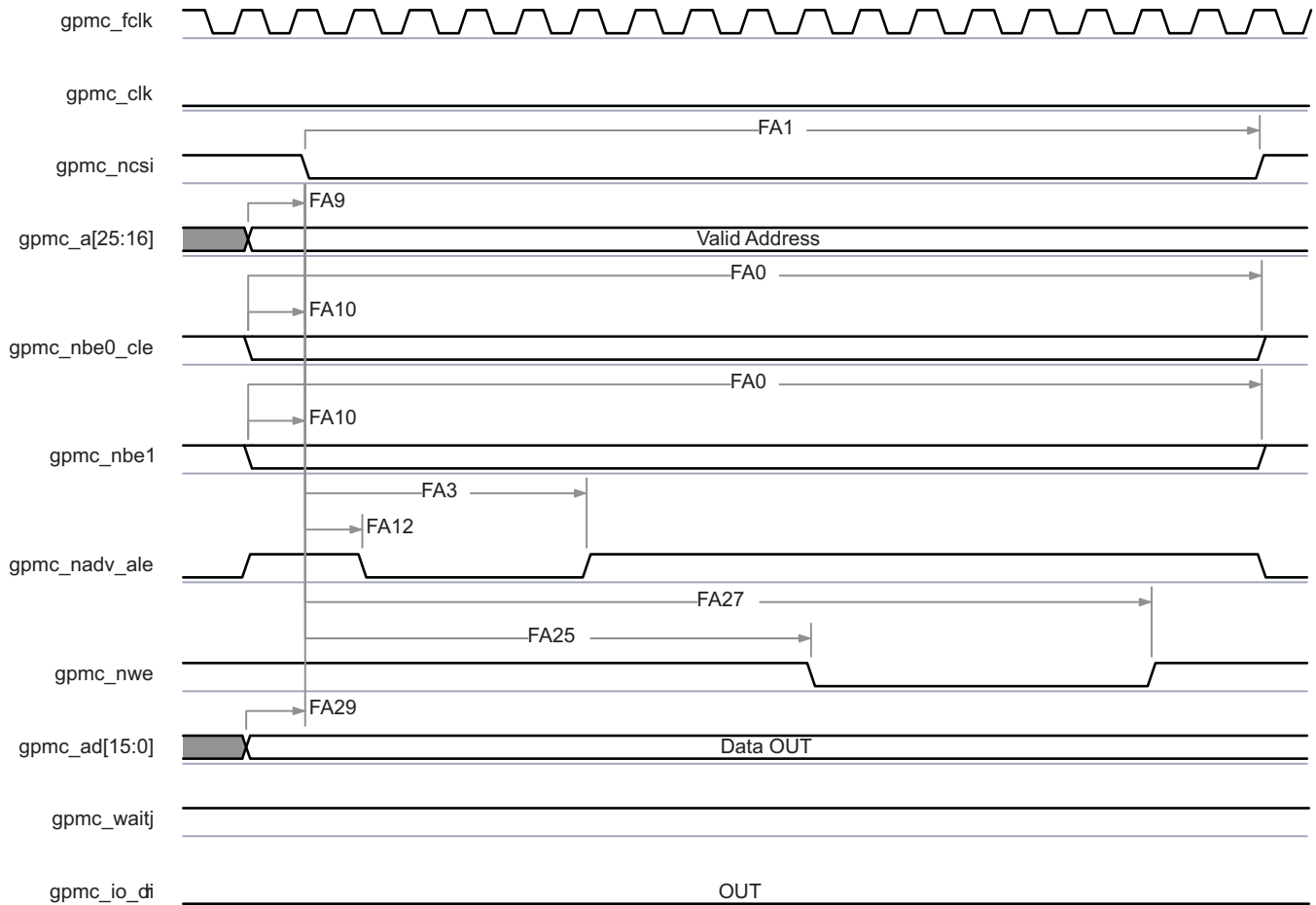
- (1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, 7.
 (2) In gpmc_waitx, x is equal to 0, 1, 2, 3.



SWPS050_GPMC_09

Figure 6-10. GPMC / Multiplexed NOR Flash - Asynchronous Read - Single Word Timing⁽¹⁾⁽²⁾⁽³⁾

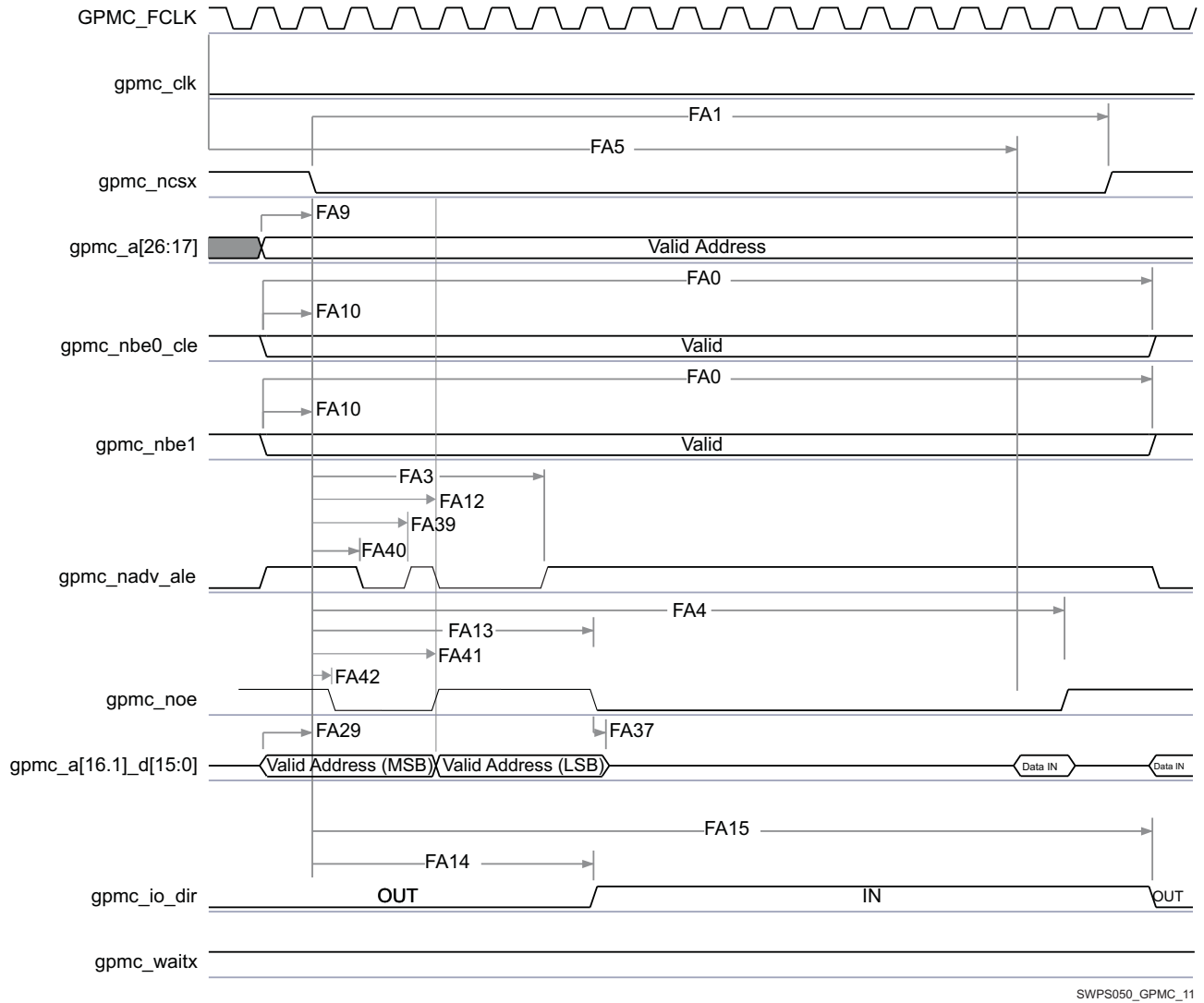
- (1) In "gpmc_ncsx", x = 0 to 7. In "gpmc_waitx", x = 0 to 3
- (2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value should be stored inside AccessTime register bits field.
- (3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally



SWPS050_GPMC_10

Figure 6-11. GPMC / Non-Multiplexed 16bits NOR Flash – Asynchronous Single Write⁽¹⁾⁽²⁾⁽³⁾

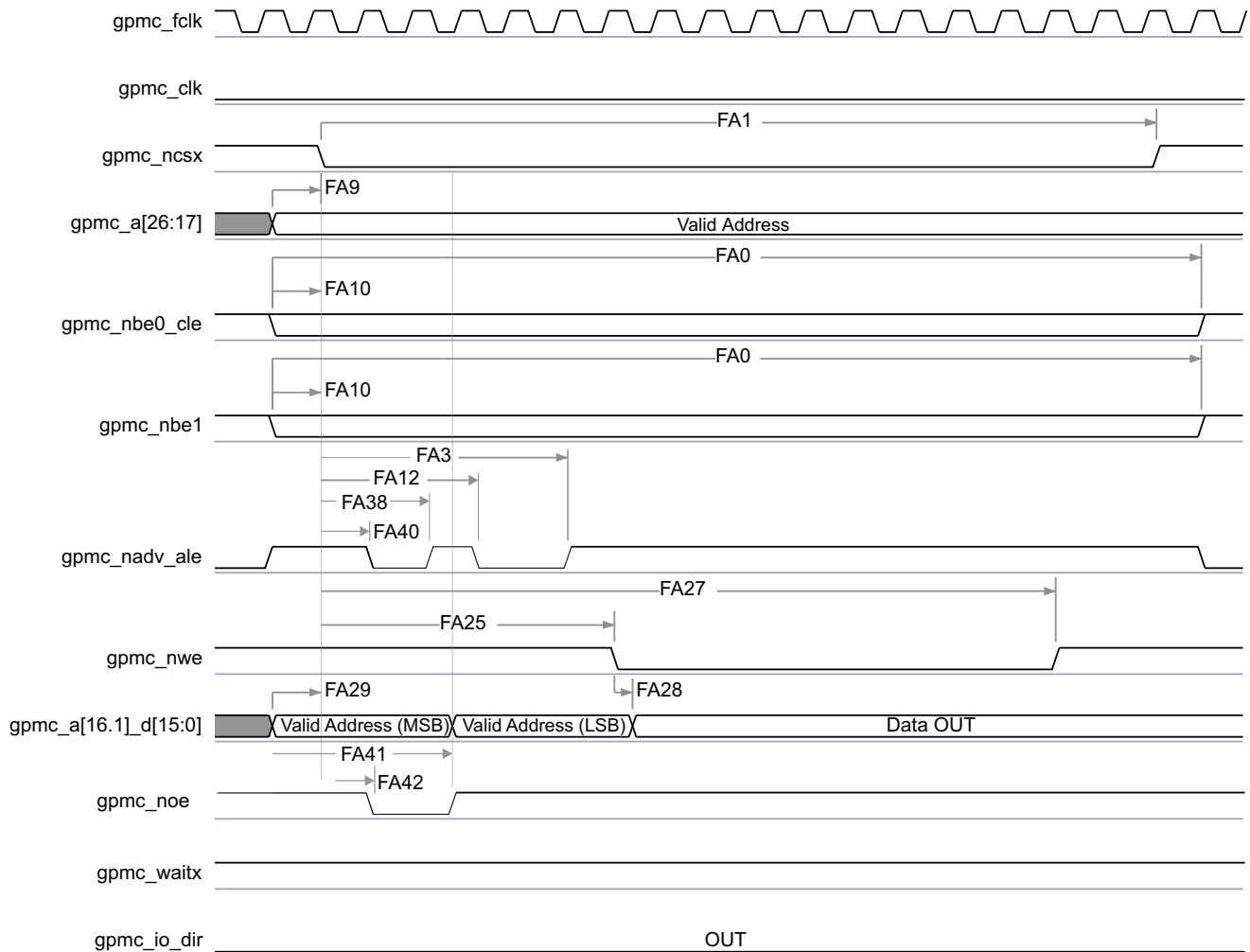
- (1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitx, x is equal to 0, 1, 2, 3.
- (3) Non Multiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.



SWPS050_GPMC_11

Figure 6-12. GPMC / AAD Multiplexed NOR Flash - Asynchronous Single Read⁽¹⁾

(1) In "gpmc_ncsx", x = 0 to 7. In "gpmc_waitx", x = 0 to 3



SWPS050_GPMC_12

Figure 6-13. GPMC / AAD Multiplexed NOR Flash - Asynchronous Single Write⁽¹⁾

(1) In "gpmc_ncsx", x = 0 to 7. In "gpmc_waitx", x = 0 to 3

6.4.1.2 NAND, Synchronous mode, 66.5 MHz, 1.8 V

Table 6-7. NAND Timing Conditions — Synchronous mode

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|-------------------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 2.03 | 5.49 | ns |
| t_F | Input signal fall time | 1.38 | 6.09 | ns |
| PCB Conditions⁽¹⁾ | | | | |

(1) See [Table 7-4](#).

(2) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-8](#) and [Table 6-9](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-8. NAND Timing Requirements —Synchronous Mode⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| F12 | $t_{SU(dV-clkH)}$ | Setup time, input data gpmc_ad[15:0] valid before output gpmc_clk high | 2.5 | | ns |
| F13 | $t_{H(clkH-dV)}$ | Hold time, input data gpmc_ad[15:0] valid after output gpmc_clk high | 1.9 | | ns |
| F21 | $t_{SU(waitV-clkH)}$ | Setup time, input wait gpmc_waitx ⁽¹⁾ valid before output gpmc_clk high | 2.5 | | ns |
| F22 | $t_{H(clkH-waitV)}$ | Hold time, input wait gpmc_waitx ⁽¹⁾ valid after output gpmc_clk high | 1.9 | | ns |

(1) In gpmc_waitx, x is equal to 0, 1, 2, or 3.

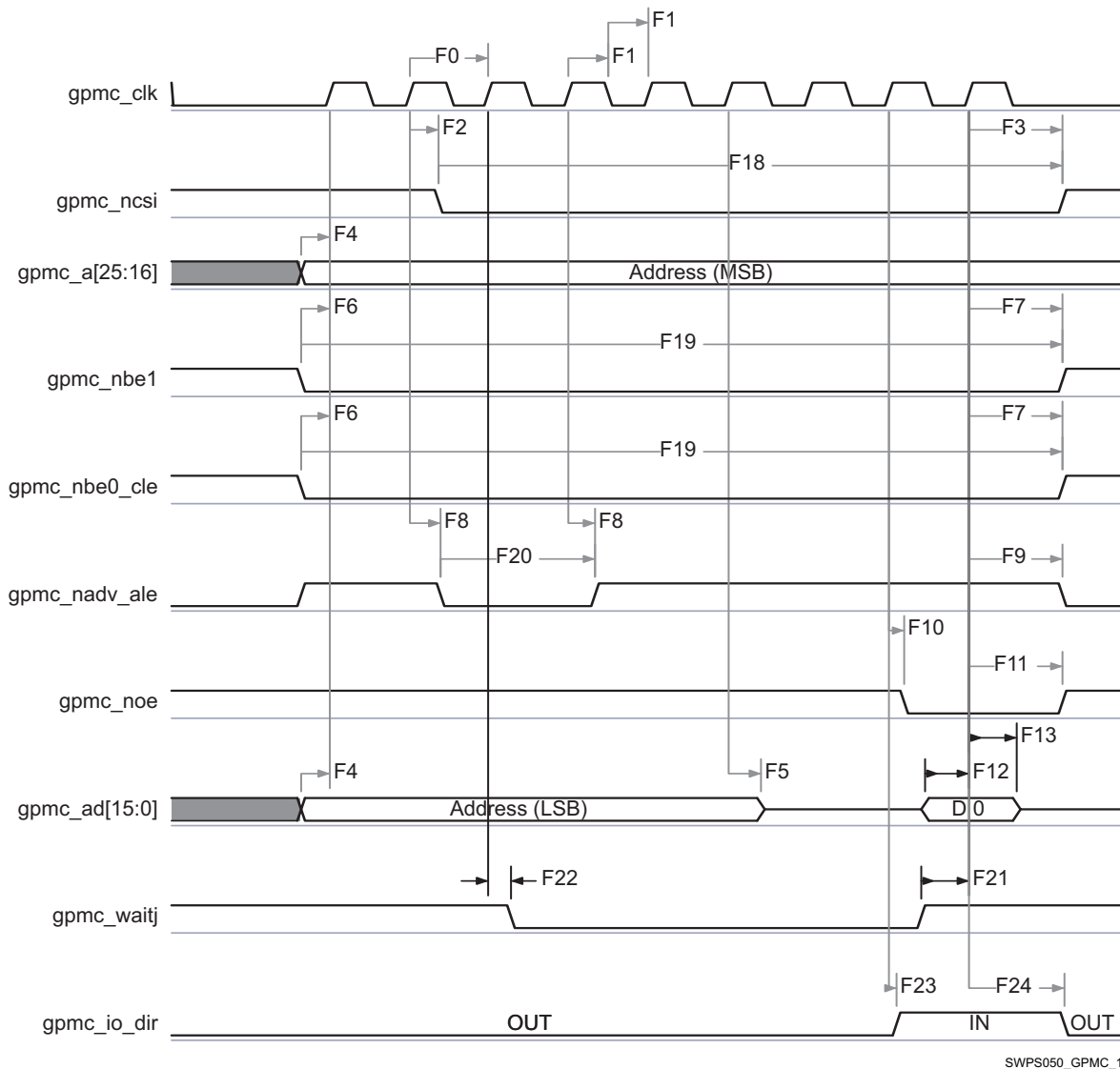
(2) See Section 4.3 for CORE OPP voltages.

Table 6-9. NAND Switching Characteristics — Synchronous Mode⁽¹⁷⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|-----------------------|--|-------------------------|-------------------------|------|
| | | | MIN | MAX | |
| F0 | $1 / t_{C(CLK)}$ | Frequency ⁽¹⁴⁾ , output gpmc_clk | | 66.5 | MHz |
| F1 | $t_{W(CLKH)}$ | Typical Pulse duration, output gpmc_clk high | 0.5 P ⁽¹²⁾ | | ns |
| F1 | $t_{W(CLKL)}$ | Typical Pulse duration, output gpmc_clk low | 0.5 P ⁽¹²⁾ | | ns |
| | $t_{DC(CLK)}$ | Duty cycle error, output gpmc_clk | | 752 | ps |
| | $t_{J(CLK)}$ | Jitter standard deviation ⁽¹⁵⁾ , output gpmc_clk | | 97.3 | ps |
| | $t_{R(CLK)}$ | Rise time, output gpmc_clk | 0.9 | 1.8 | ns |
| | $t_{F(CLK)}$ | Fall time, output gpmc_clk | 0.9 | 1.6 | ns |
| | $t_{R(DO)}$ | Rise time, output data gpmc_ad[15:0] | 0.9 | 1.8 | ns |
| | $t_{F(DO)}$ | Fall time, output data gpmc_ad[15:0] | 0.9 | 1.6 | ns |
| F2 | $t_{D(CLKH-nCSV)}$ | Delay time, gpmc_clk rising edge to gpmc_ncsx ⁽¹¹⁾ valid | F ⁽⁶⁾ + 0.6 | F ⁽⁶⁾ + 6.1 | ns |
| F3 | $t_{D(CLKH-nCSIV)}$ | Delay time, gpmc_clk rising edge to gpmc_ncsx ⁽¹¹⁾ invalid | E ⁽⁵⁾ + 0.6 | E ⁽⁵⁾ + 6.1 | ns |
| F4 | $t_{D(ADDV-CLK)}$ | Delay time, gpmc_a[25:16] address bus valid to gpmc_clk first edge | B ⁽²⁾ – 6.1 | B ⁽²⁾ – 0.7 | ns |
| F5 | $t_{D(CLKH-ADDIV)}$ | Delay time, gpmc_clk rising edge to gpmc_a[25:16] gpmc address bus invalid | 0.7 | | ns |
| F6 | $t_{D(nBEV-CLK)}$ | Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_clk first edge | B ⁽²⁾ – 4.9 | B ⁽²⁾ + 0.4 | ns |
| F7 | $t_{D(CLKH-nBEIV)}$ | Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 invalid | D ⁽⁴⁾ – 0.4 | D ⁽⁴⁾ + 4.9 | ns |
| F8 | $t_{D(CLKH-nADV)}$ | Delay time, gpmc_clk rising edge to gpmc_nadv_ale valid | G ⁽⁷⁾ + 0.6 | G ⁽⁷⁾ + 6.1 | ns |
| F9 | $t_{D(CLKH-nADVIV)}$ | Delay time, gpmc_clk rising edge to gpmc_nadv_ale invalid | D ⁽⁴⁾ + 0.6 | D ⁽⁴⁾ + 6.1 | ns |
| F10 | $t_{D(CLKH-nOE)}$ | Delay time, gpmc_clk rising edge to gpmc_noe valid | H ⁽⁸⁾ + 0.3 | H ⁽⁸⁾ + 5.1 | ns |
| F11 | $t_{D(CLKH-nOEIV)}$ | Delay time, gpmc rising edge to gpmc_noe invalid | E ⁽⁵⁾ + 0.3 | E ⁽⁵⁾ + 5.1 | ns |
| F14 | $t_{D(CLKH-nWE)}$ | Delay time, gpmc_clk rising edge to gpmc_nwe transition | I ⁽⁹⁾ + 0.6 | I ⁽⁹⁾ + 6.1 | ns |
| F15 | $t_{D(CLKH-Data)}$ | Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition | J ⁽¹⁰⁾ – 0.4 | J ⁽¹⁰⁾ + 4.9 | ns |
| F17 | $t_{D(CLKH-nBE)}$ | Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 transition | J ⁽¹⁰⁾ – 0.4 | J ⁽¹⁰⁾ + 4.9 | ns |
| F18 | $t_{W(nCSV)}$ | Pulse duration, gpmc_ncsx ⁽¹¹⁾ low | Read | A ⁽¹⁾ | ns |
| | | | Write | A ⁽¹⁾ | ns |
| F19 | $t_{W(nBEV)}$ | Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 low | Read | C ⁽³⁾ | ns |
| | | | Write | C ⁽³⁾ | ns |
| F20 | $t_{W(nADV)}$ | Pulse duration, gpmc_nadv_ale low | Read | K ⁽¹³⁾ | ns |
| | | | Write | K ⁽¹³⁾ | ns |
| F23 | $t_{D(CLKH-IODIR)}$ | Delay time, gpmc_clk rising edge to gpmc_io_dir high (IN direction) | H ⁽⁸⁾ + 0.7 | H ⁽⁸⁾ + 5.1 | ns |
| F24 | $t_{D(CLKH-IODIRIV)}$ | Delay time, gpmc rising edge to gpmc_io_dir low (OUT direction) | M ⁽¹⁶⁾ + 0.7 | M ⁽¹⁶⁾ + 5.1 | ns |

- (1) For single read: $A = (\text{CSRdOffTime} - \text{CSONTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK period}$.
 For burst read: $A = (\text{CSRdOffTime} - \text{CSONTime} + (n - 1) * \text{PageBurstAccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK period}$
 with n the page burst access number.
 For burst write: $A = (\text{CSWrOffTime} - \text{CSONTime} + (n - 1) * \text{PageBurstAccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK period}$
 with n the page burst access number.
- (2) $B = \text{ClkActivationTime} * \text{GPMC_FCLK}$
- (3) For single read: $C = \text{RdCycleTime} * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
 For burst read: $C = (\text{RdCycleTime} + (n - 1) * \text{PageBurstAccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$ with n the page burst access number.
 For Burst write: $C = (\text{WrCycleTime} + (n - 1) * \text{PageBurstAccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$ with n the page burst access number.
- (4) For single read: $D = (\text{RdCycleTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
 For burst read: $D = (\text{RdCycleTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
 For burst write: $D = (\text{WrCycleTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
- (5) For single read: $E = (\text{CSRdOffTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
 For burst read: $E = (\text{CSRdOffTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
 For burst write: $E = (\text{CSWrOffTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC_FCLK}$
- (6) For nCS falling edge (CS activated):
 Case GpmcFCLKDivider = 0:
 $F = 0.5 * \text{CSEExtraDelay} * \text{GPMC_FCLK}$
 Case GpmcFCLKDivider = 1:
 $F = 0.5 * \text{CSEExtraDelay} * \text{GPMC_FCLK}$ if (ClkActivationTime and CSONTime are odd) or (ClkActivationTime and CSONTime are even)
 $F = (1 + 0.5 * \text{CSEExtraDelay}) * \text{GPMC_FCLK}$
 otherwise
 Case GpmcFCLKDivider = 2:
 $F = 0.5 * \text{CSEExtraDelay} * \text{GPMC_FCLK}$ if ((CSONTime – ClkActivationTime) is a multiple of 3)
 $F = (1 + 0.5 * \text{CSEExtraDelay}) * \text{GPMC_FCLK}$ if ((CSONTime – ClkActivationTime – 1) is a multiple of 3)
 $F = (2 + 0.5 * \text{CSEExtraDelay}) * \text{GPMC_FCLK}$ if ((CSONTime – ClkActivationTime – 2) is a multiple of 3)
- (7) For ADV falling edge (ADV activated):
 Case GpmcFCLKDivider = 0:
 $G = 0.5 * \text{ADVExtraDelay} * \text{GPMC_FCLK}$
 Case GpmcFCLKDivider = 1:
 $G = 0.5 * \text{ADVExtraDelay} * \text{GPMC_FCLK}$ if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
 $G = (1 + 0.5 * \text{ADVExtraDelay}) * \text{GPMC_FCLK}$
 otherwise
 Case GpmcFCLKDivider = 2:
 $G = 0.5 * \text{ADVExtraDelay} * \text{GPMC_FCLK}$ if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
 $G = (1 + 0.5 * \text{ADVExtraDelay}) * \text{GPMC_FCLK}$ if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
 $G = (2 + 0.5 * \text{ADVExtraDelay}) * \text{GPMC_FCLK}$ if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)
 For ADV rising edge (ADV desactivated) in Reading mode:
 Case GpmcFCLKDivider = 0:
 $G = 0.5 * \text{ADVExtraDelay} * \text{GPMC_FCLK}$ Case GpmcFCLKDivider = 1:
 $G = 0.5 * \text{ADVExtraDelay} * \text{GPMC_FCLK}$ if (ClkActivationTime and ADVrOffTime are odd) or (ClkActivationTime and ADVrOffTime are even)
 $G = (1 + 0.5 * \text{ADVExtraDelay}) * \text{GPMC_FCLK}$
 otherwise
 Case GpmcFCLKDivider = 2:
 $G = 0.5 * \text{ADVExtraDelay} * \text{GPMC_FCLK}$ if ((ADVrOffTime – ClkActivationTime) is a multiple of 3)
 $G = (1 + 0.5 * \text{ADVExtraDelay}) * \text{GPMC_FCLK}$ if ((ADVrOffTime – ClkActivationTime – 1) is a multiple of 3)
 $G = (2 + 0.5 * \text{ADVExtraDelay}) * \text{GPMC_FCLK}$ if ((ADVrOffTime – ClkActivationTime – 2) is a multiple of 3)
 For ADV rising edge (ADV desactivated) in Writing mode:
 Case GpmcFCLKDivider = 0:
 $G = 0.5 * \text{ADVExtraDelay} * \text{GPMC_FCLK}$
 Case GpmcFCLKDivider = 1:
 $G = 0.5 * \text{ADVExtraDelay} * \text{GPMC_FCLK}$ if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
 $G = (1 + 0.5 * \text{ADVExtraDelay}) * \text{GPMC_FCLK}$ otherwise
 Case GpmcFCLKDivider = 2:
 $G = 0.5 * \text{ADVExtraDelay} * \text{GPMC_FCLK}$ if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
 $G = (1 + 0.5 * \text{ADVExtraDelay}) * \text{GPMC_FCLK}$ if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
 $G = (2 + 0.5 * \text{ADVExtraDelay}) * \text{GPMC_FCLK}$ if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)
- (8) For OE falling edge (OE activated) / IO DIR rising edge (IN direction):
 Case GpmcFCLKDivider = 0:
 $H = 0.5 * \text{OEEExtraDelay} * \text{GPMC_FCLK}$
 Case GpmcFCLKDivider = 1:
 $H = 0.5 * \text{OEEExtraDelay} * \text{GPMC_FCLK}$ if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
 $H = (1 + 0.5 * \text{OEEExtraDelay}) * \text{GPMC_FCLK}$
 otherwise
 Case GpmcFCLKDivider = 2:

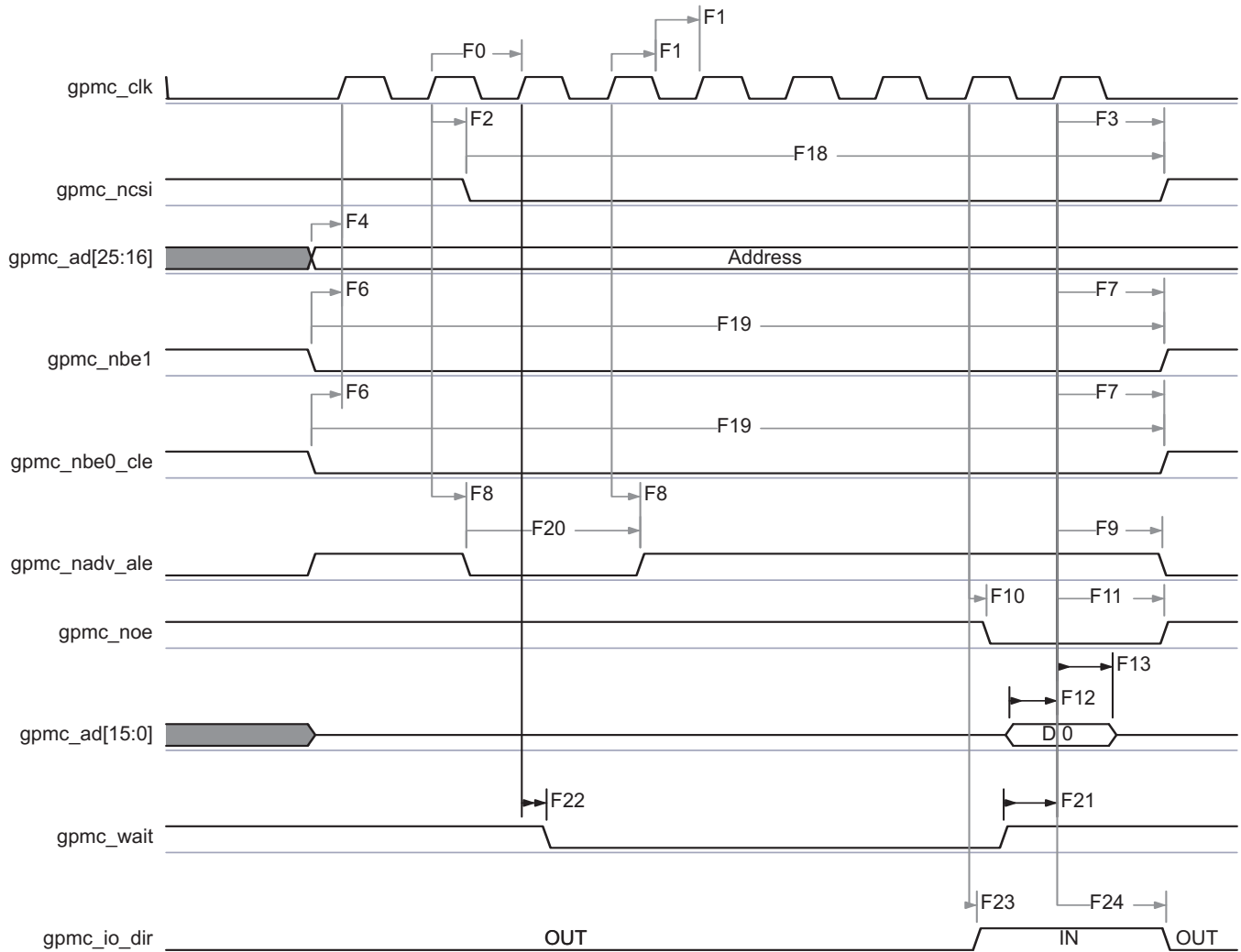
- $H = 0.5 * OEExtraDelay * GPMC_FCLK$ if $((OEOnTime - ClkActivationTime)$ is a multiple of 3)
 $H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK$ if $((OEOnTime - ClkActivationTime - 1)$ is a multiple of 3)
 $H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK$ if $((OEOnTime - ClkActivationTime - 2)$ is a multiple of 3)
 For OE rising edge (OE deactivated):
 Case GpmcFCLKDivider = 0:
 $H = 0.5 * OEExtraDelay * GPMC_FCLK$
 Case GpmcFCLKDivider = 1:
 $H = 0.5 * OEExtraDelay * GPMC_FCLK$ if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
 $H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK$
 otherwise
 Case GpmcFCLKDivider = 2:
 $H = 0.5 * OEExtraDelay * GPMC_FCLK$ if $((OEOffTime - ClkActivationTime)$ is a multiple of 3)
 $H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK$ if $((OEOffTime - ClkActivationTime - 1)$ is a multiple of 3)
 $H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK$ if $((OEOffTime - ClkActivationTime - 2)$ is a multiple of 3)
- (9) For WE falling edge (WE activated):
 Case GpmcFCLKDivider = 0:
 $I = 0.5 * WEExtraDelay * GPMC_FCLK$
 Case GpmcFCLKDivider = 1:
 $I = 0.5 * WEExtraDelay * GPMC_FCLK$ if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
 $I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK$
 otherwise
 Case GpmcFCLKDivider = 2:
 $I = 0.5 * WEExtraDelay * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime)$ is a multiple of 3)
 $I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime - 1)$ is a multiple of 3)
 $I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime - 2)$ is a multiple of 3)
 For WE rising edge (WE deactivated):
 Case GpmcFCLKDivider = 0:
 $I = 0.5 * WEExtraDelay * GPMC_FCLK$
 Case GpmcFCLKDivider = 1:
 $I = 0.5 * WEExtraDelay * GPMC_FCLK$ if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
 $I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK$
 otherwise
 Case GpmcFCLKDivider = 2:
 $I = 0.5 * WEExtraDelay * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime)$ is a multiple of 3)
 $I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime - 1)$ is a multiple of 3)
 $I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime - 2)$ is a multiple of 3)
- (10) $J = GPMC_FCLK$ period
- (11) In "gpmc_ncsx", x is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (12) $P = gpmc_clk$ period
- (13) For read: $K = (ADVrdOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
 For write: $K = (ADVWrOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
- (14) Related to the gpmc_clk output clock Maximum and minimum frequency programmable in I/F module by setting the GPMC_CONFIG1_CSx configuration register bit fields GpmcFCLKDivider
- (15) The jitter probability density can be approximated by a Gaussian function.
- (16) $M = (RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
 Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behaviour of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or non/multiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behaviour is automatically handled by GPMC controller
- (17) See the [Section 4.3](#) for CORE OPP voltages.



SWPS050_GPMC_13

Figure 6-14. GPMC / Multiplexed 16bits NAND – Synchronous Single Read (1) (2)

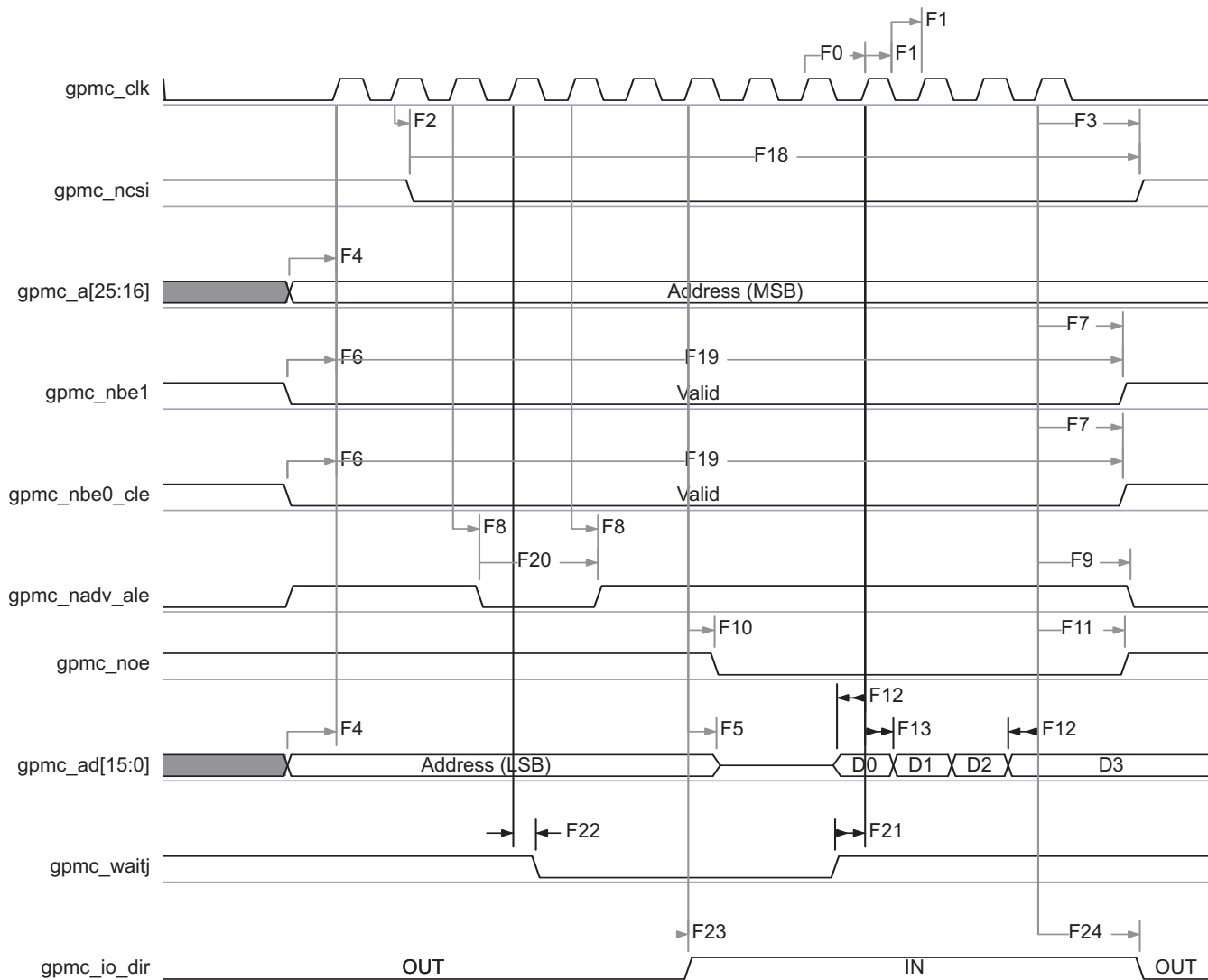
- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.



SWPS050_GPMC_14

Figure 6-15. GPMC / Non-Multiplexed 16bits NAND – Synchronous Single Read (1) (2) (3)

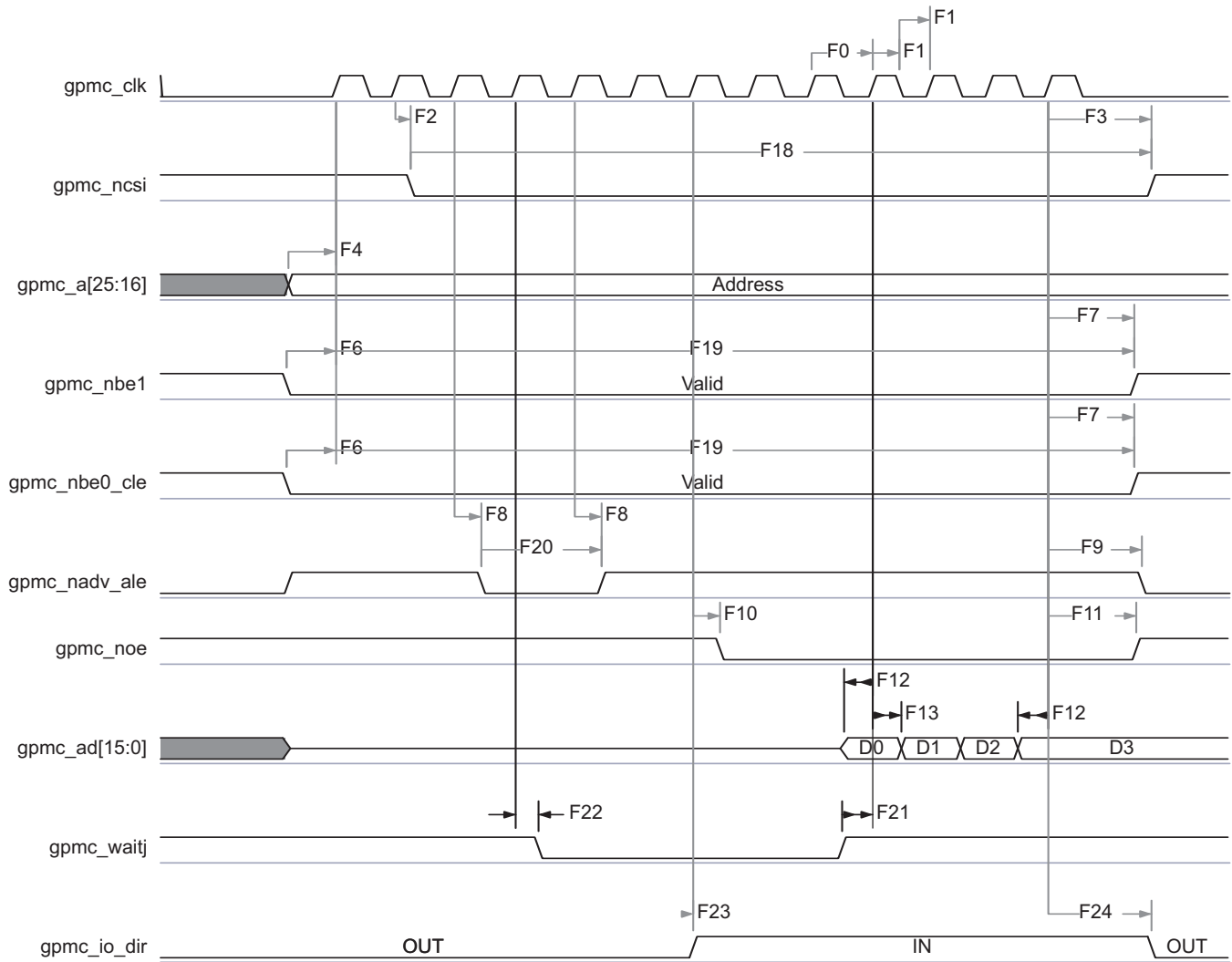
- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.
- (3) Non Multiplexed NAND interface can be used only with a limited address range corresponding to 10 address bits.



SWPS050_GPMC_15

Figure 6-16. GPMC / Multiplexed 16bits NAND – Synchronous Burst Read 4x16 bits (1) (2)

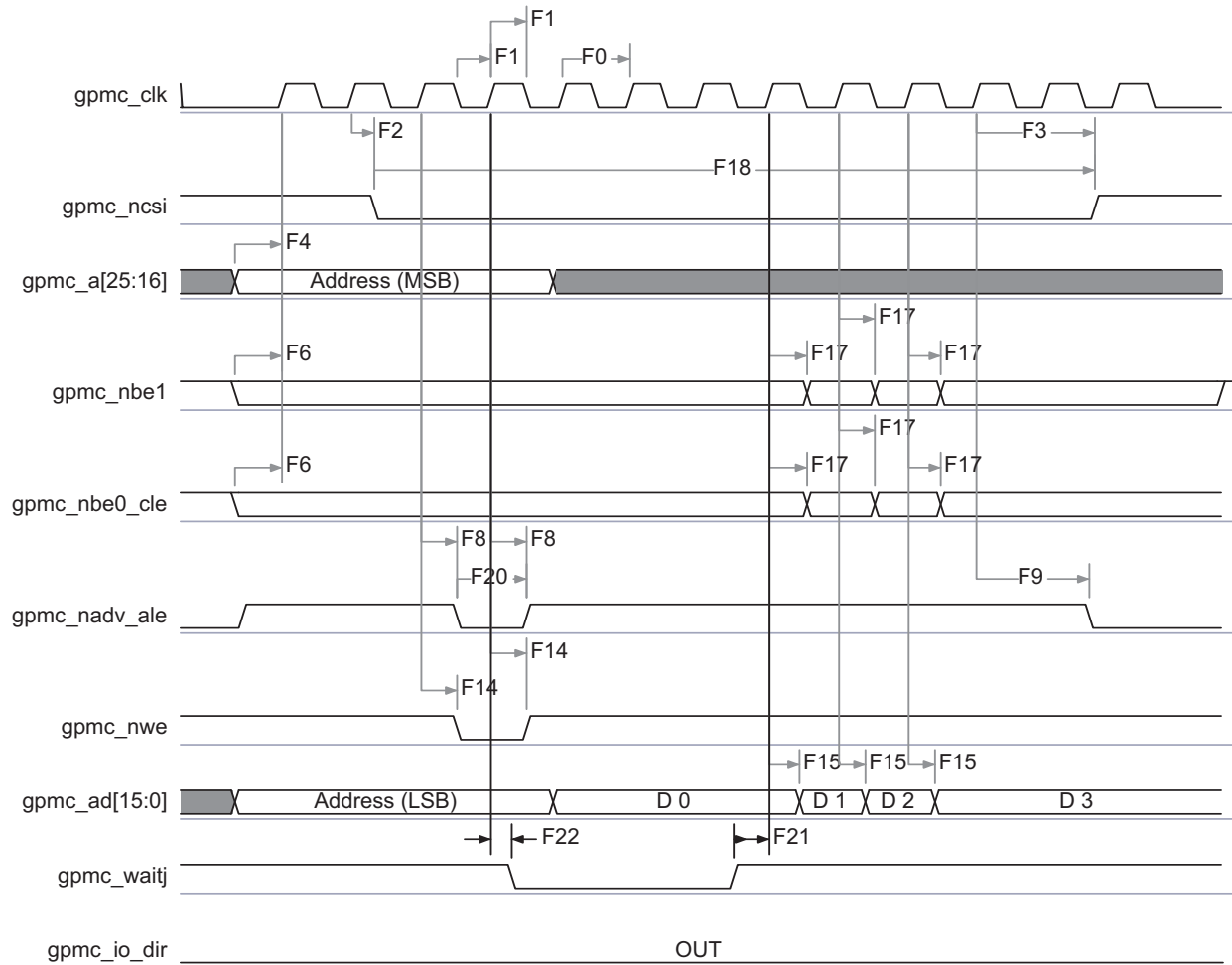
- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.



SWPS050_GPMC_16

Figure 6-17. GPMC / Non-Multiplexed 16bits NAND – Synchronous Burst Read 4x16 bits (1) (2)(3)

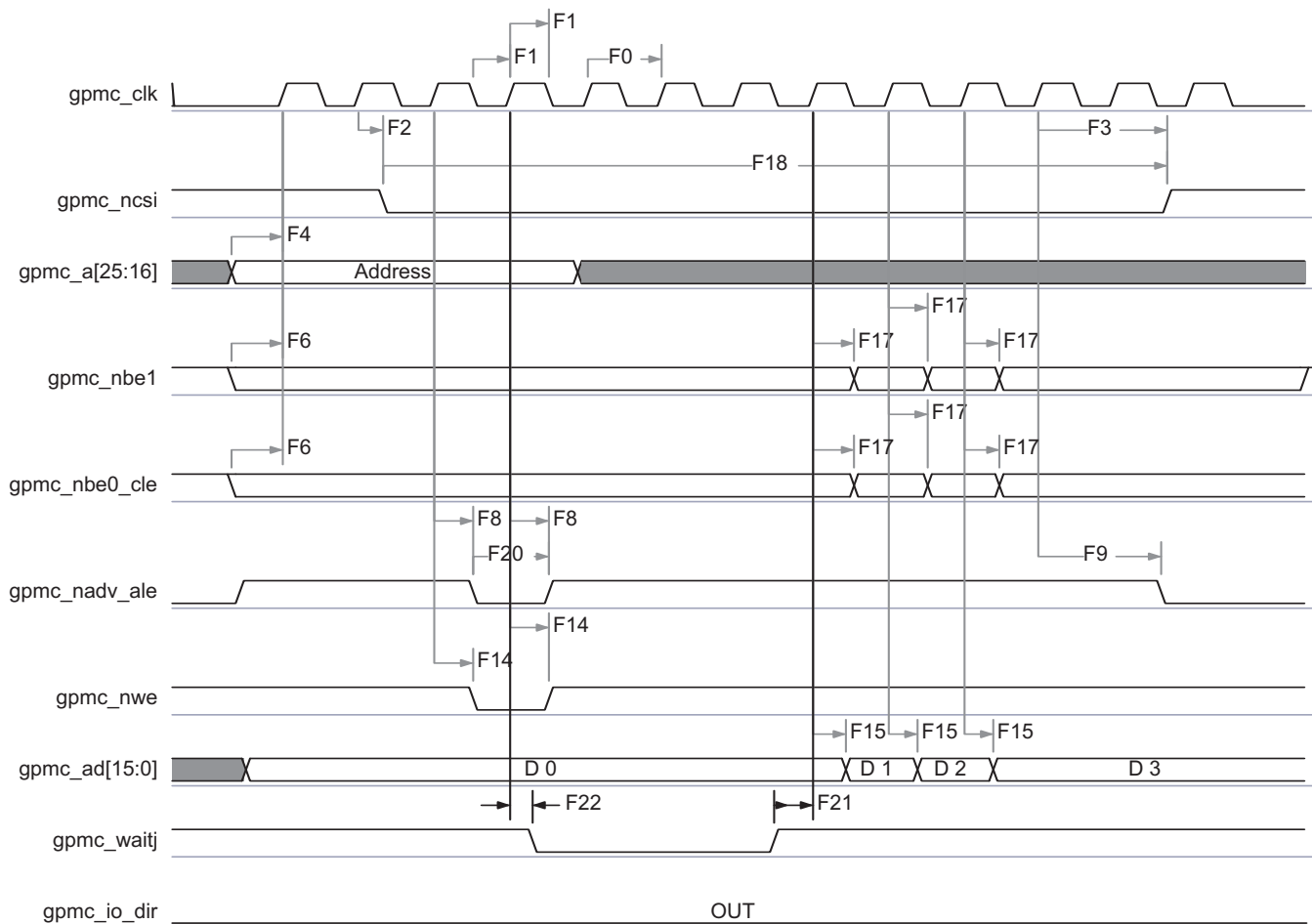
- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.
- (3) Non Multiplexed NAND interface can be used only with a limited address range corresponding to 10 address bits.



SWPS050_GPMC_17

Figure 6-18. GPMC / Multiplexed 16bits NAND – Synchronous Burst Write 4x16 bits ⁽¹⁾ ⁽²⁾

- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
 (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.



SWPS050_GPMC_18

Figure 6-19. XGPMC / Non-Multiplexed 16bits NAND – Synchronous Burst Write 4x16 bits (1) (2) (3)

- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.
- (3) Non Multiplexed NAND interface can be used only with a limited address range corresponding to 10 address bits

6.4.1.3 PSRAM, Synchronous mode, 88.6 MHz, 1.8 V

Table 6-10. PSRAM Timing Conditions — Synchronous mode

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|-------------------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t _R | Input signal rise time | 0.5 | 1.01 | ns |
| t _F | Input signal fall time | 0.46 | 0.97 | ns |
| PCB Conditions⁽¹⁾ | | | | |

- (1) See Table 7-4.
- (2) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

Table 6-10 and Table 6-11 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-11. PSRAM Timing Requirements — Synchronous Mode⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| F12 | $t_{SU(dV-clkH)}$ | Setup time, input data gpmc_ad[15:0] valid before output gpmc_clk high | 2.3 | | ns |
| F13 | $t_{H(clkH-dV)}$ | Hold time, input data gpmc_ad[15:0] valid after output gpmc_clk high | 1.6 | | ns |
| F21 | $t_{SU(waitV-clkH)}$ | Setup time, input wait gpmc_waitx ⁽¹⁾ valid before output gpmc_clk high | 2.3 | | ns |
| F22 | $t_{H(clkH-waitV)}$ | Hold time, input wait gpmc_waitx ⁽¹⁾ valid after output gpmc_clk high | 1.6 | | ns |

(1) In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) See Section 4.3 for CORE OPP voltages.

Table 6-12. PSRAM Switching Characteristics — Synchronous Mode⁽¹⁷⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|-----------------------|--|-------------------------|-------------------------|------|
| | | | MIN | MAX | |
| F0 | $1 / t_{C(CLK)}$ | Frequency ⁽¹⁴⁾ , output gpmc_clk | | 66.5 | MHz |
| F1 | $t_{W(CLKH)}$ | Typical Pulse duration, output gpmc_clk high | 0.5 P ⁽¹²⁾ | | ns |
| F1 | $t_{W(CLKL)}$ | Typical Pulse duration, output gpmc_clk low | 0.5 P ⁽¹²⁾ | | ns |
| | $t_{DC(CLK)}$ | Duty cycle error, output gpmc_clk | | 752 | ps |
| | $t_{J(CLK)}$ | Jitter standard deviation ⁽¹⁵⁾ , output gpmc_clk | | 97.3 | ps |
| | $t_{R(CLK)}$ | Rise time, output gpmc_clk | 0.9 | 1.8 | ns |
| | $t_{F(CLK)}$ | Fall time, output gpmc_clk | 0.9 | 1.6 | ns |
| | $t_{R(DO)}$ | Rise time, output data gpmc_ad[15:0] | 0.9 | 1.8 | ns |
| | $t_{F(DO)}$ | Fall time, output data gpmc_ad[15:0] | 0.9 | 1.6 | ns |
| F2 | $t_{D(CLKH-nCSV)}$ | Delay time, gpmc_clk rising edge to gpmc_ncsx ⁽¹¹⁾ valid | F ⁽⁶⁾ + 0.6 | F ⁽⁶⁾ + 6.1 | ns |
| F3 | $t_{D(CLKH-nCSIV)}$ | Delay time, gpmc_clk rising edge to gpmc_ncsx ⁽¹¹⁾ invalid | E ⁽⁵⁾ + 0.6 | E ⁽⁵⁾ + 6.1 | ns |
| F4 | $t_{D(ADDV-CLK)}$ | Delay time, gpmc_a[25:16] address bus valid to gpmc_clk first edge | B ⁽²⁾ – 6.1 | B ⁽²⁾ – 0.7 | ns |
| F5 | $t_{D(CLKH-ADDIV)}$ | Delay time, gpmc_clk rising edge to gpmc_a[25:16] gpmc address bus invalid | 0.7 | | ns |
| F6 | $t_{D(nBEV-CLK)}$ | Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_clk first edge | B ⁽²⁾ – 4.9 | B ⁽²⁾ + 0.4 | ns |
| F7 | $t_{D(CLKH-nBEIV)}$ | Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 invalid | D ⁽⁴⁾ – 0.4 | D ⁽⁴⁾ + 4.9 | ns |
| F8 | $t_{D(CLKH-nADV)}$ | Delay time, gpmc_clk rising edge to gpmc_nadv_ale valid | G ⁽⁷⁾ + 0.6 | G ⁽⁷⁾ + 6.1 | ns |
| F9 | $t_{D(CLKH-nADVIV)}$ | Delay time, gpmc_clk rising edge to gpmc_nadv_ale invalid | D ⁽⁴⁾ + 0.6 | D ⁽⁴⁾ + 6.1 | ns |
| F10 | $t_{D(CLKH-nOE)}$ | Delay time, gpmc_clk rising edge to gpmc_noe valid | H ⁽⁸⁾ + 0.3 | H ⁽⁸⁾ + 5.1 | ns |
| F11 | $t_{D(CLKH-nOEIV)}$ | Delay time, gpmc rising edge to gpmc_noe invalid | E ⁽⁵⁾ + 0.3 | E ⁽⁵⁾ + 5.1 | ns |
| F14 | $t_{D(CLKH-nWE)}$ | Delay time, gpmc_clk rising edge to gpmc_nwe transition | I ⁽⁹⁾ + 0.6 | I ⁽⁹⁾ + 6.1 | ns |
| F15 | $t_{D(CLKH-Data)}$ | Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition | J ⁽¹⁰⁾ – 0.4 | J ⁽¹⁰⁾ + 4.9 | ns |
| F17 | $t_{D(CLKH-nBE)}$ | Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 transition | J ⁽¹⁰⁾ – 0.4 | J ⁽¹⁰⁾ + 4.9 | ns |
| F18 | $t_{W(nCSV)}$ | Pulse duration, gpmc_ncsx ⁽¹¹⁾ low | Read | A ⁽¹⁾ | ns |
| | | | Write | A ⁽¹⁾ | ns |
| F19 | $t_{W(nBEV)}$ | Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 low | Read | C ⁽³⁾ | ns |
| | | | Write | C ⁽³⁾ | ns |
| F20 | $t_{W(nADV)}$ | Pulse duration, gpmc_nadv_ale low | Read | K ⁽¹³⁾ | ns |
| | | | Write | K ⁽¹³⁾ | ns |
| F23 | $t_{D(CLKH-IODIR)}$ | Delay time, gpmc_clk rising edge to gpmc_io_dir high (IN direction) | H ⁽⁸⁾ + 0.7 | H ⁽⁸⁾ + 5.1 | ns |
| F24 | $t_{D(CLKH-IODIRIV)}$ | Delay time, gpmc rising edge to gpmc_io_dir low (OUT direction) | M ⁽¹⁶⁾ + 0.7 | M ⁽¹⁶⁾ + 5.1 | ns |

- (1) For single read: $A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK$ period.
 For burst read: $A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$ period with n the page burst access number.
 For burst write: $A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$ period with n the page burst access number.
- (2) $B = ClkActivationTime * GPMC_FCLK$
- (3) For single read: $C = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK$
 For burst read: $C = (RdCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$ with n the page burst access number.
 For Burst write: $C = (WrCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$ with n the page burst access number.
- (4) For single read: $D = (RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
 For burst read: $D = (RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
 For burst write: $D = (WrCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
- (5) For single read: $E = (CSRdOffTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
 For burst read: $E = (CSRdOffTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
 For burst write: $E = (CSWrOffTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
- (6) For nCS falling edge (CS activated):
 Case GpmcFCLKDivider = 0:
 $F = 0.5 * CSExtraDelay * GPMC_FCLK$
 Case GpmcFCLKDivider = 1:
 $F = 0.5 * CSExtraDelay * GPMC_FCLK$ if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
 $F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK$
 otherwise
 Case GpmcFCLKDivider = 2:
 $F = 0.5 * CSExtraDelay * GPMC_FCLK$ if ((CSOnTime - ClkActivationTime) is a multiple of 3)
 $F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK$ if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
 $F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK$ if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)
- (7) For ADV falling edge (ADV activated):
 Case GpmcFCLKDivider = 0:
 $G = 0.5 * ADVExtraDelay * GPMC_FCLK$
 Case GpmcFCLKDivider = 1:
 $G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
 $G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$
 otherwise
 Case GpmcFCLKDivider = 2:
 $G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
 $G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
 $G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)
 For ADV rising edge (ADV desactivated) in Reading mode:
 Case GpmcFCLKDivider = 0:
 $G = 0.5 * ADVExtraDelay * GPMC_FCLK$ Case GpmcFCLKDivider = 1:
 $G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
 $G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$
 otherwise
 Case GpmcFCLKDivider = 2:
 $G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
 $G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
 $G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)
 For ADV rising edge (ADV desactivated) in Writing mode:
 Case GpmcFCLKDivider = 0:
 $G = 0.5 * ADVExtraDelay * GPMC_FCLK$
 Case GpmcFCLKDivider = 1:
 $G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
 $G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ otherwise
 Case GpmcFCLKDivider = 2:
 $G = 0.5 * ADVExtraDelay * GPMC_FCLK$ if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
 $G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
 $G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK$ if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)
- (8) For OE falling edge (OE activated) / IO DIR rising edge (IN direction):
 Case GpmcFCLKDivider = 0:
 $H = 0.5 * OEEExtraDelay * GPMC_FCLK$
 Case GpmcFCLKDivider = 1:
 $H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
 $H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$
 otherwise
 Case GpmcFCLKDivider = 2:

- $H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if $((OEOnTime - ClkActivationTime)$ is a multiple of 3)
 $H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if $((OEOnTime - ClkActivationTime - 1)$ is a multiple of 3)
 $H = (2 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if $((OEOnTime - ClkActivationTime - 2)$ is a multiple of 3)
 For OE rising edge (OE deactivated):
 Case GpmcFCLKDivider = 0:
 $H = 0.5 * OEEExtraDelay * GPMC_FCLK$
 Case GpmcFCLKDivider = 1:
 $H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if $(ClkActivationTime$ and $OEOffTime$ are odd) or $(ClkActivationTime$ and $OEOffTime$ are even)
 $H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$
 otherwise
 Case GpmcFCLKDivider = 2:
 $H = 0.5 * OEEExtraDelay * GPMC_FCLK$ if $((OEOffTime - ClkActivationTime)$ is a multiple of 3)
 $H = (1 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if $((OEOffTime - ClkActivationTime - 1)$ is a multiple of 3)
 $H = (2 + 0.5 * OEEExtraDelay) * GPMC_FCLK$ if $((OEOffTime - ClkActivationTime - 2)$ is a multiple of 3)
- (9) For WE falling edge (WE activated):
 Case GpmcFCLKDivider = 0:
 $I = 0.5 * WEEExtraDelay * GPMC_FCLK$
 Case GpmcFCLKDivider = 1:
 $I = 0.5 * WEEExtraDelay * GPMC_FCLK$ if $(ClkActivationTime$ and $WEOnTime$ are odd) or $(ClkActivationTime$ and $WEOnTime$ are even)
 $I = (1 + 0.5 * WEEExtraDelay) * GPMC_FCLK$
 otherwise
 Case GpmcFCLKDivider = 2:
 $I = 0.5 * WEEExtraDelay * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime)$ is a multiple of 3)
 $I = (1 + 0.5 * WEEExtraDelay) * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime - 1)$ is a multiple of 3)
 $I = (2 + 0.5 * WEEExtraDelay) * GPMC_FCLK$ if $((WEOnTime - ClkActivationTime - 2)$ is a multiple of 3)
 For WE rising edge (WE deactivated):
 Case GpmcFCLKDivider = 0:
 $I = 0.5 * WEEExtraDelay * GPMC_FCLK$
 Case GpmcFCLKDivider = 1:
 $I = 0.5 * WEEExtraDelay * GPMC_FCLK$ if $(ClkActivationTime$ and $WEOffTime$ are odd) or $(ClkActivationTime$ and $WEOffTime$ are even)
 $I = (1 + 0.5 * WEEExtraDelay) * GPMC_FCLK$
 otherwise
 Case GpmcFCLKDivider = 2:
 $I = 0.5 * WEEExtraDelay * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime)$ is a multiple of 3)
 $I = (1 + 0.5 * WEEExtraDelay) * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime - 1)$ is a multiple of 3)
 $I = (2 + 0.5 * WEEExtraDelay) * GPMC_FCLK$ if $((WEOffTime - ClkActivationTime - 2)$ is a multiple of 3)
- (10) $J = GPMC_FCLK$ period
- (11) In "gpmc_ncsx", x is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (12) $P = gpmc_clk$ period
- (13) For read: $K = (ADVrdOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
 For write: $K = (ADVWrOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
- (14) Related to the gpmc_clk output clock Maximum and minimum frequency programmable in I/F module by setting the GPMC_CONFIG1_CSx configuration register bit fields GpmcFCLKDivider
- (15) The jitter probability density can be approximated by a Gaussian function.
- (16) $M = (RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK$
 Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behaviour of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or non/multiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behaviour is automatically handled by GPMC controller
- (17) See the [Section 4.3](#) for CORE OPP voltages.

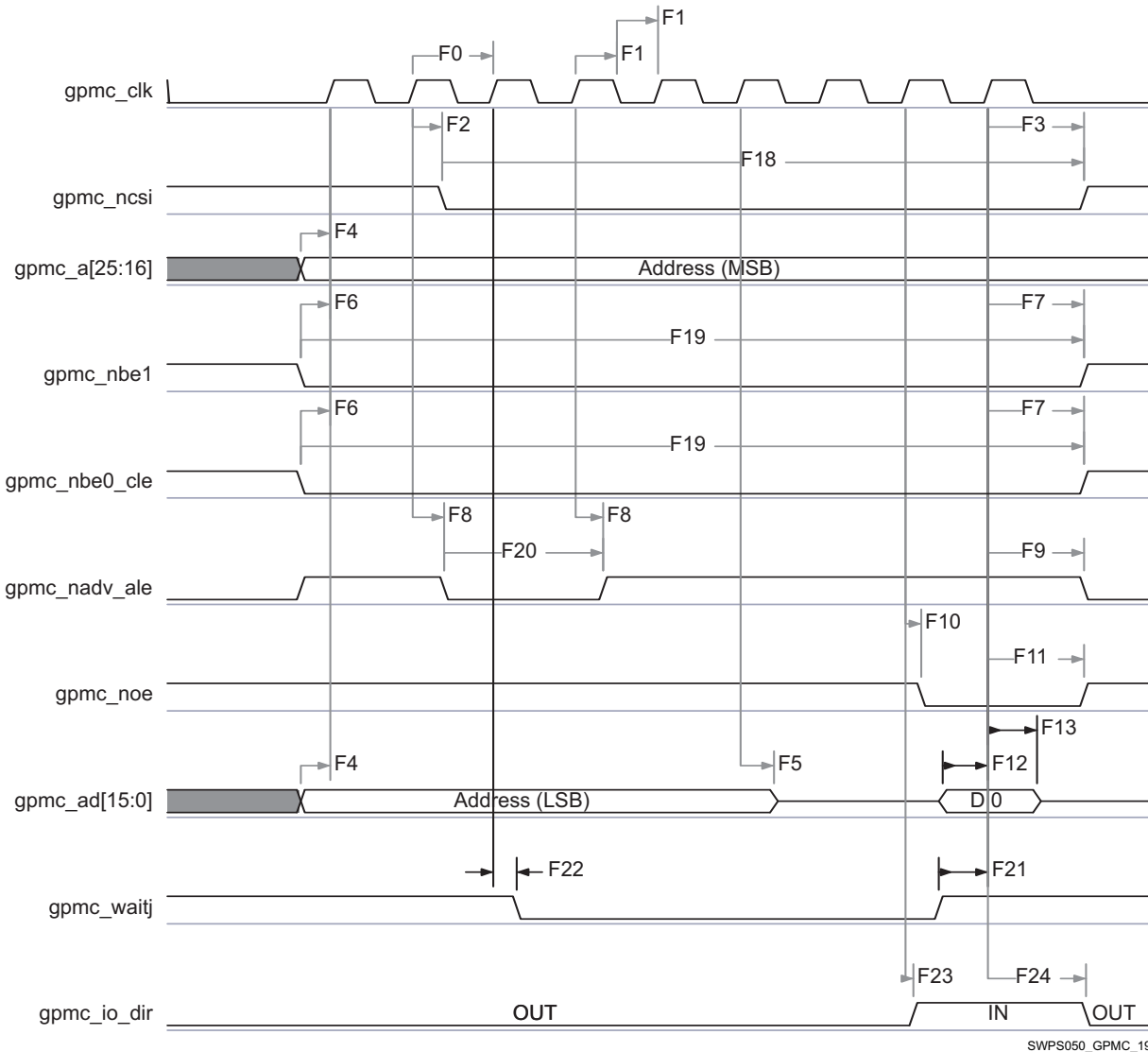
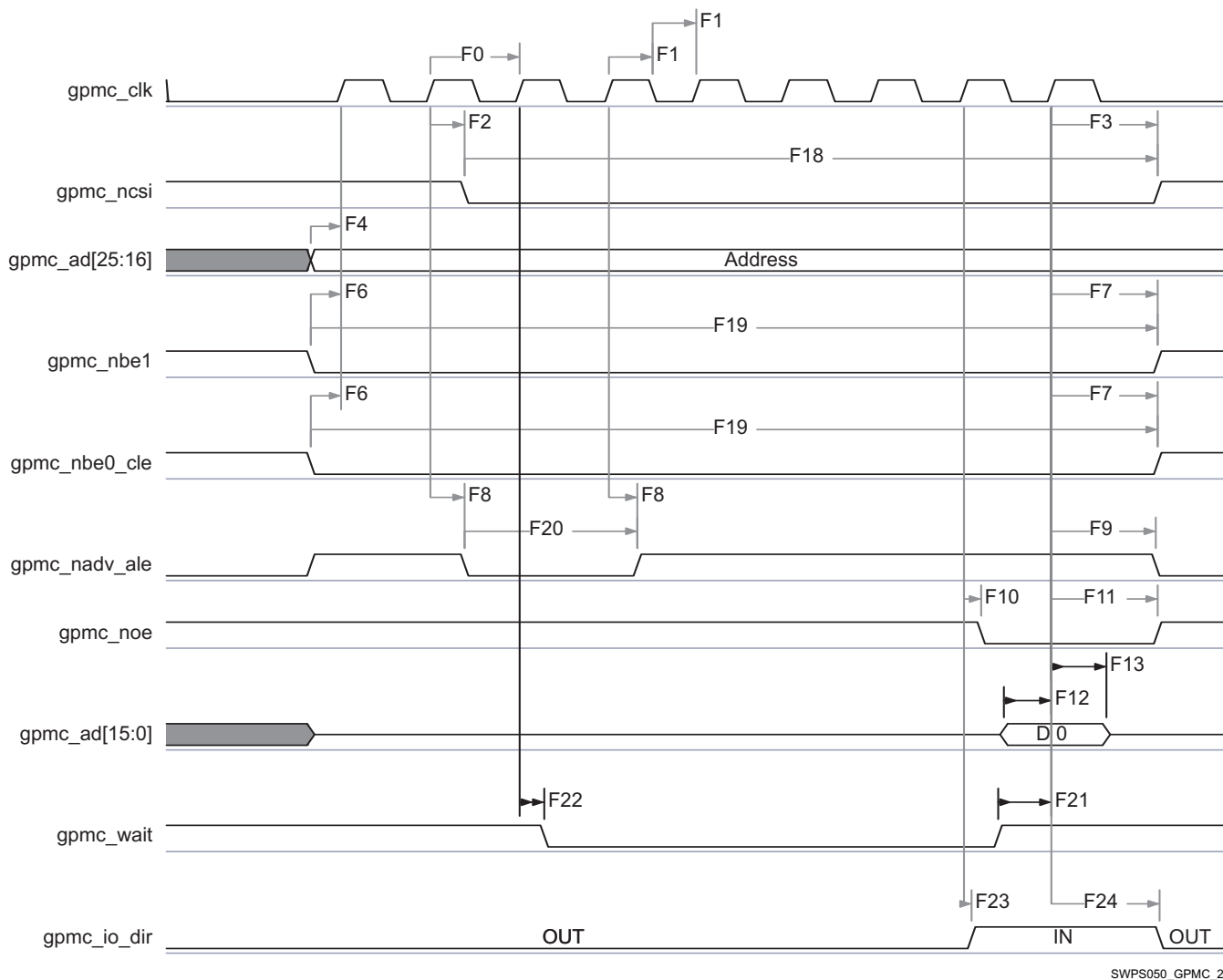


Figure 6-20. GPMC / Multiplexed 16bits PSRAM – Synchronous Single Read ⁽¹⁾⁽²⁾

- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.



SWPS050_GPMC_20

Figure 6-21. GPMC / Non-Multiplexed 16bits PSRAM – Synchronous Single Read⁽¹⁾⁽²⁾⁽³⁾

- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.
- (3) Non Multiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

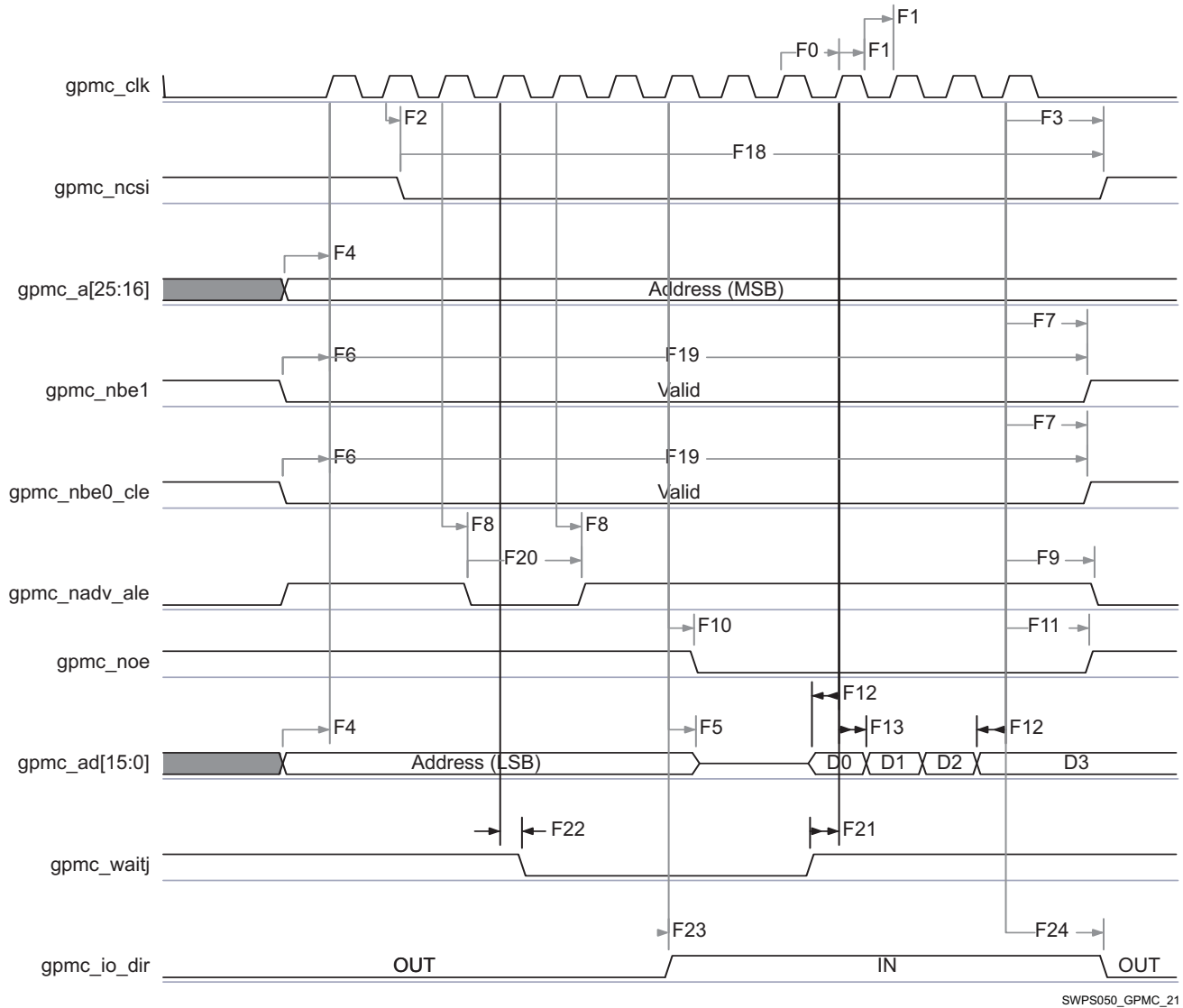


Figure 6-22. GPMC / Multiplexed 16bits PSRAM – Synchronous Burst Read 4x16 bits (1)(2)

- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

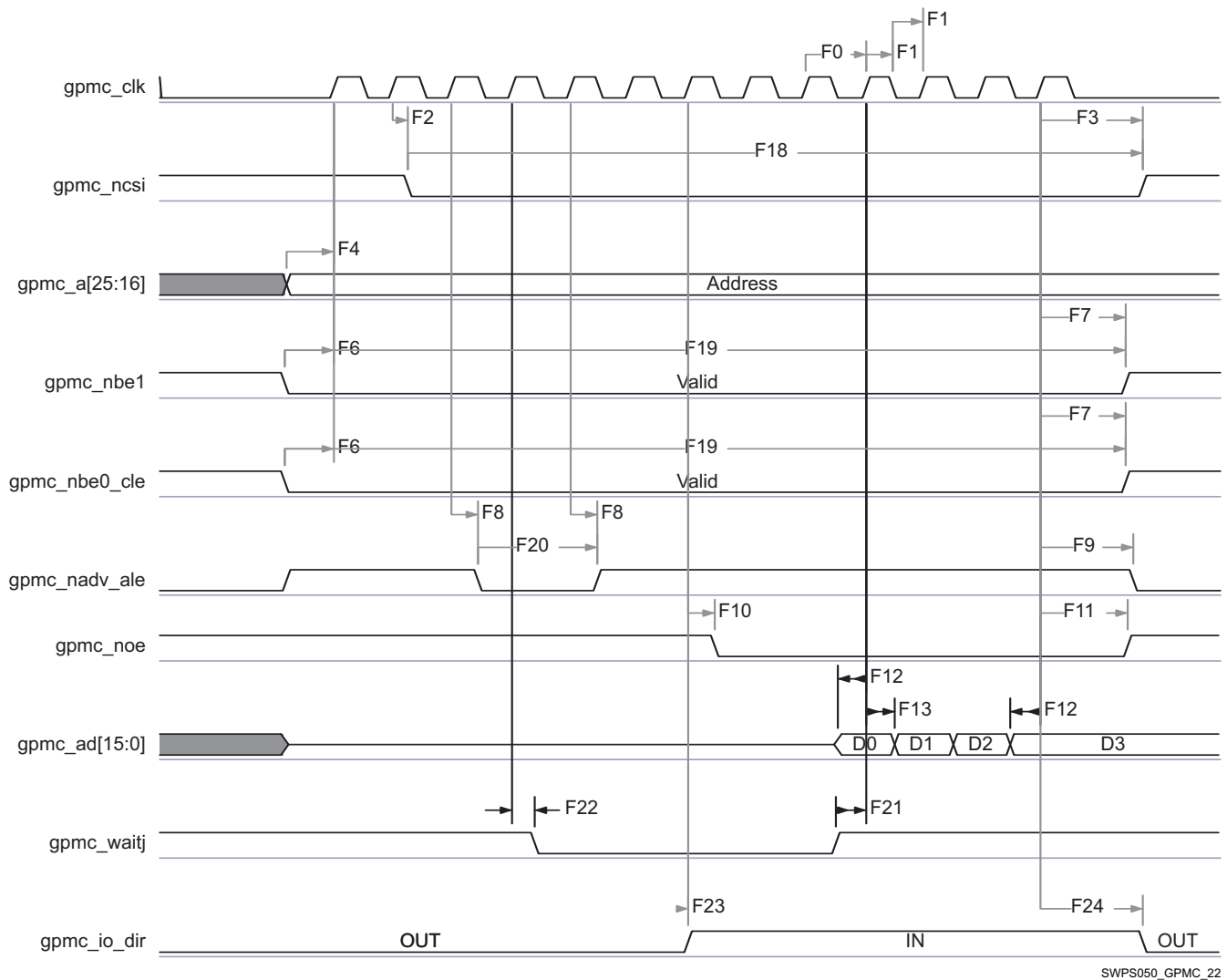
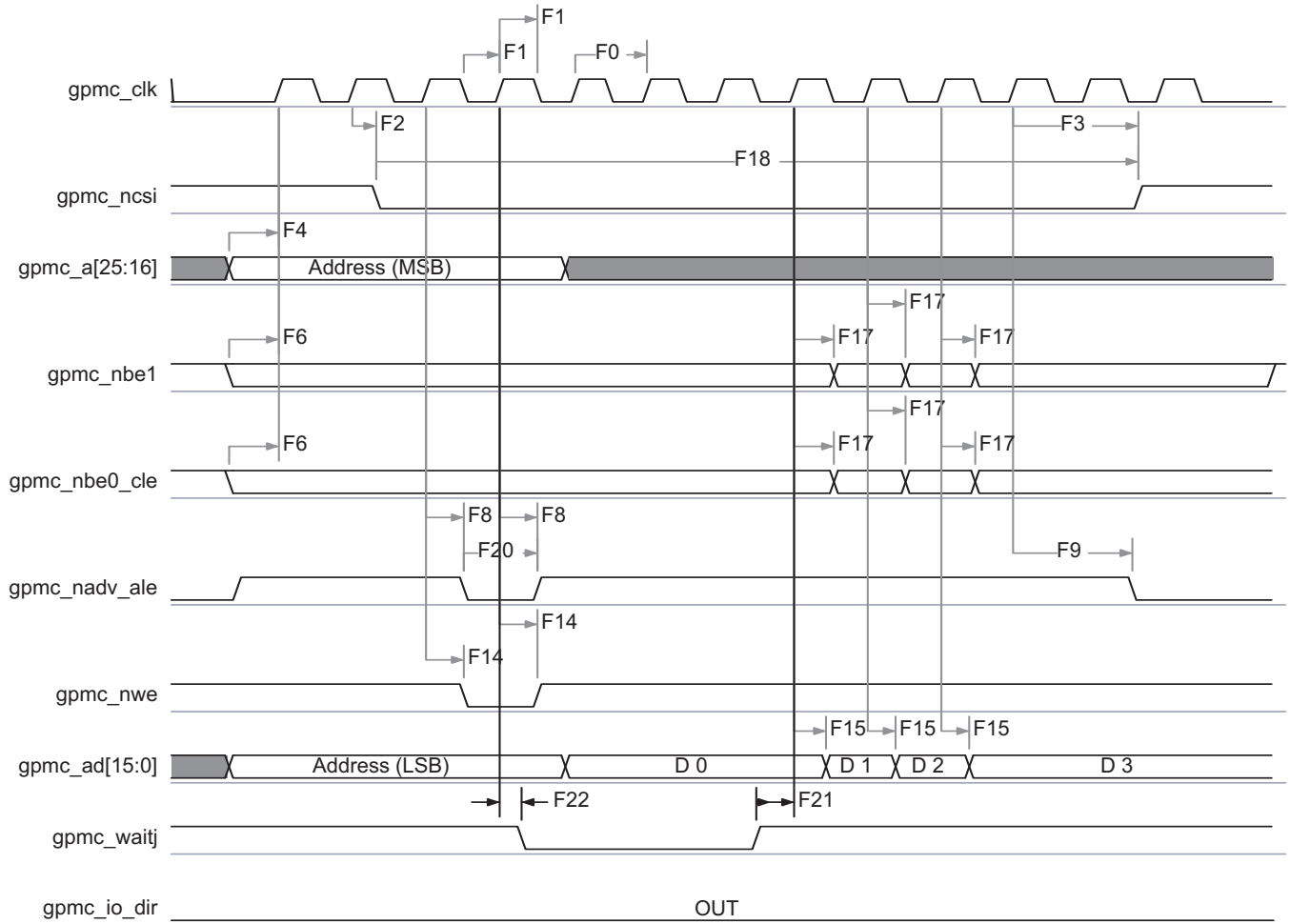


Figure 6-23. GPMC / Non-Multiplexed 16bits PSRAM – Synchronous Burst Read 4x16 bits (1)(2)(3)

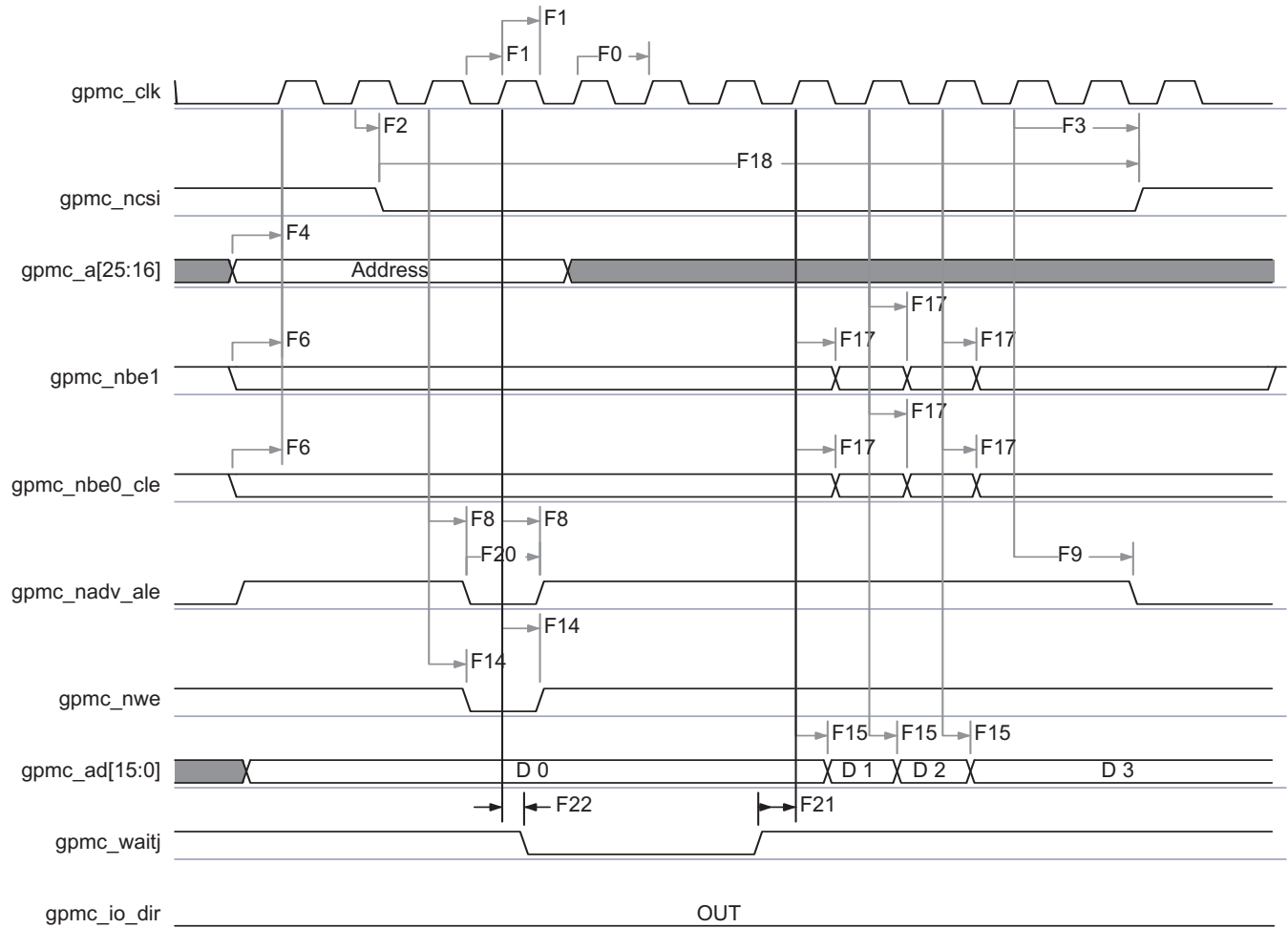
- (1) In **gpmc_ncsi**, *i* is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In **gpmc_waitj**, *x* is equal to 0, 1, 2, 3.
- (3) Non Multiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.



SWPS050_GPMC_23

Figure 6-24. GPMC / Multiplexed 16bits PSRAM – Synchronous Burst Write 4x16 bits (1)(2)

- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.



SWPS050_GPMC_24

Figure 6-25. GPMC / Non-Multiplexed 16bits PSRAM – Synchronous Burst Write 4x16 bits (1)(2)(3)

- (1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.
- (2) In gpmc_waitj, x is equal to 0, 1, 2, 3.
- (3) Non Multiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

6.4.2 External Memory Interface (EMIF)

NOTE

For more information, see the EMIF Controller section of the Device TRM.

The SDRAM controller subsystem module provides connectivity between the processor and external DRAM memory components.

The module includes support for double-data-rate SDRAM (mobile DDR).

DDR3 module embedded in the Device is compliant with the JESD79-3D standard.

For more information on the DDR3 timing requirements and switching characteristics, see the JESD79-3D standard.

NOTE

EMIF I/O (DDR) does support 1.5 V.

6.5 Multimedia Interfaces

6.5.1 Camera Interface

NOTE

For more information on the Imaging Subsystem, see the Device TRM.

The imaging subsystem (ISS) deals with the processing of the pixel data coming from an external image sensor, data from memory. The ISS is a key component for the following multimedia applications: camera viewfinder, video record, and still image capture. The ISS has three serial camera interfaces (primary, secondary, and tertiary) and a parallel interface within the ISS boundary:

- The primary serial interface (CSI2 Port A) is compliant with MIPI CSI-2 protocol with four data lanes.
- The secondary serial interface (CSI2 Port B) is compliant with MIPI CSI-2 protocol with two data lanes.
- The tertiary serial interface (CSI2 Port C) is compliant with MIPI CSI-2 protocol with one data lane.
- The camera parallel interface (CPI) supports up to 16 data lanes.

6.5.1.1 CSI-2 MIPI D-PHY—1.5 V and 1.8 V

The CSI-2 port A is compliant with the MIPI D-PHY RX specification v1.00.00 and the MIPI CSI-2 specification v1.00, with 4 data differential lanes plus 1 clock differential lane in synchronous mode, double data rate:

- 1.5 Gbps (750 MHz) @OPP_NOM for each lane.

The CSI-2 port B is compliant with the MIPI D-PHY RX specification v1.00.00 and the MIPI CSI-2 specification v1.00, with 2 data lanes plus 1 clock lane (differential) in synchronous mode, double data rate:

- 1.5 Gbps (750 MHz) @OPP_NOM for each lane, in synchronous mode.

The CSI-2 port C is compliant with the MIPI D-PHY RX specification v1.00.00 and the MIPI CSI-2 specification v1.00, with 1 data differential lane plus 1 clock differential lane in synchronous mode, double data rate:

- 1.5 Gbps (750 MHz) @OPP_NOM for each lane.

6.5.1.2 Camera Parallel Interface (CPI)—1.8 V

6.5.1.2.1 Image Sensor

The camera parallel interface supports the CPI 16-bit ITU mode, in half-cycle mode (fall to rise), for image sensor 5 Mpix 15 fps (+30% blank margin).

NOTE

Regarding the CPI parallel camera applications, consider that only half-cycle mode in single data rate (SDR) is supported.

Moreover, only the fall-to-rise mode is supported (data generated by a peripheral on falling edge, and captured by OMAP543x on rising edge of the clock).

Table 6-14 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-13. CPI Timing Conditions—Image Sensor

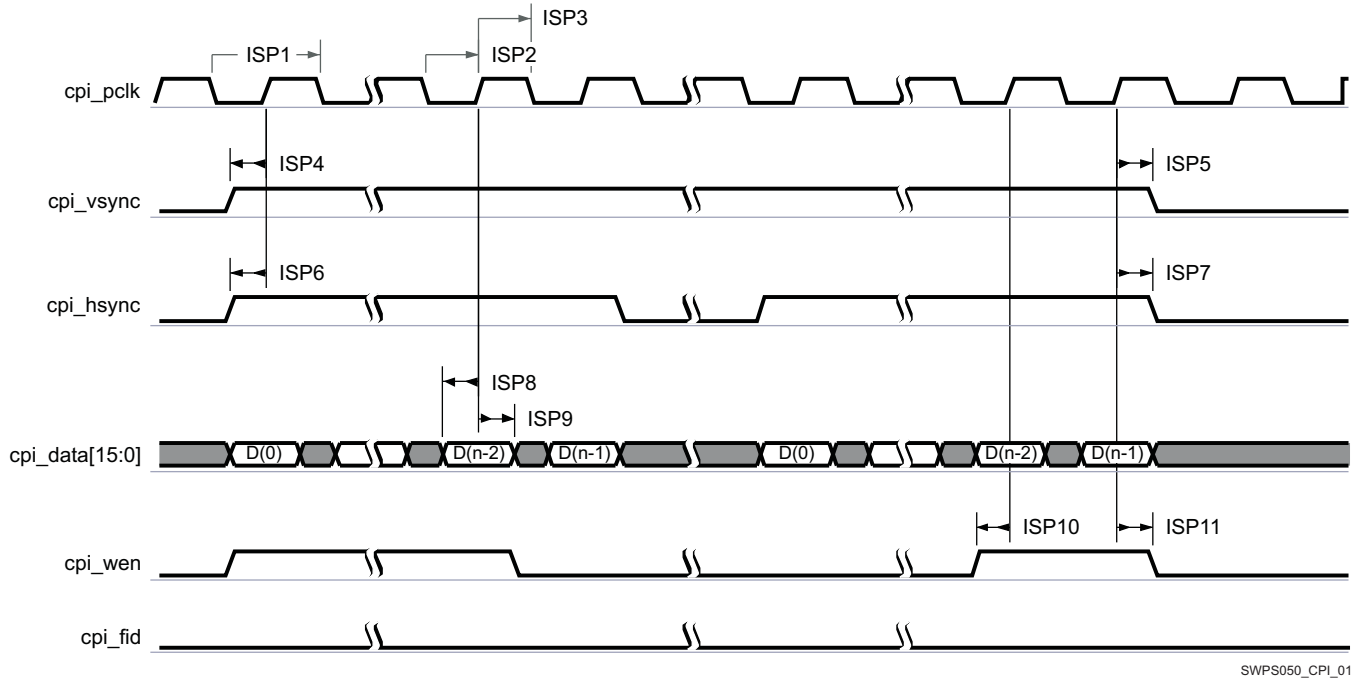
| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---------------------------------------|-------------------------------|-------|-----|------|
| | | MIN | MAX | |
| Input Conditions⁽¹⁾ | | | | |
| t_R | Input signal rise time | 120 | 920 | ps |
| t_F | Input signal fall time | 110 | 830 | ps |
| PCB Conditions | | | | |
| | Number of external peripheral | | 1 | |
| | Trace length | 5 | 20 | cm |
| | Characteristic impedance | 30 | 65 | * |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

Table 6-14. CPI Timing Requirements—Image Sensor⁽⁴⁾⁽⁵⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|---------------------|--|------------------------|-------------------------|------|
| | | | MIN | MAX | |
| ISP1 | $1 / t_{c(pclk)}$ | Frequency ⁽¹⁾ , cpi_pclk CPI input pixel clock | | 97.08 | MHz |
| ISP2 | $t_{w(pclkL)}$ | Typical pulse duration, cpi_pclk low | 0.5 * P ⁽²⁾ | | ns |
| ISP3 | $t_{w(pclkH)}$ | Typical pulse duration, cpi_pclk high | 0.5 * P ⁽²⁾ | | ns |
| | $t_{dc(pclk)}$ | Duty cycle error, cpi_pclk | | 0.5 * P—3.247 | ns |
| | $t_{j(pclk)}$ | Cycle jitter ⁽³⁾ , cpi_pclk | | 0.06 * P ⁽²⁾ | ns |
| ISP4 | $t_{su(vsV-pclk)}$ | Setup time, cpi_vsync valid before cpi_pclk rising edge | 1.76 | | ns |
| ISP5 | $t_{h(pclk-vsV)}$ | Hold time, cpi_vsync valid after cpi_pclk rising edge | 4.16 | | ns |
| ISP6 | $t_{su(hsV-pclk)}$ | Setup time, cpi_hsync valid before cpi_pclk rising edge | 1.76 | | ns |
| ISP7 | $t_{h(pclk-hsV)}$ | Hold time, cpi_hsync valid after cpi_pclk rising edge | 4.16 | | ns |
| ISP8 | $t_{su(dV-pclk)}$ | Setup time, cpi_data[15:0] valid before cpi_pclk rising edge | 1.76 | | ns |
| ISP9 | $t_{h(pclk-dV)}$ | Hold time, cpi_data[15:0] valid after cpi_pclk rising edge | 4.16 | | ns |
| ISP10 | $t_{su(wenV-pclk)}$ | Setup time, cpi_wen valid before cpi_pclk rising edge | 1.76 | | ns |
| ISP11 | $t_{h(pclk-wenV)}$ | Hold time, cpi_wen valid after cpi_pclk rising edge | 4.16 | | ns |
| ISP12 | $t_{su(fidV-pclk)}$ | Setup time, cpi_fid valid before cpi_pclk rising edge | 1.76 | | ns |
| ISP13 | $t_{h(pclk-fidV)}$ | Hold time, cpi_fid valid after cpi_pclk rising edge | 4.16 | | ns |

- (1) Related with the input maximum frequency supported by the ISP module.
- (2) P = cpi_pclk period in ns
- (3) Maximum cycle jitter supported by cpi_pclk input pixel clock.
- (4) The timing requirements are assured up to the cycle jitter and duty cycle error conditions specified.
- (5) See [Section 4.3](#) for CORE OPP voltages.



SWPS050_CPI_01

Figure 6-26. CPI—Image Sensor—1.8-V Progressive Mode⁽¹⁾

(1) $n = 16$

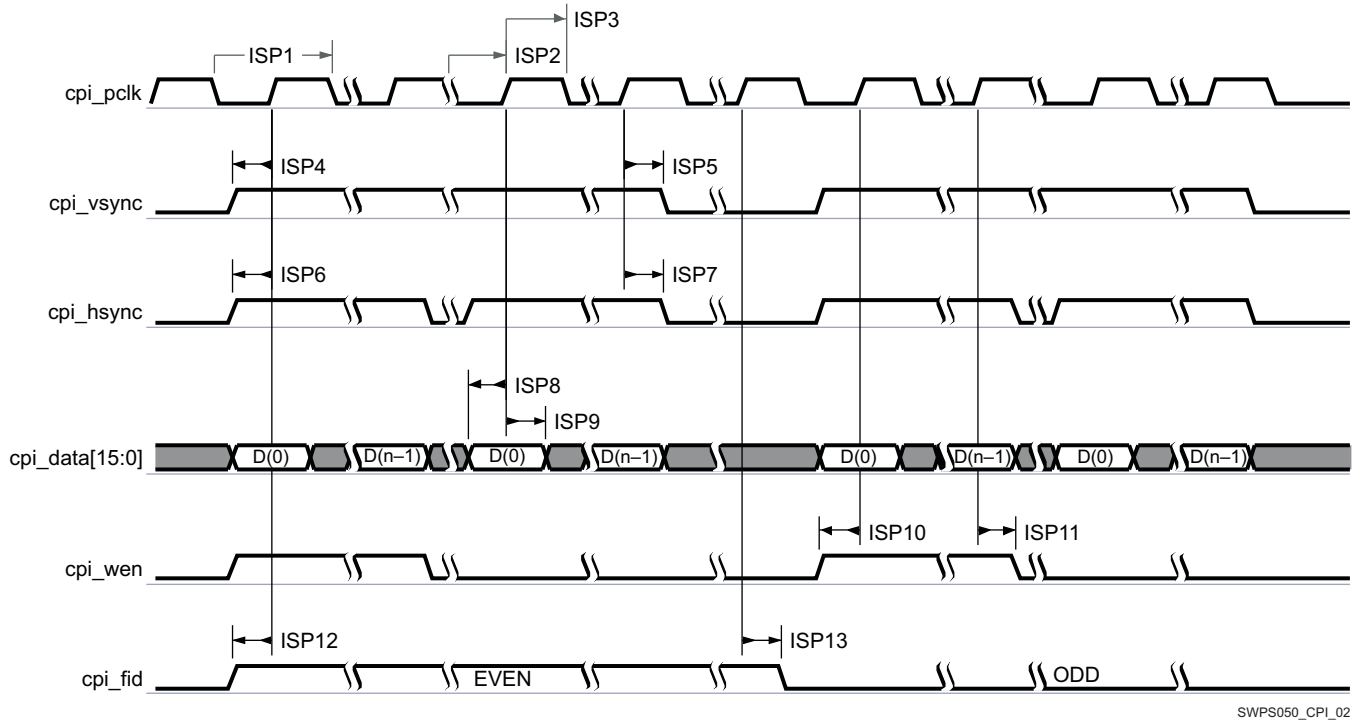


Figure 6-27. CPI—Image Sensor—1.8-V Interlaced Mode⁽¹⁾

(1) n = 16

6.5.1.2.2 HDMI Receiver

The camera parallel interface supports the CPI 16-bit ITU mode, in half-cycle mode (fall to rise), for HDMI receiver 1080p 60fps YUV422.

NOTE

Regarding the CPI parallel camera applications, consider that only half-cycle mode in SDR is supported. Moreover, only the fall-to-rise mode is supported (data generated by a peripheral on falling edge, and captured by the OMAP543x device on rising edge of the clock).

Table 6-16 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-15. CPI Timing Conditions—HDMI Receiver

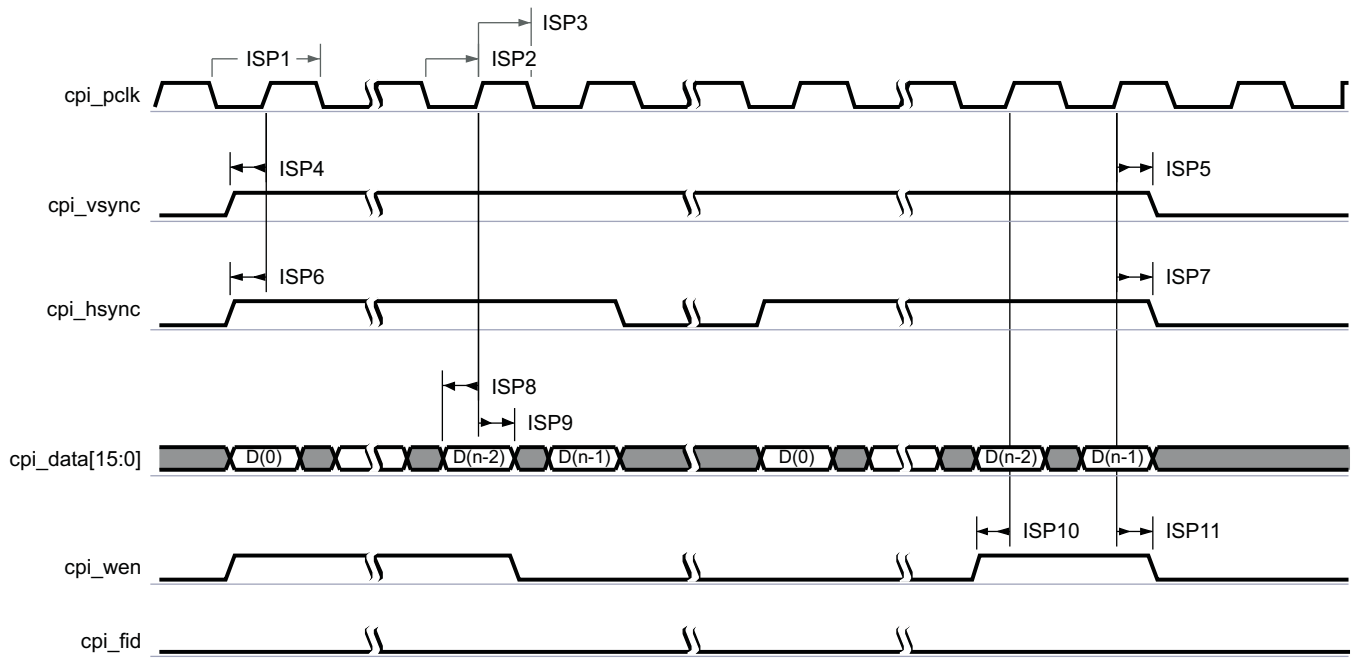
| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---------------------------------------|-------------------------------|-------|-----|----------|
| | | MIN | MAX | |
| Input Conditions⁽¹⁾ | | | | |
| t_R | Input signal rise time | 120 | 920 | ps |
| t_F | Input signal fall time | 110 | 830 | ps |
| PCB Conditions | | | | |
| | Number of external peripheral | | 1 | |
| | Trace length | 2 | 5 | cm |
| | Characteristic impedance | 30 | 65 | Ω |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

Table 6-16. CPI Timing Requirements—HDMI Receiver⁽⁴⁾⁽⁵⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|---------------------|--|------------------------|-------------------------|------|
| | | | MIN | MAX | |
| ISP1 | $1 / t_{c(pclk)}$ | Frequency ⁽¹⁾ , cpi_pclk CPI input pixel clock | | 148.5 | MHz |
| ISP2 | $t_{w(pclkL)}$ | Typical pulse duration, cpi_pclk low | 0.5 * P ⁽²⁾ | | ns |
| ISP3 | $t_{w(pclkH)}$ | Typical pulse duration, cpi_pclk high | 0.5 * P ⁽²⁾ | | ns |
| | $t_{dc(pclk)}$ | Duty cycle error, cpi_pclk | | 0.5 * P—3.247 | ns |
| | $t_{j(pclk)}$ | Cycle jitter ⁽³⁾ , cpi_pclk | | 0.06 * P ⁽²⁾ | ns |
| ISP4 | $t_{su(vsV-pclk)}$ | Setup time, cpi_vsync valid before cpi_pclk rising edge | 0.27 | | ns |
| ISP5 | $t_{h(pclk-vsV)}$ | Hold time, cpi_vsync valid after cpi_pclk rising edge | 2.67 | | ns |
| ISP6 | $t_{su(hsV-pclk)}$ | Setup time, cpi_hsync valid before cpi_pclk rising edge | 0.27 | | ns |
| ISP7 | $t_{h(pclk-hsV)}$ | Hold time, cpi_hsync valid after cpi_pclk rising edge | 2.67 | | ns |
| ISP8 | $t_{su(dV-pclk)}$ | Setup time, cpi_data[15:0] valid before cpi_pclk rising edge | 0.27 | | ns |
| ISP9 | $t_{h(pclk-dV)}$ | Hold time, cpi_data[15:0] valid after cpi_pclk rising edge | 2.67 | | ns |
| ISP10 | $t_{su(wenV-pclk)}$ | Setup time, cpi_wen valid before cpi_pclk rising edge | 0.27 | | ns |
| ISP11 | $t_{h(pclk-wenV)}$ | Hold time, cpi_wen valid after cpi_pclk rising edge | 2.67 | | ns |
| ISP12 | $t_{su(fidV-pclk)}$ | Setup time, cpi_fid valid before cpi_pclk rising edge | 0.27 | | ns |
| ISP13 | $t_{h(pclk-fidV)}$ | Hold time, cpi_fid valid after cpi_pclk rising edge | 2.67 | | ns |

- (1) Related with the input maximum frequency supported by the ISP module.
- (2) P = cpi_pclk period in ns
- (3) Maximum cycle jitter supported by cpi_pclk input pixel clock.
- (4) The timing requirements are assured up to the cycle jitter and duty cycle error conditions specified.
- (5) See Section 4.3 for CORE OPP voltages.



SWPS050_CPI_01

Figure 6-28. CPI—HDMI Receiver—1.8-V Progressive Mode⁽¹⁾

(1) n = 16

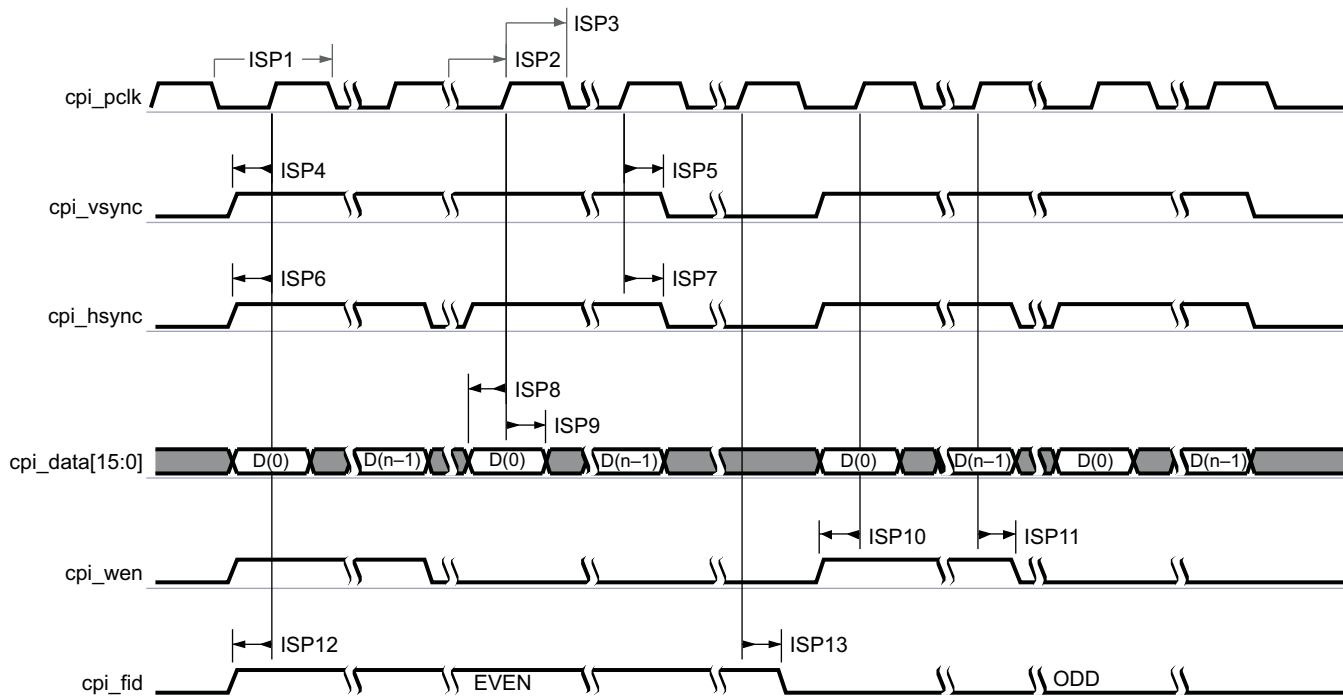


Figure 6-29. CPI—HDMI Receiver —1.8-V Interlaced Mode⁽¹⁾

(1) n = 16

6.5.2 Display Interface

NOTE

For more information, see the Display Subsystem chapter in the Device TRM.

The display subsystem (DSS) provides the logic to display a video frame from the memory frame buffer on a liquid-crystal display (LCD) panel or TV set.

The display subsystem has three interfaces for LCD output:

- DSI Port A and Port C (display serial interface) supporting MIPI DSI-1 protocol.
- RFBI (remote frame buffer interface) supporting MIPI DBI 2.0 protocol.
- DISPC supporting MIPI DPI 2.0 protocol.

The display subsystem has two interfaces for TV output:

- DISPC supporting MIPI DPI 2.0 protocol.
- HDMI (high-definition multimedia interface)

6.5.2.1 Display Controller (DISPC)

NOTE

For more information, see the Display Subsystem / Display Controller section of the Device TRM.

The DISPC interface consists of:

- 24-bit data bus (data[23:0])
- Horizontal synchronization signal (HSYNC)
- Vertical synchronization signal (VSYNC)
- Data enable (DE)
- Pixel clock (PCLK)

This interface is compliant with MIPI DPI standard revision 2.0 and delivers the parallel pixel and synchronization signals for LCD panel or TV set.

6.5.2.1.1 DISPC—MIPI DPI 24 Bits for Display Extension—1.8 V

For DISPC PCB requirements and IO programming, see [Table 7-29](#).

[Table 6-17](#) assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-17. DISPC Switching Characteristics—MIPI DPI 24 Bits for Display Extension⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|-----------------------|---|------------------------|-----|------|
| | | | MIN | MAX | |
| D1 | $1 / t_{c(pclk)}$ | Frequency, output pixel clock disp_c_pclk | | 170 | MHz |
| D2 | $t_{w(pclkL)}$ | Typical pulse duration, output pixel clock disp_c_pclk low | 0.5 * P ⁽¹⁾ | | ns |
| D3 | $t_{w(pclkH)}$ | Typical pulse duration, output pixel clock disp_c_pclk high | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{dc(pclk)}$ | Duty cycle error, output pixel clock disp_c_pclk | | 294 | ps |
| | $t_{j(pclk)}$ | Jitter standard deviation ⁽²⁾ , output pixel clock disp_c_pclk | | 39 | ps |
| | $t_{R(pclk)}$ | Rise time, output pixel clock disp_c_pclk | | 661 | ps |
| | $t_{F(pclk)}$ | Fall time, output pixel clock disp_c_pclk | | 670 | ps |
| D4 | $t_{d(pclkA-vsyncV)}$ | Delay time, output pixel clock disp_c_pclk transition to output vertical synchronization disp_c_vsync valid | -1653 | 153 | ps |
| | $t_{R(vsync)}$ | Rise time, output vertical synchronization disp_c_vsync | | 661 | ps |

Table 6-17. DISPC Switching Characteristics—MIPI DPI 24 Bits for Display Extension⁽³⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|-----------------------|---|---------|-----|------|
| | | | MIN | MAX | |
| | $t_{F(vsync)}$ | Fall time, output vertical synchronization dispc_vsync | | 670 | ps |
| D5 | $t_{d(pclkA-hsyncV)}$ | Delay time, output pixel clock dispc_pclk transition to output horizontal synchronization dispc_hsync valid | -1653 | 153 | ps |
| | $t_{R(hsync)}$ | Rise time, output horizontal synchronization dispc_hsync | | 661 | ps |
| | $t_{F(hsync)}$ | Fall time, output horizontal synchronization dispc_hsync | | 670 | ps |
| D6 | $t_{d(pclkA-dV)}$ | Delay time, output pixel clock dispc_pclk transition to output data dispc_data[23:0] valid | -1653 | 153 | ps |
| | $t_{R(d)}$ | Rise time, output data dispc_data[23:0] | | 661 | ps |
| | $t_{F(d)}$ | Fall time, output data dispc_data[23:0] | | 670 | ps |
| D7 | $t_{d(pclkA-deV)}$ | Delay time, output pixel clock dispc_pclk transition to output data enable dispc_de valid | -1653 | 153 | ps |
| | $t_{R(de)}$ | Rise time, output data enable dispc_de | | 661 | ps |
| | $t_{F(de)}$ | Fall time, output data enable dispc_de | | 670 | ps |
| D8 | $t_{d(pclkA-fidV)}$ | Delay time, output pixel clock dispc_pclk transition to output field ID dispc_fid valid | -1653 | 153 | ps |
| | $t_{R(fid)}$ | Rise time, output field ID dispc_fid | | 661 | ps |
| | $t_{F(fid)}$ | Fall time, output field ID dispc_fid | | 670 | ps |

(1) P = output dispc_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See [Section 4.3](#) for CORE OPP voltages.

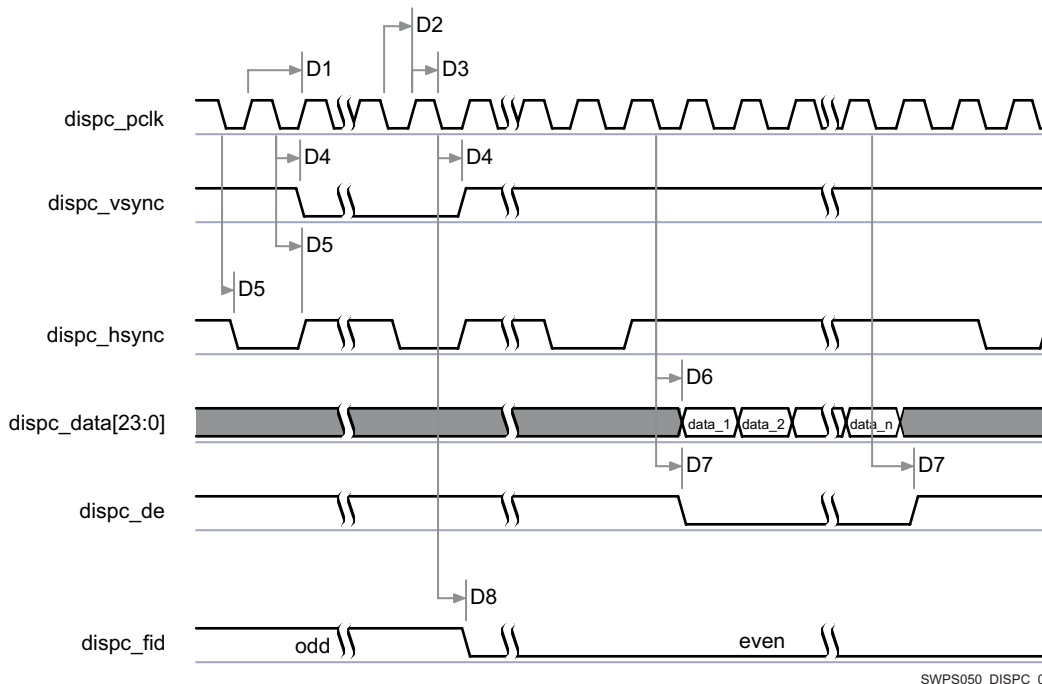


Figure 6-30. DISPC—MIPI DPI 24 Bits for Display Extension^{(1) (2)(3)}

- (1) The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.
- (2) The polarity and the pulse width of dispc_hsync and dispc_vsync are programmable, refer to the DISPC section of the Device TRM.
- (3) The dispc_pclk frequency can be configured, refer to the DISPC section of the Device TRM.

6.5.2.2 DSS—Remote Frame Buffer Interface (RFBI) Applications—1.8 V

6.5.2.2.1 DSS—Remote Frame Buffer Interface (RFBI) Applications—Pico DLP

NOTE

For more information, see the Display Subsystem / Remote Frame Buffer Interface section of the Device TRM.

The RFBI module is part of the display subsystem that provides the logic to display a picture from the memory frame buffer (SDRAM or SRAM) on an LCD panel.

For RFBI PCB requirements and IO programming, see [Table 7-30](#).

[Table 6-18](#) assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-18. DSS—RFBI Switching Characteristics—Pico DLP⁽⁹⁾

| PARAMETER | | OPP_NOM | | UNIT |
|-----------------------------------|--|------------------|-----|------|
| | | MIN | MAX | |
| $t_w(\text{rfbi_weH})$ | Pulse duration, output write enable rfb_i_we high | A ⁽¹⁾ | | ns |
| $t_w(\text{rfbi_weL})$ | Pulse duration, output write enable rfb_i_we low | B ⁽²⁾ | | ns |
| $t_d(\text{rfbi_a0-rfb_weL})$ | Delay time, output command/data control rfb_i_a0 transition to output write enable rfb_i_we low | C ⁽³⁾ | | ns |
| $t_d(\text{rfbi_weH-rfb_a0})$ | Delay time, output write enable rfb_i_we high to output command/data control rfb_i_a0 transition | D ⁽⁴⁾ | | ns |
| $t_d(\text{rfbi_csx-rfb_weL})$ | Delay time, output chip select rfb_i_cs0 low to output write enable rfb_i_we low | E ⁽⁵⁾ | | ns |
| $t_d(\text{rfbi_weH-rfb_csxH})$ | Delay time, output write enable rfb_i_we high to output chip select rfb_i_cs0 high | F ⁽⁶⁾ | | ns |

Table 6-18. DSS—RFBI Switching Characteristics—Pico DLP⁽⁹⁾ (continued)

| PARAMETER | | OPP_NOM | | UNIT |
|---------------------------|--|------------------|-----|------|
| | | MIN | MAX | |
| $t_{d(\text{dataV})}$ | Output data rfb_data[n:0] ⁽⁸⁾ valid | G ⁽⁷⁾ | | ns |
| $t_{d(\text{Skew})}$ | Skew between output write enable falling rfb_we and output data rfb_data[n:0] ⁽⁸⁾ high or low | 14.3 | | ns |
| $t_{R(\text{rfbi_we})}$ | Rise time, output write enable rfb_we | | 2 | ns |
| $t_{F(\text{rfbi_we})}$ | Fall time, output write enable rfb_we | | 2 | ns |
| $t_{R(\text{rfbi_a0})}$ | Rise time, output command/data control rfb_a0 | | 2 | ns |
| $t_{F(\text{rfbi_a0})}$ | Fall time, output command/data control rfb_a0 | | 2 | ns |
| $t_{R(\text{rfbi_csx})}$ | Rise time, output chip select rfb_cs0 | | 2 | ns |
| $t_{F(\text{rfbi_csx})}$ | Fall time, output chip select rfb_cs0 | | 2 | ns |
| $t_{R(\text{rfbi_da})}$ | Rise time, output data rfb_data[n:0] ⁽⁸⁾ | | 2 | ns |
| $t_{F(\text{rfbi_da})}$ | Fall time, output data rfb_data[n:0] ⁽⁸⁾ | | 2 | ns |

(1) $A = (\text{WeCycleTime} - \text{WeOffTime}) * (\text{TimeParaGranularity} + 1) * \text{L3CLK}$

(2) $B = (\text{WeOffTime} - \text{WeOnTime}) * (\text{TimeParaGranularity} + 1) * \text{L3CLK}$

(3) $C = (\text{WeOnTime}) * (\text{TimeParaGranularity} + 1) * \text{L3CLK}$

(4) $D = (\text{WeCycleTime} + \text{CsPulseWidth} - \text{WeOffTime}) * (\text{TimeParaGranularity} + 1) * \text{L3CLK}$

(5) $E = (\text{WeOnTime} - \text{CsOnTime}) * (\text{TimeParaGranularity} + 1) * \text{L3CLK}$

(6) $F = (\text{CsOffTime} - \text{WeOffTime}) * (\text{TimeParaGranularity} + 1) * \text{L3CLK}$

(7) $G = (\text{WeCycleTime}) * (\text{TimeParaGranularity} + 1) * \text{L3CLK}$

(8) rfb_data[n:0], n up to 15

(9) See [Section 4.3](#) for CORE OPP voltages.

Table 6-19. DSS—RFBI Registers Configuration—LCD Panel⁽¹⁾

| DESCRIPTION | REGISTER and BIT FIELD | BIT |
|---|----------------------------------|---------|
| CS signal assertion time from start access time | RFBI_ONOFF_TIME and CSONTIME | [3:0] |
| CS signal de-assertion time from start access time | RFBI_ONOFF_TIME and CSOFFTIME | [9:4] |
| WE signal assertion time from start access time | RFBI_ONOFF_TIME and WEONTIME | [13:10] |
| WE signal de-assertion time from start access time | RFBI_ONOFF_TIME and WEOFFTIME | [19:14] |
| Write cycle time | RFBI_CYCLE_TIME and WECYCLETIME | [5:0] |
| CS pulse width | RFBI_CYCLE_TIME and CSPULSEWIDTH | [17:12] |
| Write-to-write CS pulse width enable | RFBI_CYCLE_TIME and WWENABLE | [20] |
| From start access time to CLK rising edge used for the first data capture | RFBI_CYCLE_TIME and ACCESSTIME | [27:22] |
| Latencies multiplied by 2 | RFBI_CONFIG and TIMEGRANULARITY | [4] |

(1) For more information on the RFBI registers, see the Display Subsystem / Remote Frame Buffer Interface section of the Device TRM.

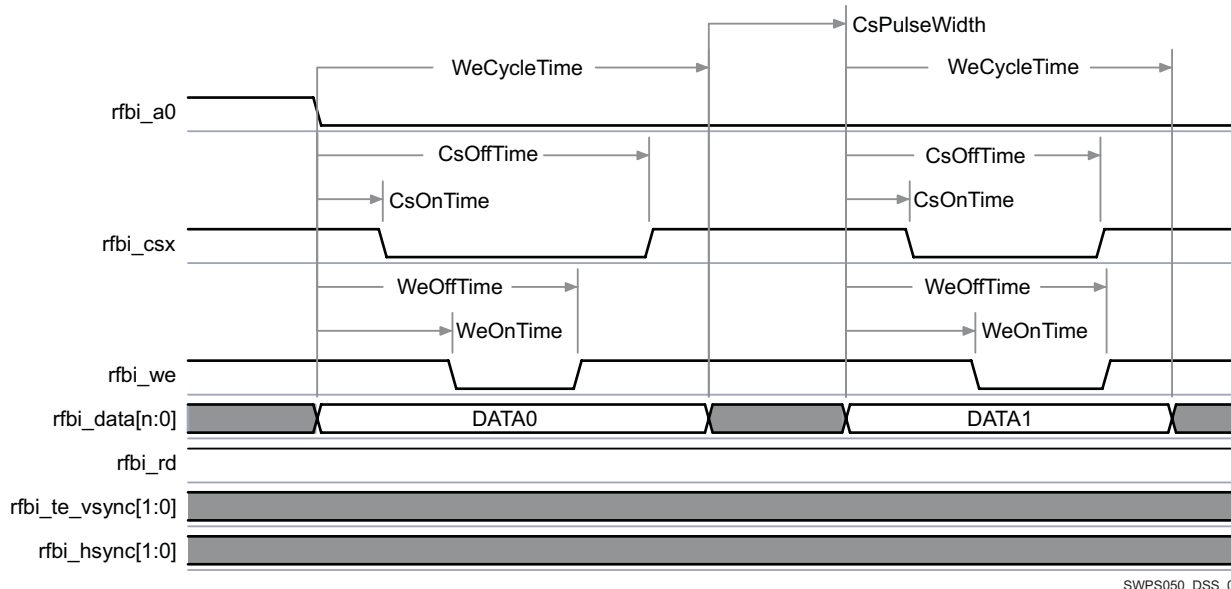


Figure 6-31. DSS—RFBI—Command / Data Write—Pico DLP⁽¹⁾⁽²⁾

- (1) In rfb_i_csx, x is equal to 0.
- (2) rfb_i_data[n:0], n up to 15

6.5.2.3 Display Serial Interface—DSI-1 MIPI D-PHY—1.5 V and 1.8 V

The DSI-1 port A and port C (display serial interface) are compliant with the MIPI D-PHY TX specification v1.00.00 and the MIPI DSI v01.01.00 standard and support these features:

- Four data lane complex input or output in addition to the clock lane
- Bidirectional data link support (only one data lane is used in reverse direction in command mode from display to OMAP for status and control)
- Video mode and command mode support
- Data interleaving support

DSI-1 port A and DSI-1 port C interfaces, with 4 data differential lanes plus 1 clock differential lane, in synchronous mode, double data rate, support the following data bit rates:

- @OPP_NOM:
 - 1.255 Gbps ($f_{c(\text{clk})} = 627.5 \text{ MHz}$) for each lane.
 - With $t_{UI(\text{NOM})} = 0.796 \text{ ps}$, $t_{UI(\text{NOM})}$ is the minimum unit interval, equal to $1 / (2 * f_{c(\text{clk})})$.
 - With $t_{UI(\text{INST,MIN})} = 0.716 \text{ ps}$, $t_{UI(\text{INST,MIN})}$ is the minimum instantaneous bit duration, equal to $0.9 * t_{UI(\text{NOM})}$.

Each DSI-1 interface supports the following display applications:

- WUXGA (Wide Ultra eXtended Graphics Array), 1920x1200, 60fps, 24bpp
- Up to QSXGA (Quad Super eXtended Graphics Array), 2560x1600, 30fps, 24bpp

6.5.2.4 High Definition Multimedia Interface (HDMI)

NOTE

For more information on HDMI, please contact your TI representative.

6.6 Serial and Parallel Communication Interfaces

6.6.1 Multichannel Buffered Serial Port (McBSP), 1.8 V

NOTE

For more information, see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) / McBSP Functional Description section of the Device TRM.

The multichannel buffered serial port (McBSP) provides a full duplex direct serial interface between OMAP chip and other devices (digital baseband), audio and voice codec, etc. It can accommodate a wide range of peripherals and clocked frame oriented protocols (I2S, PCM, TDM) due to its high level of versatility.

6.6.1.1 McBSP1, McBSP2, and McBSP3—I2S/PCM—1 Peripheral—SDR—12.288 MHz—1.8 V

Table 6-20. McBSP1, McBSP2, and McBSP3 Timing Conditions—I2S/PCM

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 400 | 6500 | ps |
| t_F | Input signal fall time | 400 | 6500 | ps |
| Output Condition | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1, POWER NAME \[9\]](#) column with the ball name.

[Table 6-21](#) through [Table 6-24](#) assume testing over the recommended operating conditions and electrical characteristic conditions below.

6.6.1.1.1 McBSP1, McBSP2, and McBSP3—I2S/PCM—Master Mode

Table 6-21. McBSP1, McBSP2, and McBSP3 Timing Requirements—I2S/PCM—Master Mode⁽¹⁾⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|---------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| BM5 | $t_{su}(drV-clkAE)$ | Setup time, abemcbspy_dr ⁽²⁾ valid before abemcbspy_clkx ⁽²⁾ active edge | 4.6 | | ns |
| BM6 | $t_h(clkAE-drV)$ | Hold time, abemcbspy_dr ⁽²⁾ valid after abemcbspy_clkx ⁽²⁾ active edge | 0.7 | | ns |

(1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(2) In abemcbspy_dr and abemcbspy_clkx, y is equal to 1, 2, or 3.

(3) See [Section 4.3](#) for CORE OPP voltages.

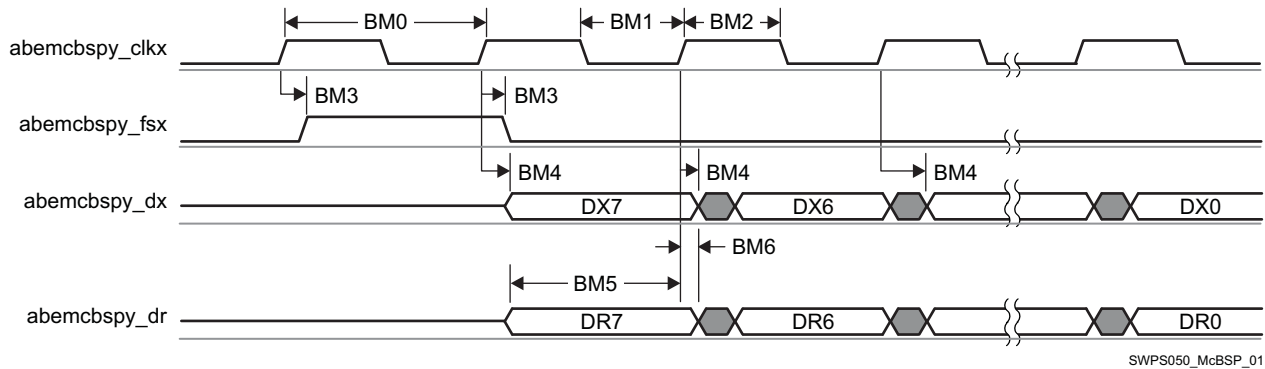
Table 6-22. McBSP1, McBSP2, and McBSP3 Switching Characteristics—I2S/PCM—Master Mode⁽³⁾⁽⁵⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|------------------|---|------------------------|-----------------------|------|
| | | | MIN | MAX | |
| BM0 | $1 / t_{C}(clk)$ | Frequency, output abemcbspy_clkx ⁽⁴⁾ clock | | 12.288 ⁽⁵⁾ | MHz |
| BM1 | $t_{W}(clkL)$ | Typical pulse duration, output abemcbspy_clkx ⁽⁴⁾ low | 0.5 * P ⁽¹⁾ | | ns |
| BM2 | $t_{W}(clkH)$ | Typical pulse duration, output abemcbspy_clkx ⁽⁴⁾ high | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{dc}(clk)$ | Duty cycle error, output abemcbspy_clkx ⁽⁴⁾ | | 4069 | ps |
| | $t_{j}(clk)$ | Jitter standard deviation ⁽²⁾ , output abemcbspy_clkx ⁽⁴⁾ | | 527 | ps |
| | $t_{R}(clk)$ | Rise time, output abemcbspy_clkx ⁽⁴⁾ | 400 | 6500 | ps |
| | $t_{F}(clk)$ | Fall time, output abemcbspy_clkx ⁽⁴⁾ | 400 | 6500 | ps |

Table 6-22. McBSP1, McBSP2, and McBSP3 Switching Characteristics—I2S/PCM—Master Mode⁽³⁾⁽⁵⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------------|---|---------|------|------|
| | | | MIN | MAX | |
| BM3 | $t_{d(\text{clkAE-fsV})}$ | Delay time, output abemcbspy_clkx ⁽⁴⁾ active edge to output abemcbspy_fsx ⁽⁴⁾ valid | 1.1 | 21.8 | ns |
| BM4 | $t_{d(\text{clkxAE-dxV})}$ | Delay time, output ⁽⁴⁾ active edge to output abemcbspy_dx ⁽⁴⁾ valid | 1.1 | 21.8 | ns |
| | $t_{R(\text{fs})}$ | Rise time, output abemcbspy_fsx ⁽⁴⁾ | 400 | 6500 | ps |
| | $t_{F(\text{fs})}$ | Fall time, output abemcbspy_fsx ⁽⁴⁾ | 400 | 6500 | ps |
| | $t_{R(\text{dx})}$ | Rise time, output abemcbspy_dx ⁽⁴⁾ | 400 | 6500 | ps |
| | $t_{F(\text{dx})}$ | Fall time, output abemcbspy_dx ⁽⁴⁾ | 400 | 6500 | ps |

- (1) P = output clk period in ns
- (2) The jitter probability density can be approximated by a Gaussian function.
- (3) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.
- (4) In abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1, 2, or 3.
- (5) See Section 4.3 for CORE OPP voltages.



SWPS050_McBSP_01

Figure 6-32. McBSP1, McBSP2, and McBSP3—I2S/PCM—Master Mode⁽¹⁾⁽²⁾⁽³⁾

- (1) The polarity of McBSP frame synchronization is software configurable.
- (2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.
- (3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1, 2, or 3.

6.6.1.1.2 McBSP1, McBSP2 and McBSP3—I2S/PCM—Slave Mode

Table 6-23. McBSP1, McBSP2, and McBSP3 Timing Requirements—I2S/PCM—Slave Mode⁽³⁾⁽⁴⁾⁽⁶⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------------|---|------------------------|--------|------|
| | | | MIN | MAX | |
| BS0 | $1 / t_{C(\text{clk})}$ | Frequency, input abemcbspy_clkx ⁽⁵⁾ clock | | 12.288 | MHz |
| BS1 | $t_{W(\text{clkL})}$ | Typical pulse duration, output abemcbspy_clkx ⁽⁵⁾ low | 0.5 * P ⁽¹⁾ | | ns |
| BS2 | $t_{W(\text{clkH})}$ | Typical pulse duration, output abemcbspy_clkx ⁽⁵⁾ high | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output abemcbspy_clkx ⁽⁵⁾ | | 4069 | ps |
| | $t_{J(\text{clk})}$ | Jitter standard deviation ⁽²⁾ , output abemcbspy_clkx ⁽⁵⁾ | | 2000 | ps |
| BS3 | $t_{su(\text{fsV-clkAE})}$ | Setup time, abemcbspy_fsx ⁽⁵⁾ valid before abemcbspy_clkx ⁽⁵⁾ active edge | 12.1 | | ns |
| BS4 | $t_{h(\text{clkAE-fsV})}$ | Hold time, abemcbspy_fsx ⁽⁵⁾ valid after abemcbspy_clkx ⁽⁵⁾ active edge | -0.1 | | ns |
| BS6 | $t_{su(\text{drV-clkAE})}$ | Setup time, abemcbspy_dr ⁽⁵⁾ valid before abemcbspy_clkx ⁽⁵⁾ active edge | 12.1 | | ns |
| BS7 | $t_{h(\text{clkAE-drV})}$ | Hold time, abemcbspy_dr ⁽⁵⁾ valid after abemcbspy_clkx ⁽⁵⁾ active edge | -0.1 | | ns |

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(4) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(5) In abemcbspy_dr, abemcbspy_clkx, and abemcbspy_fsx, y is equal to 1, 2, or 3.

(6) See [Section 4.3](#) for CORE OPP voltages.

Table 6-24. McBSP1, McBSP2, and McBSP3 Switching Characteristics—I2S/PCM –Slave Mode⁽¹⁾⁽²⁾⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------------|---|---------|------|------|
| | | | MIN | MAX | |
| BS5 | $t_{d(\text{clkxAE-dxV})}$ | Delay time, input abemcbspy_clkx ⁽²⁾ active edge to output abemcbspy_dx ⁽²⁾ valid | 1.0 | 20.7 | ns |
| | $t_{R(dx)}$ | Rise time, output abemcbspy_dx ⁽²⁾ | 400 | 6500 | ps |
| | $t_{F(dx)}$ | Fall time, output abemcbspy_dx ⁽²⁾ | 400 | 6500 | ps |

- (1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.
- (2) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1, 2, or 3.
- (3) See Section 4.3 for CORE OPP voltages.

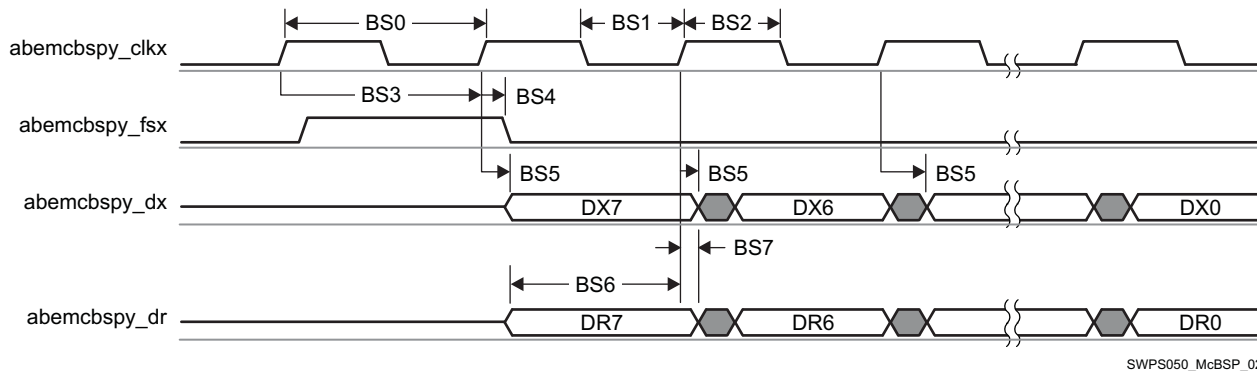


Figure 6-33. McBSP1, McBSP2, and McBSP3—I2S/PCM—Slave Mode⁽¹⁾⁽²⁾⁽³⁾

- (1) The polarity of McBSP frame synchronization is software configurable.
- (2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.
- (3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1, 2, or 3.

6.6.1.2 McBSP2 and McBSP3—I2S/PCM—2 Peripherals—SDR—12.288 MHz—1.8 V

Table 6-25. McBSP2 and McBSP3 Timing Conditions—I2S/PCM

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t _R | Input signal rise time | 400 | 6500 | ps |
| t _F | Input signal fall time | 400 | 6500 | ps |
| Output Condition | | | | |

- (1) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding Device VDDS power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

Table 6-26 through Table 6-29 assume testing over the recommended operating conditions and electrical characteristic conditions below.

6.6.1.2.1 McBSP2 and McBSP3—I2S/PCM—Master Mode

Table 6-26. McBSP2 and McBSP3 Timing Requirements—I2S/PCM—Master Mode⁽¹⁾⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| BM5 | t _{su(drV-clkAE)} | Setup time, abemcbspy_dr ⁽²⁾ valid before abemcbspy_clkx ⁽²⁾ active edge | 10.6 | | ns |
| BM6 | t _{h(clkAE-drV)} | Hold time, abemcbspy_dr ⁽²⁾ valid after abemcbspy_clkx ⁽²⁾ active edge | -0.1 | | ns |

- (1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.
- (2) In abemcbspy_dr and abemcbspy_clkx, y is equal to 2 or 3.
- (3) See Section 4.3 Section for CORE OPP voltages.

Table 6-27. McBSP2 and McBSP3 Switching Characteristics—I2S/PCM—Master Mode⁽³⁾⁽⁵⁾

| NO. | PARAMETER | OPP_NOM | | UNIT |
|-----|----------------------------|---|------|------|
| | | MIN | MAX | |
| BM0 | $1 / t_{C(\text{clk})}$ | Frequency, output abemcbspy_clkx ⁽⁴⁾ clock | | MHz |
| BM1 | $t_{W(\text{clkL})}$ | Typical pulse duration, output abemcbspy_clkx ⁽⁴⁾ low | | ns |
| BM2 | $t_{W(\text{clkH})}$ | Typical pulse duration, output abemcbspy_clkx ⁽⁴⁾ high | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output abemcbspy_clkx ⁽⁴⁾ | | ps |
| | $t_{J(\text{clk})}$ | Jitter standard deviation ⁽²⁾ , output abemcbspy_clkx ⁽⁴⁾ | | ps |
| | $t_{R(\text{clk})}$ | 1000 | 6500 | ps |
| | $t_{F(\text{clk})}$ | 1000 | 6500 | ps |
| BM3 | $t_{d(\text{clkxAE-fsV})}$ | 1.6 | 21.4 | ns |
| BM4 | $t_{d(\text{clkxAE-dxV})}$ | 1.6 | 21.4 | ns |
| | $t_{R(\text{fs})}$ | 1000 | 6500 | ps |
| | $t_{F(\text{fs})}$ | 1000 | 6500 | ps |
| | $t_{R(\text{dx})}$ | 1000 | 6500 | ps |
| | $t_{F(\text{dx})}$ | 1000 | 6500 | ps |

- (1) P = output clk period in ns
- (2) The jitter probability density can be approximated by a Gaussian function.
- (3) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.
- (4) In abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 2 or 3.
- (5) See Section 4.3 for CORE OPP voltages.

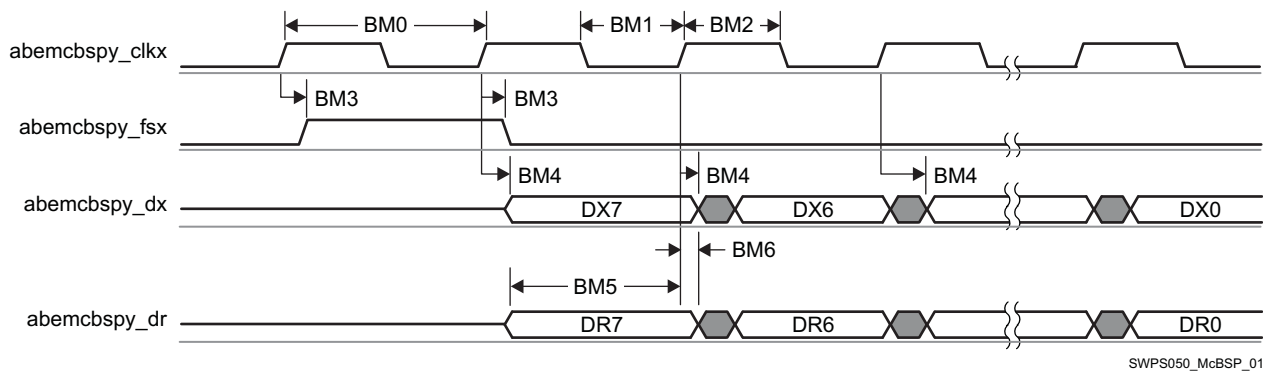


Figure 6-34. McBSP2 and McBSP3—I2S/PCM—Master Mode⁽¹⁾⁽²⁾⁽³⁾

- (1) The polarity of McBSP frame synchronization is software configurable.
- (2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.
- (3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 2 or 3.

6.6.1.2.2 McBSP2 and McBSP3—I2S/PCM—Slave Mode
Table 6-28. McBSP2 and McBSP3 Timing Requirements—I2S/PCM—Slave Mode⁽³⁾⁽⁴⁾⁽⁶⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------------|---|------------------------|--------|------|
| | | | MIN | MAX | |
| BS0 | $1 / t_{C(\text{clk})}$ | Frequency, input abemcbspy_clkx ⁽⁵⁾ clock | | 12.288 | MHz |
| BS1 | $t_{W(\text{clkL})}$ | Typical pulse duration, output abemcbspy_clkx ⁽⁵⁾ low | 0.5 * P ⁽¹⁾ | | ns |
| BS2 | $t_{W(\text{clkH})}$ | Typical pulse duration, output abemcbspy_clkx ⁽⁵⁾ high | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output abemcbspy_clkx ⁽⁵⁾ | | 4069 | ps |
| | $t_{J(\text{clk})}$ | Jitter standard deviation ⁽²⁾ , output abemcbspy_clkx ⁽⁵⁾ | | 2000 | ps |
| BS3 | $t_{su(\text{fsV-clkAE})}$ | Setup time, abemcbspy_fsx ⁽⁵⁾ valid before abemcbspy_clkx ⁽⁵⁾ active edge | 11.8 | | ns |
| BS4 | $t_{h(\text{clkAE-fsV})}$ | Hold time, abemcbspy_fsx ⁽⁵⁾ valid after abemcbspy_clkx ⁽⁵⁾ active edge | -0.5 | | ns |
| BS6 | $t_{su(\text{drV-clkAE})}$ | Setup time, abemcbspy_dr ⁽⁵⁾ valid before abemcbspy_clkx ⁽⁵⁾ active edge | 11.8 | | ns |
| BS7 | $t_{h(\text{clkAE-drV})}$ | Hold time, abemcbspy_dr ⁽⁵⁾ valid after abemcbspy_clkx ⁽⁵⁾ active edge | -0.5 | | ns |

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(4) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(5) In abemcbspy_dr, abemcbspy_clkx, and abemcbspy_fsx, y is equal to 2 or 3.

(6) See [Section 4.3](#) for CORE OPP voltages.

Table 6-29. McBSP2 and McBSP3 Switching Characteristics—I2S/PCM –Slave Mode⁽¹⁾⁽²⁾ (3)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------------|---|---------|------|------|
| | | | MIN | MAX | |
| BS5 | $t_{d(\text{clkxAE-dxV})}$ | Delay time, input abemcbspy_clkx ⁽²⁾ active edge to output abemcbspy_dx ⁽²⁾ valid | 1.1 | 18.9 | ns |
| | $t_{R(\text{dx})}$ | Rise time, output abemcbspy_dx ⁽²⁾ | 400 | 6500 | ps |
| | $t_{F(\text{dx})}$ | Fall time, output abemcbspy_dx ⁽²⁾ | 400 | 6500 | ps |

- (1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.
- (2) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 2 or 3.
- (3) See [Section 4.3](#) for CORE OPP voltages.

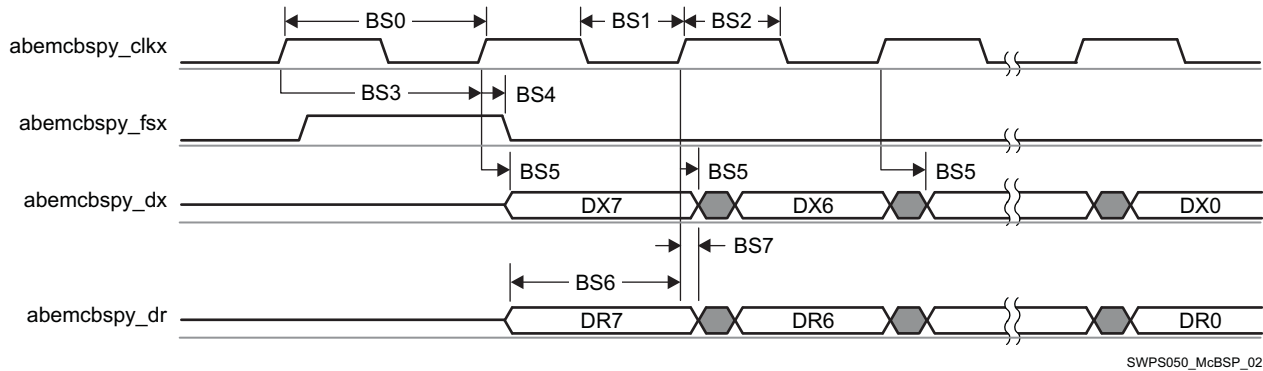


Figure 6-35. McBSP2 and McBSP3—I2S/PCM—Slave Mode⁽¹⁾⁽²⁾⁽³⁾

- (1) The polarity of McBSP frame synchronization is software configurable.
- (2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.
- (3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 2 or 3.

6.6.1.3 McBSP1—TDM—5 Peripherals—SDR—6.144 MHz—1.8 V

Table 6-30. McBSP1 Timing Conditions—TDM

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|-------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 1000 | 17700 | ps |
| t_F | Input signal fall time | 1000 | 17700 | ps |
| Output Condition | | | | |

- (1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

6.6.1.3.1 McBSP1—TDM—Master Mode

[Table 6-31](#) through [Table 6-34](#) assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 6-31. McBSP1 Timing Requirements—TDM—Master Mode⁽¹⁾⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|---------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| BM5 | $t_{su}(drV-clkAE)$ | Setup time, abemcbspy_dr ⁽²⁾ valid before abemcbspy_clkx ⁽²⁾ active edge | 19.5 | | ns |
| BM6 | $t_{h}(clkAE-drV)$ | Hold time, abemcbspy_dr ⁽²⁾ valid after abemcbspy_clkx ⁽²⁾ active edge | -1.1 | | ns |

- (1) The timings apply to all configurations regardless of abemcbpsy_clkx polarity and which clock edges are used to drive output data and capture input data.
- (2) In abemcbpsy_dr and abemcbpsy_clkx, y is equal to 1.
- (3) See Section 4.3 for CORE OPP voltages.

Table 6-32. McBSP1 Switching Characteristics—TDM –Master Mode⁽³⁾⁽⁵⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------------|---|-----------------|----------------------|------|
| | | | MIN | MAX | |
| BM0 | $1 / t_{C(\text{clk})}$ | Frequency, output abemcbpsy_clkx ⁽⁴⁾ clock | | 6.144 ⁽⁵⁾ | MHz |
| BM1 | $t_{W(\text{clkL})}$ | Typical pulse duration, output abemcbpsy_clkx ⁽⁴⁾ low | $0.5 * P^{(1)}$ | | ns |
| BM2 | $t_{W(\text{clkH})}$ | Typical pulse duration, output abemcbpsy_clkx ⁽⁴⁾ high | $0.5 * P^{(1)}$ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output abemcbpsy_clkx ⁽⁴⁾ | | 8138 | ps |
| | $t_{J(\text{clk})}$ | Jitter standard deviation ⁽²⁾ , output abemcbpsy_clkx ⁽⁴⁾ | | 65 | ps |
| | $t_{R(\text{clk})}$ | Rise time, output abemcbpsy_clkx ⁽⁴⁾ | 1000 | 17700 | ps |
| | $t_{F(\text{clk})}$ | Fall time, output abemcbpsy_clkx ⁽⁴⁾ | 1000 | 17700 | ps |
| BM3 | $t_{d(\text{clkAE-fsV})}$ | Delay time, output abemcbpsy_clkx ⁽⁴⁾ active edge to output abemcbpsy_fsx ⁽⁴⁾ valid | 2.1 | 45.7 | ns |
| BM4 | $t_{d(\text{clkxAE-dxV})}$ | Delay time, output ⁽⁴⁾ active edge to output abemcbpsy_dx ⁽⁴⁾ valid | 2.1 | 45.7 | ns |
| | $t_{R(\text{fs})}$ | Rise time, output abemcbpsy_fsx ⁽⁴⁾ | 1000 | 17700 | ps |
| | $t_{F(\text{fs})}$ | Fall time, output abemcbpsy_fsx ⁽⁴⁾ | 1000 | 17700 | ps |
| | $t_{R(\text{dx})}$ | Rise time, output abemcbpsy_dx ⁽⁴⁾ | 1000 | 17700 | ps |
| | $t_{F(\text{dx})}$ | Fall time, output abemcbpsy_dx ⁽⁴⁾ | 1000 | 17700 | ps |

- (1) P = output clk period in ns
- (2) The jitter probability density can be approximated by a Gaussian function.
- (3) The timings apply to all configurations regardless of abemcbpsy_clkx polarity and which clock edges are used to drive output data and capture input data.
- (4) In abemcbpsy_clkx, abemcbpsy_fsx, and abemcbpsy_dx, y is equal to 1.
- (5) See Section 4.3 for CORE OPP voltages.

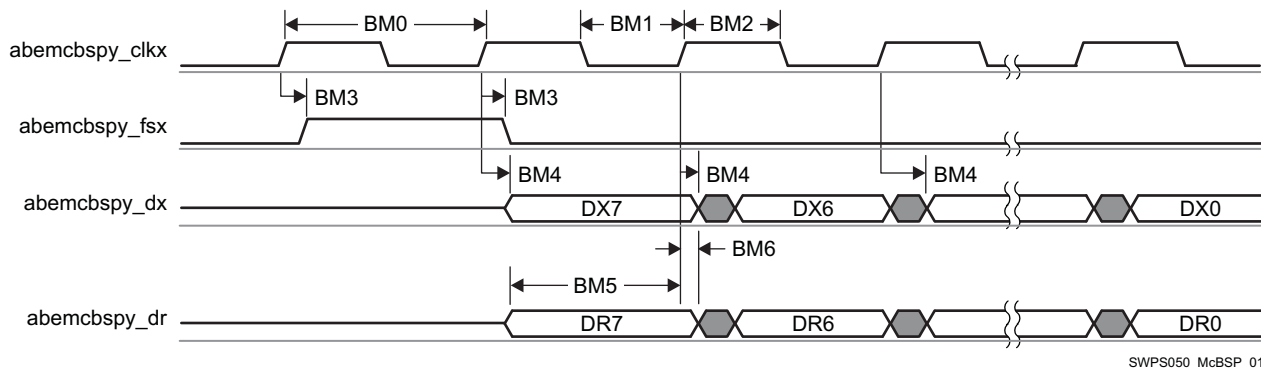


Figure 6-36. McBSP1—TDM—Master Mode⁽¹⁾⁽²⁾⁽³⁾

- (1) The polarity of McBSP frame synchronization is software configurable.
- (2) The active clock edge selection of abemcbpsy_clkx (rising or falling) on which abemcbpsy_dx data is latched and abemcbpsy_dr data is sampled is software configurable.
- (3) In abemcbpsy_dr, abemcbpsy_clkx, abemcbpsy_fsx, and abemcbpsy_dx, y is equal to 1.

6.6.1.3.2 McBSP1—TDM—Slave Mode

Table 6-33. McBSP1 Timing Requirements—TDM—Slave Mode⁽³⁾⁽⁴⁾⁽⁶⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|-------------------------|--|---------|-------|------|
| | | | MIN | MAX | |
| BS0 | $1 / t_{C(\text{clk})}$ | Frequency, input abemcbpsy_clkx ⁽⁵⁾ clock | | 6.144 | MHz |

Table 6-33. McBSP1 Timing Requirements—TDM—Slave Mode⁽³⁾⁽⁴⁾⁽⁶⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------------|---|------------------------|------|------|
| | | | MIN | MAX | |
| BS1 | $t_{W(\text{clkL})}$ | Typical pulse duration, output abemcbspy_clkx ⁽⁵⁾ low | 0.5 * P ⁽¹⁾ | | |
| BS2 | $t_{W(\text{clkH})}$ | Typical pulse duration, output abemcbspy_clkx ⁽⁵⁾ high | 0.5 * P ⁽¹⁾ | | |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output abemcbspy_clkx ⁽⁵⁾ | | 8138 | ps |
| | $t_{J(\text{clk})}$ | Jitter standard deviation ⁽²⁾ , output abemcbspy_clkx ⁽⁵⁾ | | 2000 | ps |
| BS3 | $t_{su(\text{fsV-clkAE})}$ | Setup time, abemcbspy_fsx ⁽⁵⁾ valid before abemcbspy_clkx ⁽⁵⁾ active edge | 25.7 | | ns |
| BS4 | $t_{h(\text{clkAE-fsV})}$ | Hold time, abemcbspy_fsx ⁽⁵⁾ valid after abemcbspy_clkx ⁽⁵⁾ active edge | -0.8 | | ns |
| BS6 | $t_{su(\text{drV-clkAE})}$ | Setup time, abemcbspy_dr ⁽⁵⁾ valid before abemcbspy_clkx ⁽⁵⁾ active edge | 25.7 | | ns |
| BS7 | $t_{h(\text{clkAE-drV})}$ | Hold time, abemcbspy_dr ⁽⁵⁾ valid after abemcbspy_clkx ⁽⁵⁾ active edge | -0.8 | | ns |

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(4) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(5) In abemcbspy_dr, abemcbspy_clkx, and abemcbspy_fsx, y is equal to 1.

(6) See Section 4.3 for CORE OPP voltages.

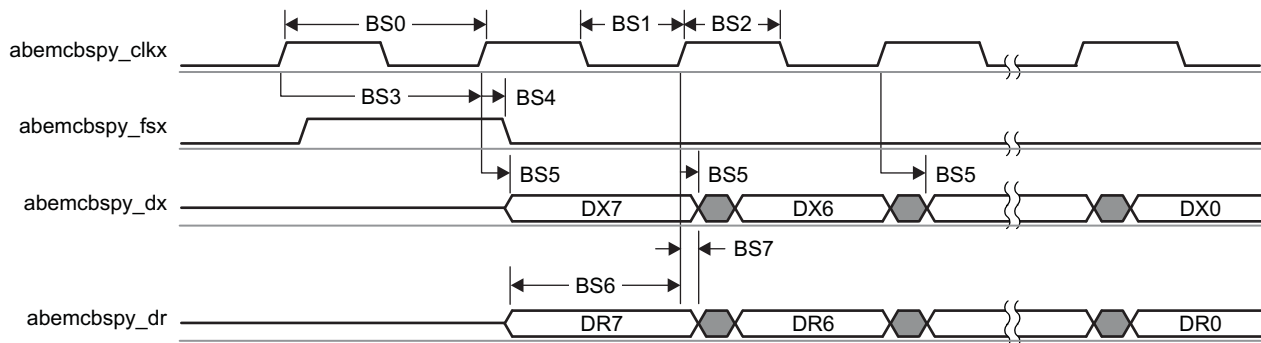
Table 6-34. McBSP1 Switching Characteristics—TDM—Slave Mode⁽¹⁾⁽²⁾⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------------|---|---------|-------|------|
| | | | MIN | MAX | |
| BS5 | $t_{d(\text{clkxAE-dxV})}$ | Delay time, input abemcbspy_clkx ⁽²⁾ active edge to output abemcbspy_dx ⁽²⁾ valid | 5.2 | 24.4 | ns |
| | $t_{R(\text{dx})}$ | Rise time, output abemcbspy_dx ⁽²⁾ | 1000 | 17700 | ps |
| | $t_{F(\text{dx})}$ | Fall time, output abemcbspy_dx ⁽²⁾ | 1000 | 17700 | ps |

(1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(2) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1.

(3) See Section 4.3 for CORE OPP voltages.



SWPS050_McBSP_02

Figure 6-37. McBSP1—TDM—Slave Mode⁽¹⁾⁽²⁾⁽³⁾

(1) The polarity of McBSP frame synchronization is software configurable.

(2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.

(3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1.

6.6.1.4 McBSP2 and McBSP3—TDM—1 Peripheral —SDR—12.288 MHz—1.8 V
Table 6-35. McBSP2 and McBSP3 Timing Conditions—TDM

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 600 | 6500 | ps |
| t_F | Input signal fall time | 600 | 6500 | ps |
| Output Condition | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding Device VDDS power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-36](#) through [Table 6-39](#) assume testing over the recommended operating conditions and electrical characteristic conditions below.

6.6.1.4.1 McBSP2 and McBSP3—TDM—Master Mode
Table 6-36. McBSP2 and McBSP3 Timing Requirements—TDM—Master Mode⁽¹⁾⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|---------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| BM5 | $t_{su(drV-clkAE)}$ | Setup time, abemcbpsy_dr ⁽²⁾ valid before abemcbpsy_clkx ⁽²⁾ active edge | 8.6 | | ns |
| BM6 | $t_h(clkAE-drV)$ | Hold time, abemcbpsy_dr ⁽²⁾ valid after abemcbpsy_clkx ⁽²⁾ active edge | 0.8 | | ns |

(1) The timings apply to all configurations regardless of abemcbpsy_clkx polarity and which clock edges are used to drive output data and capture input data.

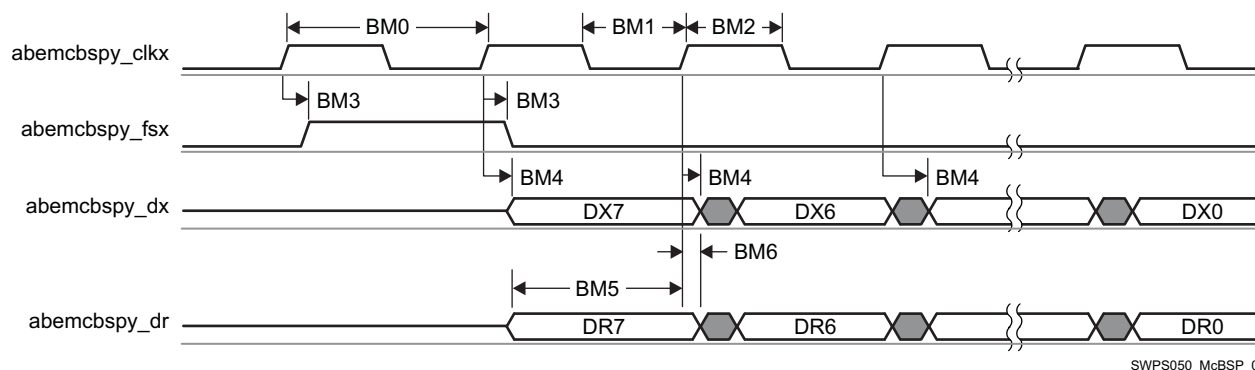
(2) In abemcbpsy_dr and abemcbpsy_clkx, y is equal to 2 or 3.

(3) See [Section 4.3](#) for CORE OPP voltages.

Table 6-37. McBSP2 and McBSP3 Switching Characteristics—TDM—Master Mode⁽³⁾⁽⁵⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|---------------------|---|------------------------|-----------------------|------|
| | | | MIN | MAX | |
| BM0 | $1 / t_{C(clk)}$ | Frequency, output abemcbpsy_clkx ⁽⁴⁾ clock | | 12.288 ⁽⁵⁾ | MHz |
| BM1 | $t_{W(clkL)}$ | Typical pulse duration, output abemcbpsy_clkx ⁽⁴⁾ low | 0.5 * P ⁽¹⁾ | | ns |
| BM2 | $t_{W(clkH)}$ | Typical pulse duration, output abemcbpsy_clkx ⁽⁴⁾ high | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output abemcbpsy_clkx ⁽⁴⁾ | | 4069 | ps |
| | $t_{j(clk)}$ | Jitter standard deviation ⁽²⁾ , output abemcbpsy_clkx ⁽⁴⁾ | | 658 | ps |
| | $t_{R(clk)}$ | Rise time, output abemcbpsy_clkx ⁽⁴⁾ | 600 | 6500 | ps |
| | $t_{F(clk)}$ | Fall time, output abemcbpsy_clkx ⁽⁴⁾ | 600 | 6500 | ps |
| BM3 | $t_{d(clkAE-fsV)}$ | Delay time, output abemcbpsy_clkx ⁽⁴⁾ active edge to output abemcbpsy_fsx ⁽⁴⁾ valid | 1.3 | 19.9 | ns |
| BM4 | $t_{d(clkxAE-dxV)}$ | Delay time, output ⁽⁴⁾ active edge to output abemcbpsy_dx ⁽⁴⁾ valid | 1.3 | 19.9 | ns |
| | $t_{R(fs)}$ | Rise time, output abemcbpsy_fsx ⁽⁴⁾ | 600 | 6500 | ps |
| | $t_{F(fs)}$ | Fall time, output abemcbpsy_fsx ⁽⁴⁾ | 600 | 6500 | ps |
| | $t_{R(dx)}$ | Rise time, output abemcbpsy_dx ⁽⁴⁾ | 600 | 6500 | ps |
| | $t_{F(dx)}$ | Fall time, output abemcbpsy_dx ⁽⁴⁾ | 600 | 6500 | ps |

- (1) P = output clk period in ns
- (2) The jitter probability density can be approximated by a Gaussian function.
- (3) The timings apply to all configurations regardless of abemcbpsy_clkx polarity and which clock edges are used to drive output data and capture input data.
- (4) In abemcbpsy_clkx, abemcbpsy_fsx, and abemcbpsy_dx, y is equal to 2 or 3.
- (5) See Section 4.3 for CORE OPP voltages.



SWPS050_McBSP_01

Figure 6-38. McBSP2 and McBSP3—TDM—Master Mode⁽¹⁾⁽²⁾⁽³⁾

- (1) The polarity of McBSP frame synchronization is software configurable.
- (2) The active clock edge selection of abemcbpsy_clkx (rising or falling) on which abemcbpsy_dx data is latched and abemcbpsy_dr data is sampled is software configurable.
- (3) In abemcbpsy_dr, abemcbpsy_clkx, abemcbpsy_fsx, and abemcbpsy_dx, y is equal to 2 or 3.

6.6.1.4.2 McBSP2 and McBSP3—TDM—Slave Mode

Table 6-38. McBSP2 and McBSP3 Timing Requirements—TDM—Slave Mode⁽³⁾⁽⁴⁾⁽⁶⁾

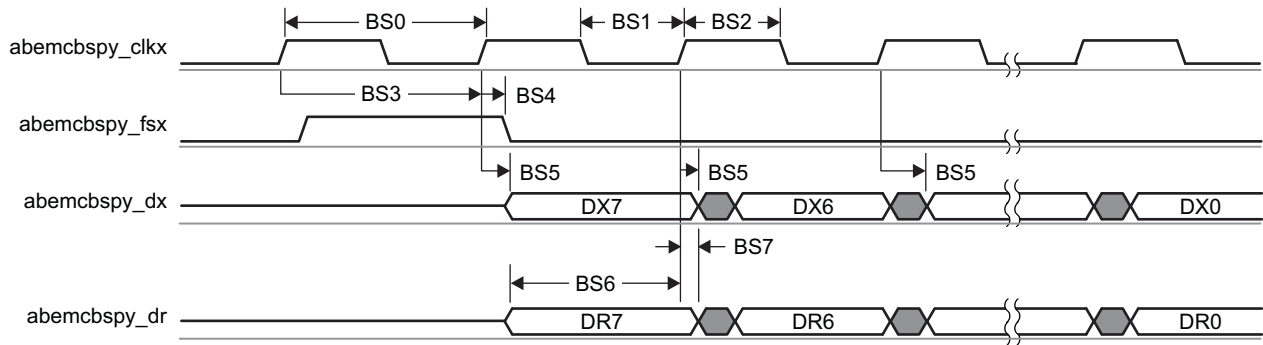
| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------------|---|-----------------|--------|------|
| | | | MIN | MAX | |
| BS0 | $1 / t_{C(\text{clk})}$ | Frequency, input abemcbpsy_clkx ⁽⁵⁾ clock | | 12.288 | MHz |
| BS1 | $t_{W(\text{clkL})}$ | Typical pulse duration, output abemcbpsy_clkx ⁽⁵⁾ low | $0.5 * P^{(1)}$ | | ns |
| BS2 | $t_{W(\text{clkH})}$ | Typical pulse duration, output abemcbpsy_clkx ⁽⁵⁾ high | $0.5 * P^{(1)}$ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output abemcbpsy_clkx ⁽⁵⁾ | | 4069 | ps |
| | $t_{j(\text{clk})}$ | Jitter standard deviation ⁽²⁾ , output abemcbpsy_clkx ⁽⁵⁾ | | 2000 | ps |
| BS3 | $t_{su(\text{fsV-clkAE})}$ | Setup time, abemcbpsy_fsx ⁽⁵⁾ valid before abemcbpsy_clkx ⁽⁵⁾ active edge | 12.0 | | ns |
| BS4 | $t_{h(\text{clkAE-fsV})}$ | Hold time, abemcbpsy_fsx ⁽⁵⁾ valid after abemcbpsy_clkx ⁽⁵⁾ active edge | 0.1 | | ns |
| BS6 | $t_{su(\text{drV-clkAE})}$ | Setup time, abemcbpsy_dr ⁽⁵⁾ valid before abemcbpsy_clkx ⁽⁵⁾ active edge | 12.0 | | ns |
| BS7 | $t_{h(\text{clkAE-drV})}$ | Hold time, abemcbpsy_dr ⁽⁵⁾ valid after abemcbpsy_clkx ⁽⁵⁾ active edge | 0.7 | | ns |

- (1) P = output clk period in ns
- (2) The jitter probability density can be approximated by a Gaussian function.
- (3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
- (4) The timings apply to all configurations regardless of abemcbpsy_clkx polarity and which clock edges are used to drive output data and capture input data.
- (5) In abemcbpsy_dr, abemcbpsy_clkx, and abemcbpsy_fsx, y is equal to 2 or 3.
- (6) See Section 4.3 for CORE OPP voltages.

Table 6-39. McBSP2 and McBSP3 Switching Characteristics—TDM—Slave Mode⁽¹⁾⁽²⁾⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------------|---|---------|------|------|
| | | | MIN | MAX | |
| BS5 | $t_{d(\text{clkxAE-dxV})}$ | Delay time, input abemcbpsy_clkx ⁽²⁾ active edge to output abemcbpsy_dx ⁽²⁾ valid | 1.3 | 16.8 | ns |
| | $t_{R(dx)}$ | Rise time, output abemcbpsy_dx ⁽²⁾ | 600 | 6500 | ps |
| | $t_{F(dx)}$ | Fall time, output abemcbpsy_dx ⁽²⁾ | 600 | 6500 | ps |

- (1) The timings apply to all configurations regardless of abemcbpsy_clkx polarity and which clock edges are used to drive output data and capture input data.
- (2) In abemcbpsy_dr, abemcbpsy_clkx, abemcbpsy_fsx, and abemcbpsy_dx, y is equal to 2 or 3.
- (3) See Section 4.3 for CORE OPP voltages.



SWPS050_McBSP_02

Figure 6-39. McBSP2 and McBSP3—TDM—Slave Mode⁽¹⁾⁽²⁾⁽³⁾

- (1) The polarity of McBSP frame synchronization is software configurable.
- (2) The active clock edge selection of abemcbpsy_clkx (rising or falling) on which abemcbpsy_dx data is latched and abemcbpsy_dr data is sampled is software configurable.
- (3) In abemcbpsy_dr, abemcbpsy_clkx, abemcbpsy_fsx, and abemcbpsy_dx, y is equal to 2 or 3.

6.6.1.5 McBSP1 and McBSP3—TDM—1 Peripheral —SDR—24.576 MHz—1.8 V

Table 6-40. McBSP1 and McBSP3 Timing Conditions—TDM

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 400 | 6500 | ps |
| t_F | Input signal fall time | 400 | 6500 | ps |
| Output Condition | | | | |

- (1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

Table 6-41 and Table 6-42 assume testing over the recommended operating conditions and electrical characteristic conditions below.

6.6.1.5.1 McBSP1—TDM—Slave Mode

Table 6-41. McBSP1 and McBSP3 Timing Requirements—TDM—Slave Mode⁽³⁾⁽⁴⁾⁽⁶⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|-------------------------|---|-----------------|--------|------|
| | | | MIN | MAX | |
| BS0 | $1 / t_{C(\text{clk})}$ | Frequency, input abemcbpsy_clkx ⁽⁵⁾ clock | | 24.576 | MHz |
| BS1 | $t_{W(\text{clkL})}$ | Typical pulse duration, output abemcbpsy_clkx ⁽⁵⁾ low | $0.5 * P^{(1)}$ | | ns |
| BS2 | $t_{W(\text{clkH})}$ | Typical pulse duration, output abemcbpsy_clkx ⁽⁵⁾ high | $0.5 * P^{(1)}$ | | ns |

Table 6-41. McBSP1 and McBSP3 Timing Requirements—TDM—Slave Mode⁽³⁾⁽⁴⁾⁽⁶⁾ (continued)

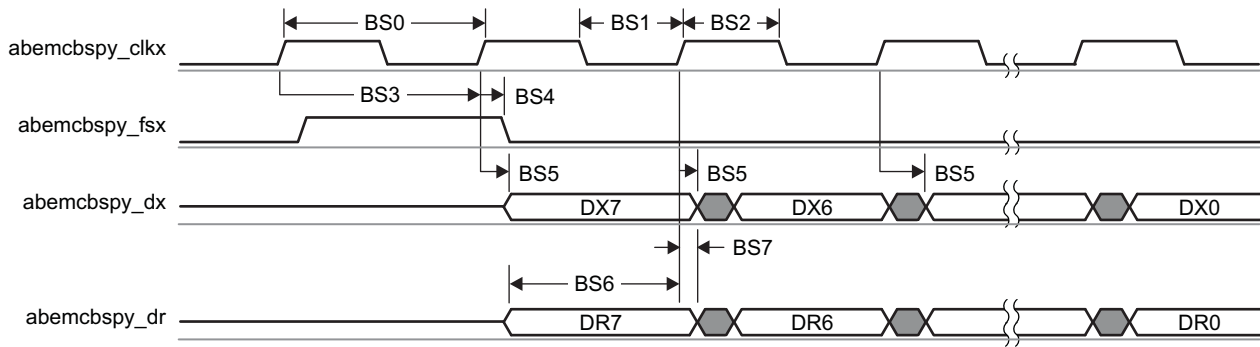
| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|---------------------|---|---------|------|------|
| | | | MIN | MAX | |
| | $t_{dc}(clk)$ | Duty cycle error, output abemcbspy_clkx ⁽⁵⁾ | | 4069 | ps |
| | $t_{j}(clk)$ | Jitter standard deviation ⁽²⁾ , output abemcbspy_clkx ⁽⁵⁾ | | 2000 | ps |
| BS3 | $t_{su}(fsV-clkAE)$ | Setup time, abemcbspy_fsx ⁽⁵⁾ valid before abemcbspy_clkx ⁽⁵⁾ active edge | 12 | | ns |
| BS4 | $t_{h}(clkAE-fsV)$ | Hold time, abemcbspy_fsx ⁽⁵⁾ valid after abemcbspy_clkx ⁽⁵⁾ active edge | 0.1 | | ns |
| BS6 | $t_{su}(drV-clkAE)$ | Setup time, abemcbspy_dr ⁽⁵⁾ valid before abemcbspy_clkx ⁽⁵⁾ active edge | 12 | | ns |
| BS7 | $t_{h}(clkAE-drV)$ | Hold time, abemcbspy_dr ⁽⁵⁾ valid after abemcbspy_clkx ⁽⁵⁾ active edge | 0.1 | | ns |

- (1) P = output clk period in ns
- (2) The jitter probability density can be approximated by a Gaussian function.
- (3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
- (4) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.
- (5) In abemcbspy_dr, abemcbspy_clkx, and abemcbspy_fsx, y is equal to 1.
- (6) See *Operating Performance Points* for CORE OPP voltages.

Table 6-42. McBSP1 and McBSP3 Switching Characteristics—TDM—Slave Mode⁽¹⁾⁽²⁾⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|---------------------|---|---------|------|------|
| | | | MIN | MAX | |
| BS5 | $t_{d}(clkxAE-dxV)$ | Delay time, input abemcbspy_clkx ⁽²⁾ active edge to output abemcbspy_dx ⁽²⁾ valid | 1.3 | 16.8 | ns |
| | $t_{R}(dx)$ | Rise time, output abemcbspy_dx ⁽²⁾ | 600 | 6500 | ps |
| | $t_{F}(dx)$ | Fall time, output abemcbspy_dx ⁽²⁾ | 600 | 6500 | ps |

- (1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.
- (2) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1 or 3.
- (3) See *Operating Performance Points* for CORE OPP voltages.



SWPS050_McBSP_02

Figure 6-40. McBSP1 and McBSP3 —TDM—Slave Mode⁽¹⁾⁽²⁾⁽³⁾

- (1) The polarity of McBSP frame synchronization is software configurable.
- (2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.
- (3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1 or 3.

6.6.2 Multichannel Audio Serial Port (McASP), 1.8 V

NOTE

For more information, see the Serial Communication Interface section of the Device TRM.

6.6.2.1 McASP – I2S - 1 Peripheral – SDR – 12.288 MHz – 1.8 V

Table 6-43. McASP Timing Conditions – I2S

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 1000 | 5000 | ps |
| t_F | Input signal fall time | 1000 | 5000 | ps |
| Output Condition | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

6.6.2.1.1 McASP—I2S—Slave Mode

[Table 6-44](#) assumes testing over the recommended operating conditions and electrical characteristic conditions below.

Table 6-44. McASP Timing Requirements – I2S– Slave Mode ⁽³⁾⁽⁴⁾⁽⁷⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------------|---|------------------------|--------|------|
| | | | MIN | MAX | |
| BS0 | $1 / t_{C(\text{clk})}$ | Frequency, input abemcasp_aclk ⁽⁵⁾ clock | | 12.288 | MHz |
| BS1 | $t_{W(\text{clkL})}$ | Typical Pulse duration, abemcasp_aclk ⁽⁵⁾ low | 0.5 * P ⁽¹⁾ | | |
| BS2 | $t_{W(\text{clkH})}$ | Typical Pulse duration, abemcasp_aclk ⁽⁵⁾ high | 0.5 * P ⁽¹⁾ | | |
| | $t_{dc(\text{clk})}$ | Duty cycle error, abemcasp_aclk ⁽⁵⁾ | | 8138 | ps |
| | $t_{J(\text{clk})}$ | Cycle jitter ⁽²⁾ , abemcasp_aclk ⁽⁵⁾ | | 2000 | ps |
| BS3 | $t_{su(\text{fsV-clkAE})}$ | Setup time, abemcasp_afs ⁽⁶⁾ valid before abemcasp_aclk ⁽⁵⁾ active edge | 14.3 | | ns |
| BS4 | $t_{h(\text{clkAE-fsV})}$ | Hold time, abemcasp_afs ⁽⁶⁾ valid after abemcasp_aclk ⁽⁵⁾ active edge | -0.3 | | ns |
| BS6 | $t_{su(\text{drV-clkAE})}$ | Setup time, abemcasp_axr valid before abemcasp_aclk ⁽⁵⁾ active edge | 14.3 | | ns |
| BS7 | $t_{h(\text{clkAE-drV})}$ | Hold time, abemcasp_axr valid after abemcasp_aclk ⁽⁵⁾ active edge | -0.3 | | ns |

(1) P = abemcasp_aclkx / abemcasp_aclkr period in ns

(2) Maximum cycle jitter supported by abemcasp_aclkx / abemcasp_aclkr input clock

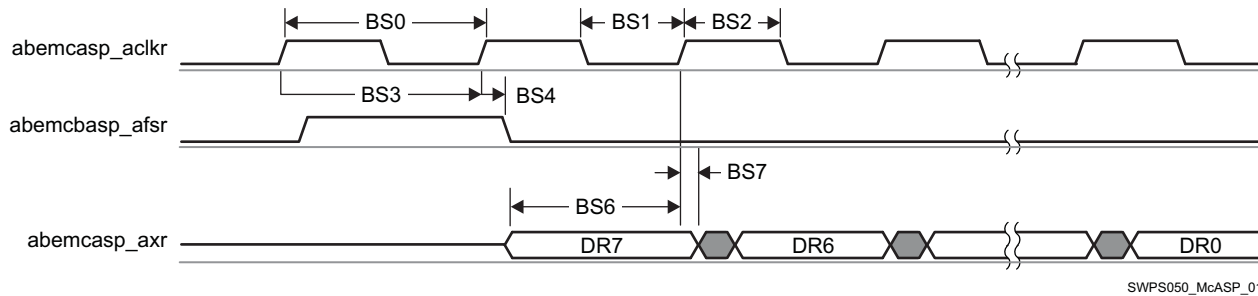
(3) The timing requirements are guaranteed till the cycle jitter and duty cycle error conditions specified.

(4) The timings apply to all configurations regardless of abemcasp_aclk polarity and which clock edges are used to drive output data and capture input data.

(5) abemcasp_aclk corresponds to either abemcasp_aclkx or abemcasp_aclkr; abemcasp_aclkr is available in 6-pins mode only

(6) abemcasp_afs corresponds to either abemcasp_afsx or abemcasp_afsr; abemcasp_afsr is available in 6-pins mode only

(7) See [Section 4.3](#) for CORE OPP voltages.



SWPS050_McASP_01

Figure 6-41. McASP – I2S – Slave Mode

6.6.3 Multichannel Serial Port Interface (McSPI), 1.8 V

NOTE

For more information, see the Serial Communication Interface section of the Device TRM.

McSPI allows a duplex, synchronous, serial communication between a local host and SPI compliant external devices.

6.6.3.1 McSPI1, McSPI2 and McSPI4 – 1 Peripheral – SDR – Master – 48 MHz

Table 6-45. McSPI1, McSPI2 and McSPI4 Timing Conditions – Master Mode – 48 MHz

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 100 | 4000 | ps |
| t_F | Input signal fall time | 100 | 4000 | ps |
| Output Condition | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

Table 6-46 and Table 6-47 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 6-46. McSPI1, McSPI2 and McSPI4 Timing Requirements – Master Mode – 48 MHz ⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| SM4 | $t_{su}(SOMI-CLKAE)$ | Setup time, mcspix_somi ⁽²⁾ valid before mcspix_clk ⁽¹⁾⁽²⁾ active edge | 4.59 | | ns |
| SM5 | $t_h(CLKAE-SOMI)$ | Hold time, mcspix_somi ⁽²⁾ valid after mcspix_clk ⁽¹⁾⁽²⁾ active edge | 3.43 | | ns |

(1) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(2) In mcspix_clk and mcspix_somi, x is equal to 1, 2 or 4.

(3) See Section 4.3 for CORE OPP voltages.

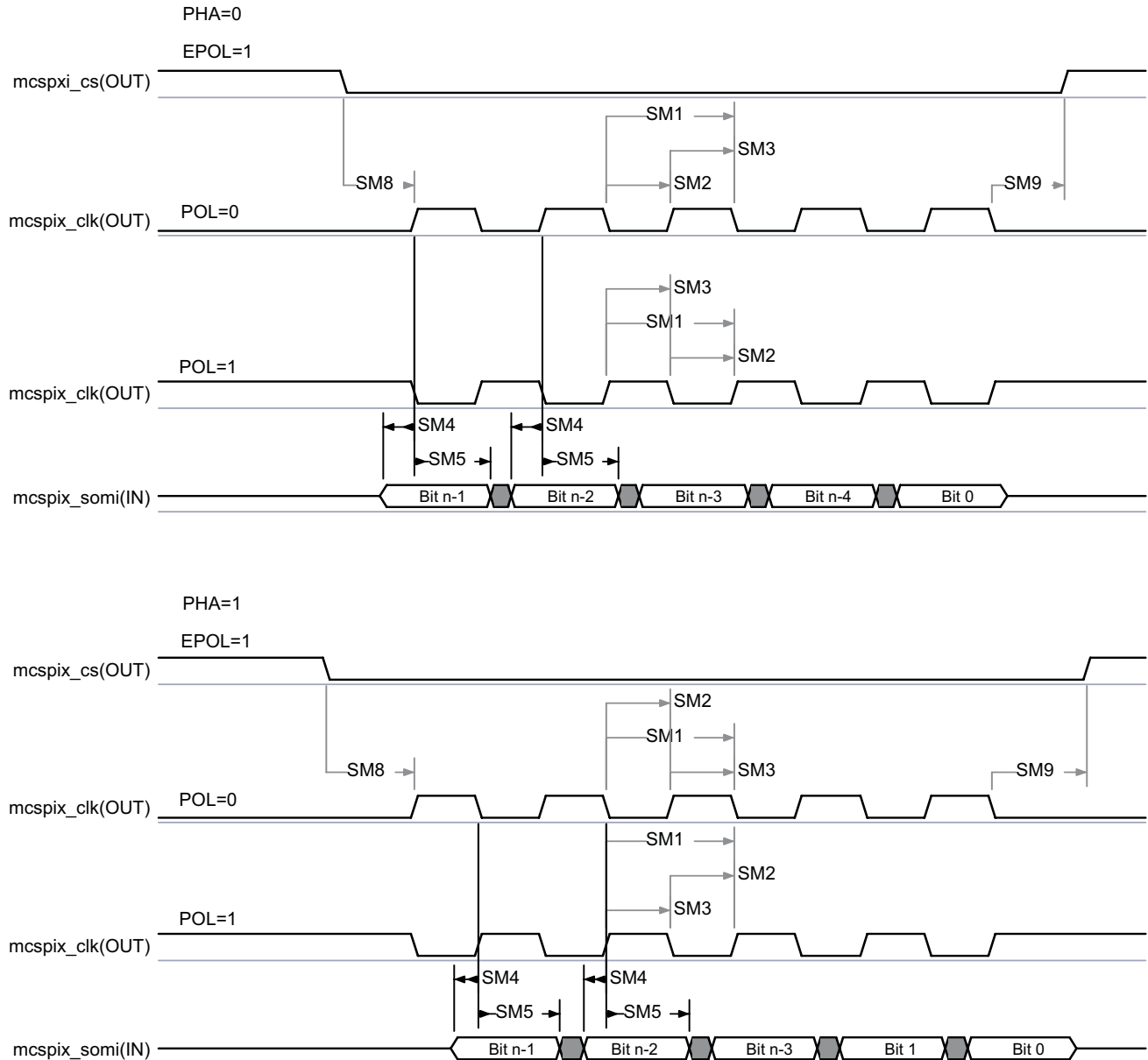
Table 6-47. McSPI1, McSPI2 and McSPI4 Switching Requirements – Master Mode – 48 MHz ⁽¹⁰⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------|---|---------------------|-----|------|
| | | | MIN | MAX | |
| SM1 | $1 / t_C(CLK)$ | Frequency ⁽²⁾ , mcspix_clk ⁽¹⁾⁽⁸⁾ | | 48 | MHz |
| SM2 | $t_W(CLKL)$ | Typical Pulse duration, mcspix_clk ⁽⁴⁾⁽⁸⁾ low | $0.5 \cdot P^{(2)}$ | | ns |
| SM3 | $t_W(CLKH)$ | Typical Pulse duration, mcspix_clk ⁽⁴⁾⁽⁸⁾ high | $0.5 \cdot P^{(2)}$ | | ns |

Table 6-47. McSPI1, McSPI2 and McSPI4 Switching Requirements – Master Mode – 48 MHz ⁽¹⁰⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|-------------------|---|----------------------|----------------------------|------|
| | | | MIN | MAX | |
| | $t_{dc}(clk)$ | Duty cycle error, mcspix_clk ⁽⁸⁾ | | 1042 | ps |
| | $t_{j}(clk)$ | Jitter standard deviation ⁽³⁾ , mcspix_clk ⁽⁸⁾ | | 65 | ps |
| | $t_{R}(clk)$ | Rise time, mcspix_clk ⁽⁸⁾ | | 1928.3 | ps |
| | $t_{F}(clk)$ | Fall time, mcspix_clk ⁽⁸⁾ | | 1877.1 | ps |
| SM6 | $t_{d}(CLK-SIMO)$ | Delay time, mcspix_clk ⁽⁴⁾⁽⁸⁾ active edge to mcspix_simo ⁽⁸⁾ transition | -2.43 | 3.63 | ns |
| SM7 | $t_{d9CS-SIMO}$ | Delay time, mcspix_cs ⁽⁹⁾ active edge to mcspix_simo ⁽⁸⁾ transition | PHA=0 ⁽⁷⁾ | 3.63 | ns |
| SM8 | $t_{d}(CS-CLK)$ | Delay time, mcspix_cs ⁽⁹⁾ active to mcspix_clk ⁽⁴⁾ first edge | PHA=1 ⁽⁷⁾ | A ⁽⁵⁾ - 3.63 | ns |
| | | | PHA=0 ⁽⁷⁾ | B ⁽⁶⁾ - 3.63 | ns |
| SM9 | $t_{d}(CLK-CS)$ | Delay time, mcspix_clk ⁽⁴⁾⁽⁸⁾ last edge to mcspix_cs ⁽⁹⁾ inactive | PHA=1 ⁽⁷⁾ | B ⁽⁶⁾ - 2.43 | ns |
| | | | PHA=0 ⁽⁷⁾ | A ⁽⁵⁾ - 2.43 | ns |
| | $t_{R}(SIMO)$ | Rise time, mcspix_simo ⁽⁸⁾ | | 1928.3 | ps |
| | $t_{F}(SIMO)$ | Fall time, mcspix_simo ⁽⁸⁾ | | 1877.1 | ps |
| | $t_{R}(CS)$ | Rise time, mcspix_cs ⁽⁹⁾ | | 1928.3 | ps |
| | $t_{F}(CS)$ | Fall time, mcspix_cs ⁽⁹⁾⁽⁹⁾ | | 1877.1 | ps |

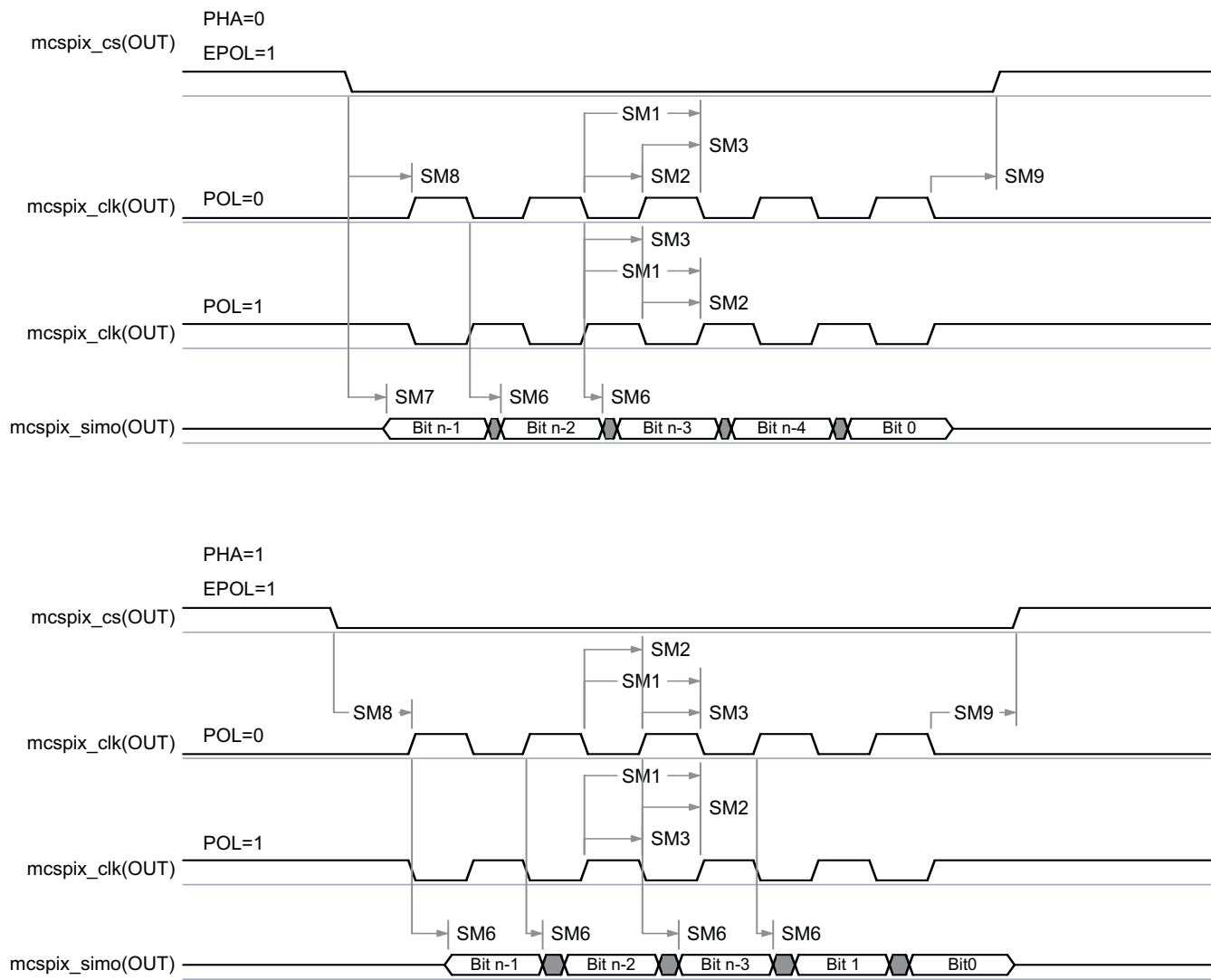
- (1) Related with the mcspix_clk maximum frequency programmable in the MCSPI module by setting the configuration register MCSPI_CHxCONF. For more information, see the McSPI environment chapter, Data Format Configurations section of the Device TRM for modes and phase correspondence description.
- (2) P = mcspix_clk clock period
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.
- (5) Case 1/P = 48MHz:
- $A=(TCS+1) * T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).
Case 1/P < 48MHz
- $A=(TCS+0.5) * F_{RATIO} * T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).
For more information, see the McSPI chapter of Device TRM.
- (6) $B = (TCS+0.5) * T_{SPICLKREF} * F_{RATIO}$ (TCS is a bit field of MCSPI_CHxCONF register, F_{RATIO} : Even = 2).
For more information, see the McSPI chapter of Device TRM.
- (7) mcspix_clk phase is programmable with the bit PHA, of MCSPI_CHxCONF register.
- (8) In mcspix_clk, mcspix_simo, x is equal to 1, 2 or 4.
- (9) mcspix_cs is equal to mcspi1_cs[3:0], mcspi2_cs[1:0] or mcspi4_cs0
- (10) See [Section 4.3](#) for CORE OPP voltages.



SWPS050_McSPI_01

Figure 6-42. McSPI1, McSPI2 and McSPI4 – Master Mode Receive (1)(2)(3)(4)

- (1) The active clock edge selection of `mcspix_clk` (rising or falling) on which `mcspix_simo` is driven is software configurable with the bit `MCSP1_CHxCONF[1] = POL` and the bit `MCSP1_CHxCONF[0] = PHA`.
- (2) The polarity of `mcspxi_cs` is software configurable with the bit `MCSP1_CHxCONF[6] = EPOL`.
- (3) In `mcspix_clk`, `mcspix_simo`, `x` is equal to 1, 2 or 4.
- (4) `mcspxi_cs` is equal to `mcspi1_cs[3:0]`, `mcspi2_cs[1:0]` or `mcspi4_cs0`



SWPS050_McSPI_02

Figure 6-43. McSPI1, McSPI2 and McSPI4 – Master Mode Transmit (1)(2)(3)(4)

- (1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_simo is driven is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.
- (2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL
- (3) In mcspix_clk, mcspix_simo, x is equal to 1, 2 or 4.
- (4) mcspix_cs is equal to mcspi1_cs[3:0], mcspi2_cs[1:0] or mcspi4_cs0

6.6.3.2 McSPI3 – 1 Peripheral – SDR – Master – 48 MHz

Table 6-48. McSPI3 Timing Conditions – Master Mode – 48 MHz

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|---------------------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t _R | Input signal rise time | 1000 | 4000 | ps |
| t _F | Input signal fall time | 1000 | 4000 | ps |
| Output Condition⁽¹⁾ | | | | |

(1) See [Table 7-14](#).

(2) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

Table 6-49. McSPI3 Timing Requirements – Master Mode – 48 MHz ⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| SM4 | $t_{su(SOMI-CLKAE)}$ | Setup time, mcspix_somi ⁽²⁾ valid before mcspix_clk ⁽¹⁾⁽²⁾ active edge | 2.52 | | ns |
| SM5 | $t_{h(CLKAE-SOMI)}$ | Hold time, mcspix_somi ⁽²⁾ valid after mcspix_clk ⁽¹⁾⁽²⁾ active edge | 3.43 | | ns |

(1) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(2) In mcspix_clk and mcspix_somi, x is equal to 3.

(3) See [Section 4.3](#) for CORE OPP voltages.

Table 6-50. McSPI3 Switching Requirements – Master Mode – 48 Mhz ⁽¹⁰⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT | |
|--------------------|-------------------|---|----------------------|-------------------------|------|----|
| | | | MIN | MAX | | |
| SM1 | $1 / t_{C(CLK)}$ | Frequency ⁽²⁾ , mcspix_clk ^{(1) (8)} | | 48 | MHz | |
| SM2 | $t_{W(CLKL)}$ | Typical Pulse duration, mcspix_clk ⁽⁴⁾ low | 0.5*P ⁽²⁾ | | ns | |
| SM3 ⁽⁸⁾ | $t_{W(CLKH)}$ | Typical Pulse duration, mcspix_clk ⁽⁴⁾⁽⁸⁾ high | 0.5*P ⁽²⁾ | | ns | |
| | $t_{dc(clk)}$ | Duty cycle error, mcspix_clk ⁽⁸⁾ | | 1042 | ps | |
| | $t_{j(clk)}$ | Jitter standard deviation ⁽³⁾ , mcspix_clk ⁽⁸⁾ | | 65 | ps | |
| | $t_{R(clk)}$ | Rise time, mcspix_clk ⁽⁸⁾ | | 4000.0 | ps | |
| | $t_{F(clk)}$ | Fall time, mcspix_clk ⁽⁸⁾ | | 4000.0 | ps | |
| SM6 | $t_{d(CLK-SIMO)}$ | Delay time, mcspix_clk ⁽⁴⁾⁽⁸⁾ active edge to mcspix_simo ⁽⁸⁾ transition | -3.59 | 3.63 | ns | |
| SM7 | $t_{d9CS-SIMO}$ | Delay time, mcspix_cs ⁽⁹⁾ active edge to mcspix_simo ⁽⁸⁾ transition | PHA=0 ⁽⁷⁾ | 3.63 | 3.63 | ns |
| SM8 | $t_{d(CS-CLK)}$ | Delay time, mcspix_cs ⁽⁹⁾ active to mcspix_clk ⁽⁴⁾ first edge | PHA=1 ⁽⁷⁾ | A ⁽⁵⁾ - 4.25 | ns | |
| | | | PHA=0 ⁽⁷⁾ | B ⁽⁶⁾ - 4.25 | ns | |
| SM9 | $t_{d(CLK-CS)}$ | Delay time, mcspix_clk ⁽⁴⁾⁽⁸⁾ last edge to mcspix_cs ⁽⁹⁾ inactive | PHA=1 ⁽⁷⁾ | B ⁽⁶⁾ - 4.22 | ns | |
| | | | PHA=0 ⁽⁷⁾ | A ⁽⁵⁾ - 4.22 | ns | |
| | $t_{R(SIMO)}$ | Rise time, mcspix_simo ⁽⁸⁾ | | 4000.0 | ps | |
| | $t_{F(SIMO)}$ | Fall time, mcspix_simo ⁽⁸⁾ | | 4000.0 | ps | |
| | $t_{R(CS)}$ | Rise time, mcspix_cs ⁽⁹⁾ | | 4000.0 | ps | |
| | $t_{F(CS)}$ | Fall time, mcspix_cs ⁽⁹⁾ | | 4000.0 | ps | |

(1) Related with the mcspix_clk maximum frequency programmable in the MCSPI module by setting the configuration register MCSPI_CHxCONF. For more information, see the McSPI environment chapter, Data Format Configurations section of the Device TRM for modes and phase correspondence description.

(2) P = mcspix_clk clock period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(5) Case 1/P = 48MHz:

- $A=(TCS+1) * T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).

Case 1/P < 48MHz

- $A=(TCS+0.5) * F_{RATIO} * T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).

For more information, see the McSPI chapter of Device TRM.

(6) B = (TCS+0.5) * $T_{SPICLKREF} * F_{RATIO}$ (TCS is a bit field of MCSPI_CHxCONF register, F_{RATIO} : Even = 2).

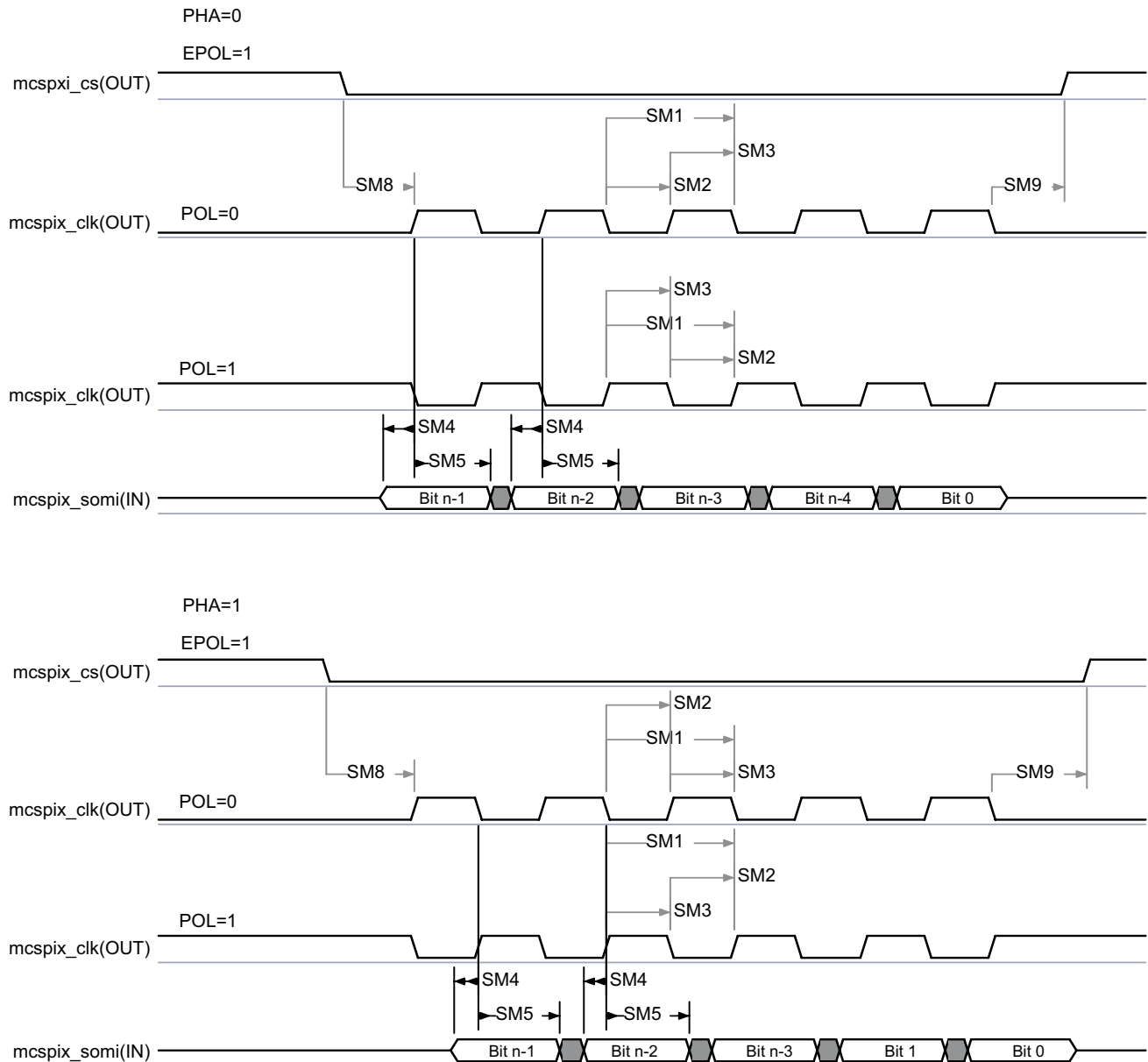
For more information, see the McSPI chapter of Device TRM.

(7) mcspix_clk phase is programmable with the bit PHA, of MCSPI_CHxCONF register.

(8) In mcspix_clk, mcspix_simo, x is equal to 3.

(9) mcspix_cs is equal to mcspi3_cs0

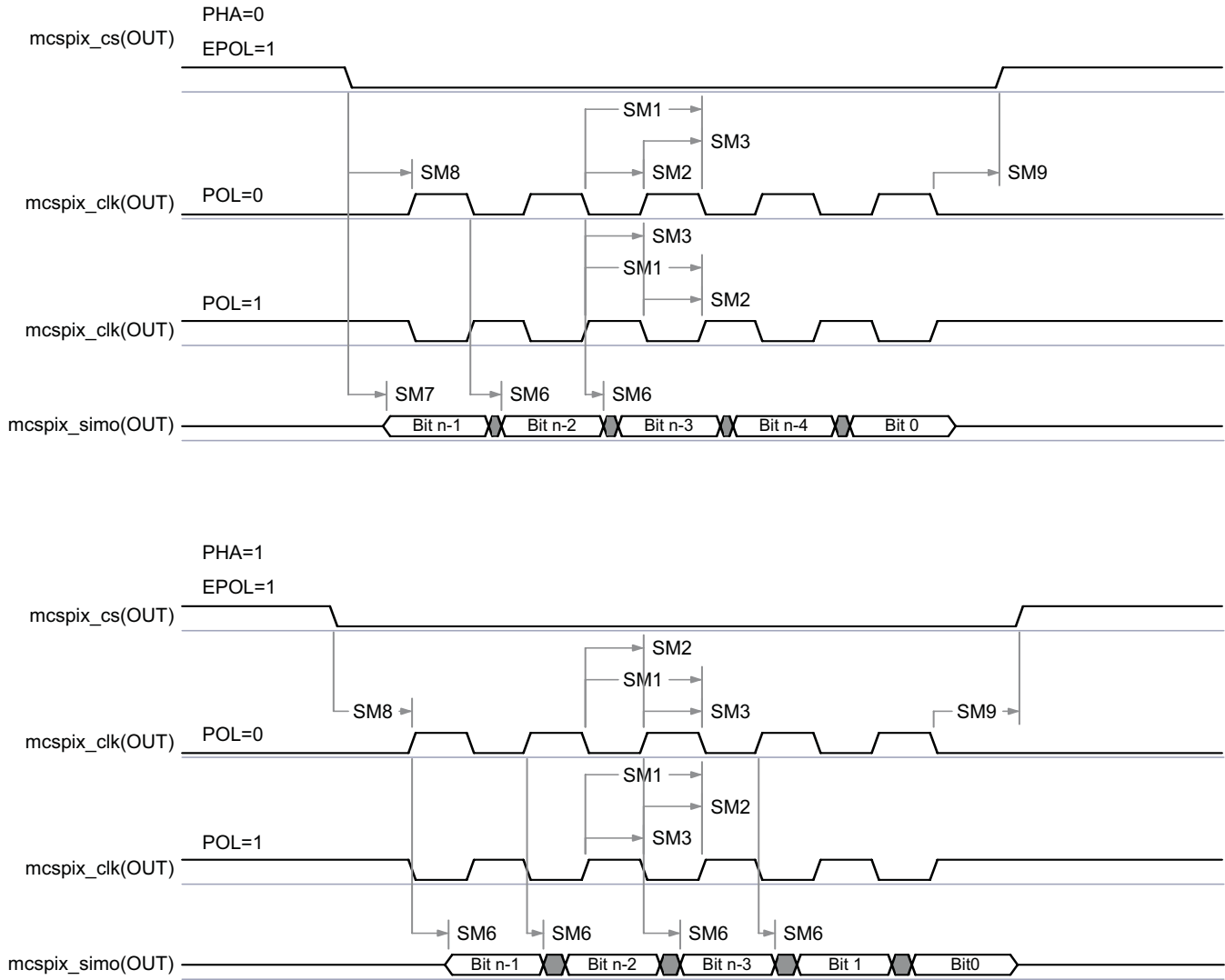
(10) See [Section 4.3](#) for CORE OPP voltages.



SWPS050_McSPI_01

Figure 6-44. McSPI3 – Master Mode Receive (1)(2)(3)(4)

- (1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_somi data is latched is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.
- (2) The polarity of mcspxi_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL
- (3) In mcspix_clk, mcspix_somi, x is equal to 3
- (4) mcspxi_cs is equal to mcspi3_cs0



SWPS050_McSPI_02

Figure 6-45. McSPI3 – Master Mode Transmit (1)(2)(3)(4)

- (1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_somi data is latched is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.
- (2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL
- (3) In mcspix_clk, mcspix_somi, x is equal to 3
- (4) mcspix_cs is equal to mcspi3_cs0

6.6.3.3 McSPI1 and McSPI2 – 2 Peripherals – SDR – Master – 24 MHz

Table 6-51. McSPI1 and McSPI2 Timing Conditions – Master Mode – 24 MHz

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t _R | Input signal rise time | 100 | 7500 | ps |
| t _F | Input signal fall time | 100 | 7500 | ps |
| Output Condition | | | | |

- (1) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding Device VDDS power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-52](#) and [Table 6-53](#) assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 6-52. McSPI1 and McSPI2 Timing Requirements – Master Mode – 24 MHz ⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| SM4 | $t_{su}(SOMI-CLKAE)$ | Setup time, mcspix_somi ⁽²⁾ valid before mcspix_clk ⁽¹⁾⁽²⁾ active edge | 2.47 | | ns |
| SM5 | $t_h(CLKAE-SOMI)$ | Hold time, mcspix_somi ⁽²⁾ valid after mcspix_clk ⁽¹⁾⁽²⁾ active edge | 2.17 | | ns |

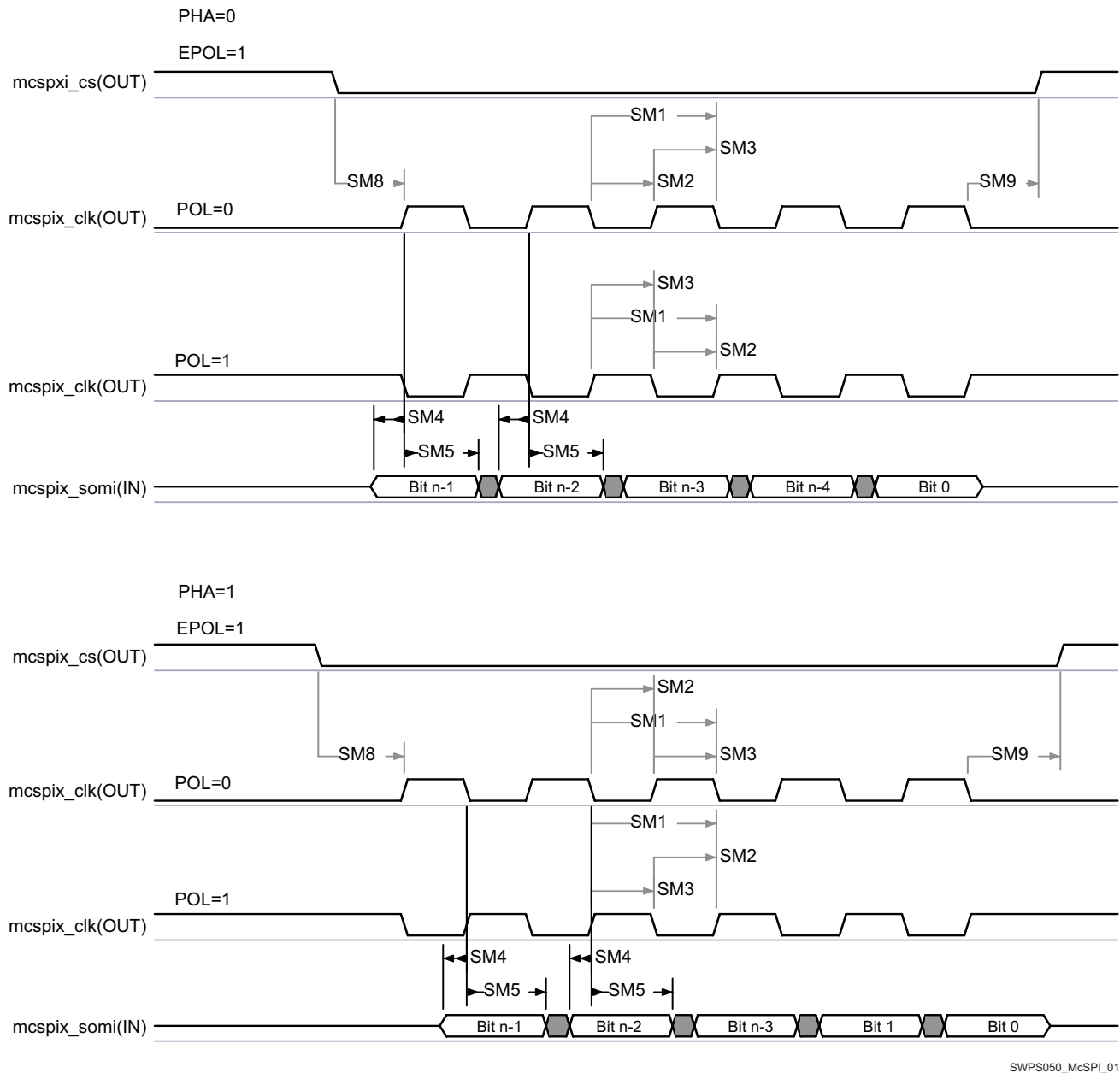
- (1) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.
- (2) In mcspix_clk and mcspix_somi, x is equal to 1 or 2.
- (3) See [Section 4.3](#) for CORE OPP voltages.

Table 6-53. McSPI1 and McSPI2 Switching Requirements – Master Mode – 24 MHz ⁽¹⁰⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT | |
|-----|-----------------|---|----------------------|-------------------------|------|----|
| | | | MIN | MAX | | |
| SM1 | $1 / t_C(CLK)$ | Frequency ⁽²⁾ , mcspix_clk ⁽¹⁾⁽⁸⁾ | | 24 | MHz | |
| SM2 | $t_W(CLKL)$ | Typical Pulse duration, mcspix_clk ⁽⁴⁾⁽⁸⁾ low | 0.5*P ⁽²⁾ | | ns | |
| SM3 | $t_W(CLKH)$ | Typical Pulse duration, mcspix_clk ⁽⁴⁾⁽⁸⁾ high | 0.5*P ⁽²⁾ | | ns | |
| | $t_{dc}(clk)$ | Duty cycle error, mcspix_clk ⁽⁸⁾ | | 2083 | ps | |
| | $t_J(clk)$ | Jitter standard deviation ⁽³⁾ , mcspix_clk ⁽⁸⁾ | | 65 | ps | |
| | $t_R(clk)$ | Rise time, mcspix_clk ⁽⁸⁾ | | 5542 | ps | |
| | $t_F(clk)$ | Fall time, mcspix_clk ⁽⁸⁾ | | 5083 | ps | |
| SM6 | $t_d(CLK-SIMO)$ | Delay time, mcspix_clk ⁽⁴⁾⁽⁸⁾ active edge to mcspix_simo ⁽⁸⁾ transition | -4.59 | 4.59 | ns | |
| SM7 | $t_{d9CS-SIMO}$ | Delay time, mcspix_cs ⁽⁹⁾ active edge to mcspix_simo ⁽⁸⁾ transition | PHA=0 ⁽⁷⁾ | 4.59 | 3.63 | ns |
| SM8 | $t_d(CS-CLK)$ | Delay time, mcspix_cs ⁽⁹⁾ active to mcspix_clk ⁽⁴⁾ first edge | PHA=1 ⁽⁷⁾ | A ⁽⁵⁾ - 2.5 | | ns |
| | | | PHA=0 ⁽⁷⁾ | B ⁽⁶⁾ - 2.5 | | ns |
| SM9 | $t_d(CLK-CS)$ | Delay time, mcspix_clk ⁽⁴⁾⁽⁸⁾ last edge to mcspix_cs ⁽⁹⁾ inactive | PHA=1 ⁽⁷⁾ | B ⁽⁶⁾ - 2.57 | | ns |
| | | | PHA=0 ⁽⁷⁾ | A ⁽⁵⁾ - 2.57 | | ns |
| | $t_R(SIMO)$ | Rise time, mcspix_simo ⁽⁸⁾ | | 5542 | ps | |
| | $t_F(SIMO)$ | Fall time, mcspix_simo ⁽⁸⁾ | | 5083 | ps | |
| | $t_R(CS)$ | Rise time, mcspix_cs ⁽⁹⁾ | | 5542 | ps | |
| | $t_F(CS)$ | Fall time, mcspix_cs ⁽⁹⁾ | | 5083 | ps | |

- (1) Related with the mcspix_clk maximum frequency programmable in the MCSPI module by setting the configuration register MCSPI_CHxCONF.
For more information, see the McSPI environment chapter, Data Format Configurations section of the Device TRM for modes and phase correspondence description.
- (2) P = mcspix_clk clock period
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.
- (5) Case 1/P = 48MHz:
- A=(TCS+1) * T_{SPICLKREF} (TCS is a bit field of MCSPI_CHxCONF register).
Case 1/P < 48MHz
- A=(TCS+0.5) * F_{RATIO} * T_{SPICLKREF} (TCS is a bit field of MCSPI_CHxCONF register).
For more information, see the McSPI chapter of Device TRM.
- (6) B = (TCS+0.5) * T_{SPICLKREF} * F_{RATIO} (TCS is a bit field of MCSPI_CHxCONF register, F_{RATIO}: Even = 2).
For more information, see the McSPI chapter of Device TRM.
- (7) mcspix_clk phase is programmable with the bit PHA, of MCSPI_CHxCONF register.
- (8) In mcspix_clk, mcspix_simo, x is equal to 1 or 2.

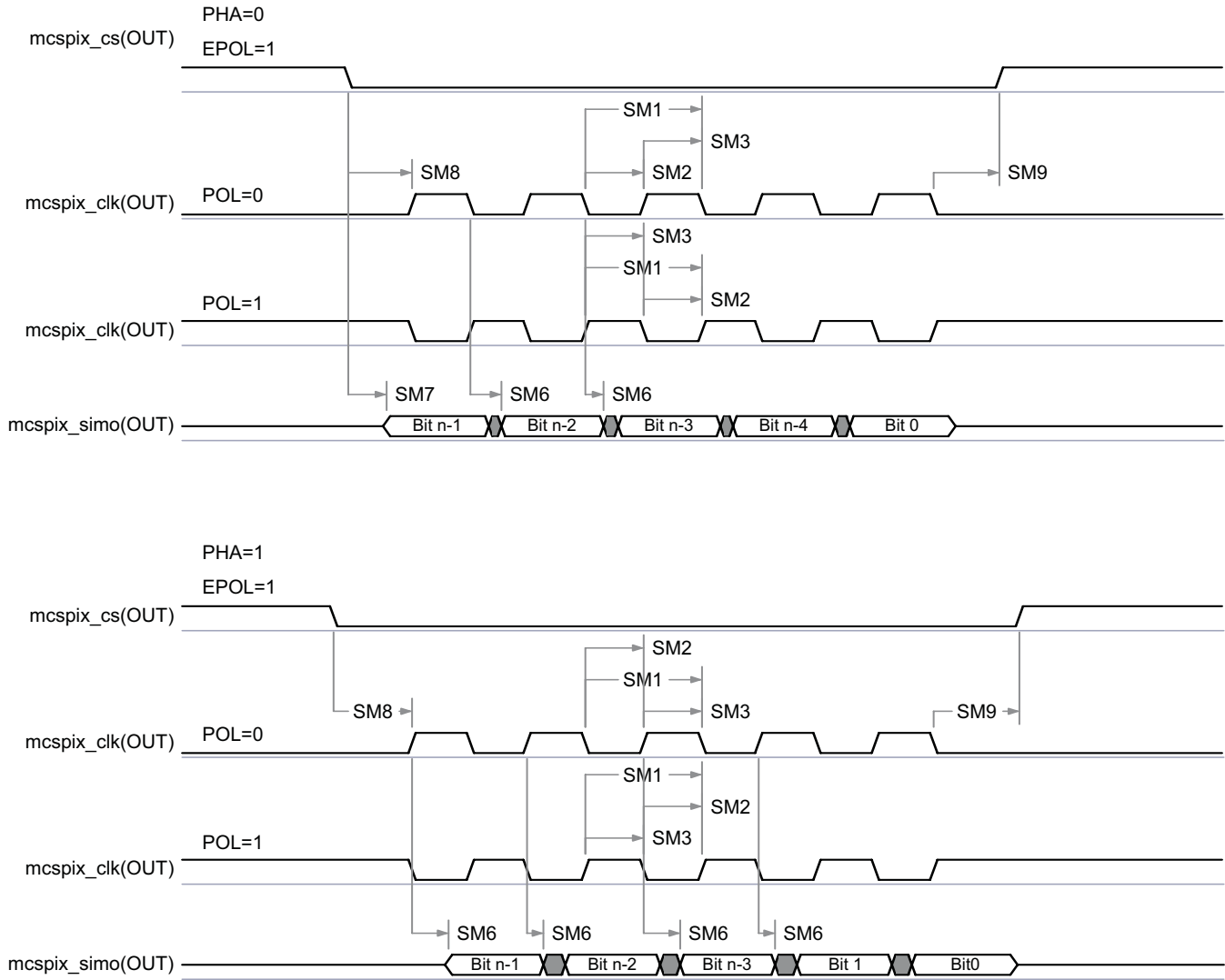
- (9) mcspx_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0].
 (10) See [Section 4.3](#) for CORE OPP voltages.



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Figure 6-46. McSPI1 McSPI2 – Master Mode Receive (1)(2)(3)(4)

- (1) The active clock edge selection of mcspx_clk (rising or falling) on which mcspx_simo is driven is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.
- (2) The polarity of mcspx_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL
- (3) In mcspx_clk, mcspx_simo, x is equal to 1 or 2.
- (4) mcspx_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]



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Figure 6-47. McSPI1 McSPI2 – Master Mode Transmit (1)(2)(3)(4)

- (1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_simo is driven is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.
- (2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL
- (3) In mcspix_clk, mcspix_simo, x is equal to 1 or 2.
- (4) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]

6.6.3.4 McSPI1 and McSPI2 – 1 Peripheral – SDR – Master – 12 MHz

Table 6-54. McSPI1 and McSPI2 Timing Conditions – Master Mode – 12 MHz

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|-------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t _R | Input signal rise time | 100 | 12000 | ps |
| t _F | Input signal fall time | 100 | 12000 | ps |
| Output Condition | | | | |

- (1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-55](#) and [Table 6-56](#) assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 6-55. McSPI1 and McSPI2 Timing Requirements – Master Mode – 12 MHz ⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| SM4 | $t_{su(SOMI-CLKAE)}$ | Setup time, mcspix_somi ⁽²⁾ valid before mcspix_clk ⁽¹⁾⁽²⁾ active edge | 4.25 | | ns |
| SM5 | $t_{h(CLKAE-SOMI)}$ | Hold time, mcspix_somi ⁽²⁾ valid after mcspix_clk ⁽¹⁾⁽²⁾ active edge | -0.34 | | ns |

- (1) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

- (2) In mcspix_clk and mcspix_somi, x is equal to 1 or 2.

- (3) See [Section 4.3](#) for CORE OPP voltages.

Table 6-56. McSPI1 and McSPI2 Switching Requirements – Master Mode – 12 MHz ⁽¹⁰⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT | |
|-----|-------------------|---|----------------------|-------------------------|------|----|
| | | | MIN | MAX | | |
| SM1 | $1 / t_{C(CLK)}$ | Frequency ⁽²⁾ , mcspix_clk ⁽¹⁾⁽⁸⁾ | | 12 | MHz | |
| SM2 | $t_{W(CLKL)}$ | Typical Pulse duration, mcspix_clk ⁽⁴⁾⁽⁸⁾ low | 0.5*P ⁽²⁾ | | ns | |
| SM3 | $t_{W(CLKH)}$ | Typical Pulse duration, mcspix_clk ⁽⁴⁾⁽⁸⁾ high | 0.5*P ⁽²⁾ | | ns | |
| | $t_{dc(clk)}$ | Duty cycle error, mcspix_clk ⁽⁸⁾ | | 4167 | ps | |
| | $t_{J(clk)}$ | Jitter standard deviation ⁽³⁾ , mcspix_clk ⁽⁸⁾ | | 65 | ps | |
| | $t_{R(clk)}$ | Rise time, mcspix_clk ⁽⁸⁾ | | 5544 | ps | |
| | $t_{F(clk)}$ | Fall time, mcspix_clk ⁽⁸⁾ | | 5234 | ps | |
| SM6 | $t_{d(CLK-SIMO)}$ | Delay time, mcspix_clk ⁽⁴⁾⁽⁸⁾ active edge to mcspix_simo ⁽⁸⁾ transition | -16.62 | 12.80 | ns | |
| SM7 | $t_{d9CS-SIMO}$ | Delay time, mcspix_cs ⁽⁹⁾ active edge to mcspix_simo ⁽⁸⁾ transition | PHA=0 ⁽⁷⁾ | 12.80 | 3.63 | ns |
| SM8 | $t_{d(CS-CLK)}$ | Delay time, mcspix_cs ⁽⁹⁾ active to mcspix_clk ⁽⁴⁾ first edge | PHA=1 ⁽⁷⁾ | A ⁽⁵⁾ – 12.8 | | ns |
| | | | PHA=0 ⁽⁷⁾ | B ⁽⁶⁾ – 12.8 | | ns |
| SM9 | $t_{d(CLK-CS)}$ | Delay time, mcspix_clk ⁽⁴⁾⁽⁸⁾ last edge to mcspix_cs ⁽⁹⁾ inactive | PHA=1 ⁽⁷⁾ | B ⁽⁶⁾ – 0.01 | | ns |
| | | | PHA=0 ⁽⁷⁾ | A ⁽⁵⁾ – 0.01 | | ns |
| | $t_{R(SIMO)}$ | Rise time, mcspix_simo ⁽⁸⁾ | | 5544 | ps | |
| | $t_{F(SIMO)}$ | Fall time, mcspix_simo ⁽⁸⁾ | | 5234 | ps | |
| | $t_{R(CS)}$ | Rise time, mcspix_cs ⁽⁹⁾ | | 5544 | ps | |
| | $t_{F(CS)}$ | Fall time, mcspix_cs ⁽⁹⁾ | | 5234 | ps | |

- (1) Related with the mcspix_clk maximum frequency programmable in the MCSPI module by setting the configuration register MCSPI_CHxCONF.

For more information, see the McSPI environment chapter, Data Format Configurations section of the Device TRM for modes and phase correspondence description.

- (2) P = mcspix_clk clock period

- (3) The jitter probability density can be approximated by a Gaussian function.

- (4) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

- (5) Case 1/P = 48MHz:

- A=(TCS+1) * T_{SPICLKREF} (TCS is a bit field of MCSPI_CHxCONF register).

Case 1/P < 48MHz

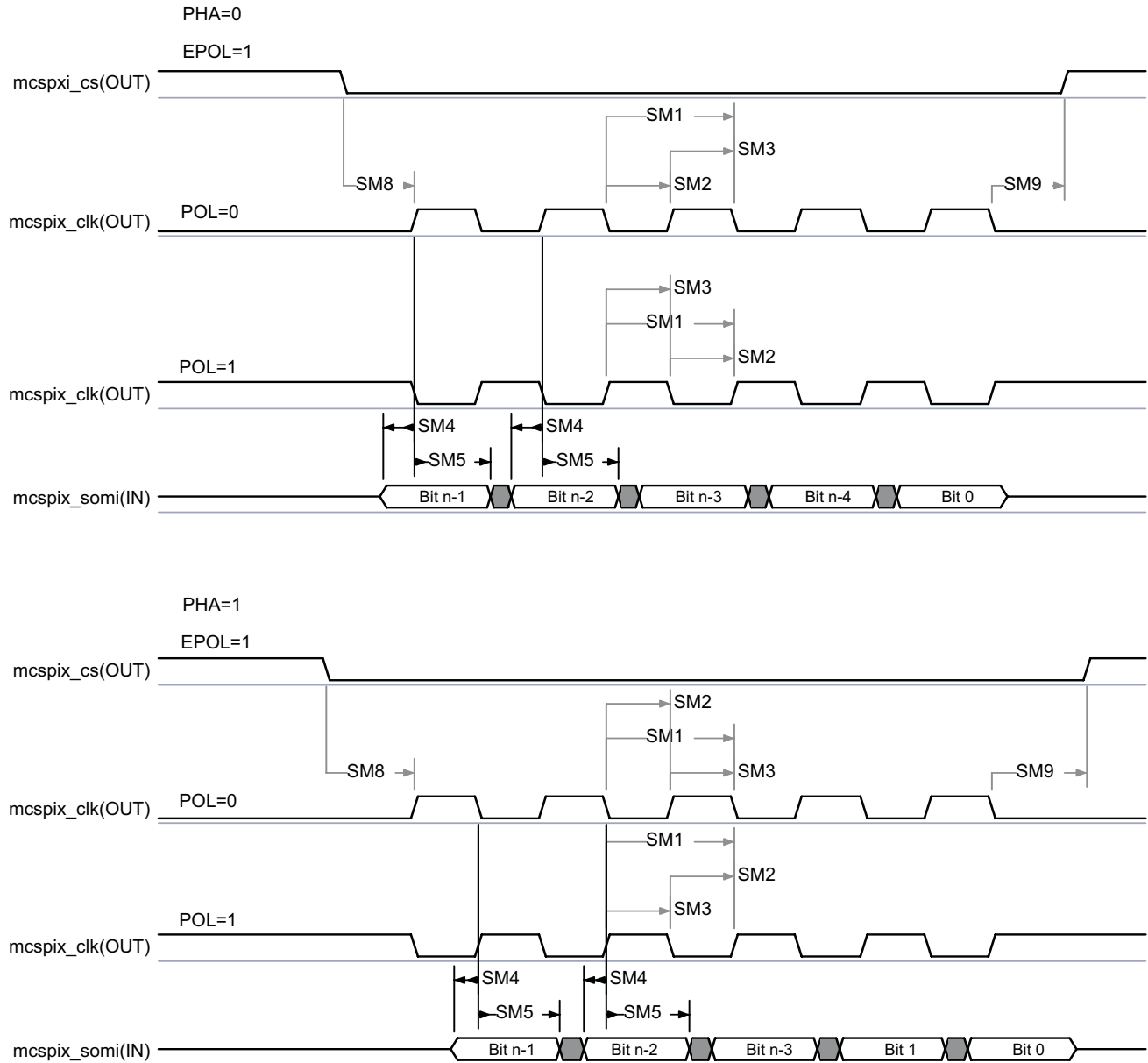
- A=(TCS+0.5) * F_{RATIO} * T_{SPICLKREF} (TCS is a bit field of MCSPI_CHxCONF register).

For more information, see the McSPI chapter of Device TRM.

- (6) B = (TCS+0.5) * T_{SPICLKREF} * F_{RATIO} (TCS is a bit field of MCSPI_CHxCONF register, F_{RATIO}: Even = 2).

For more information, see the McSPI chapter of Device TRM.

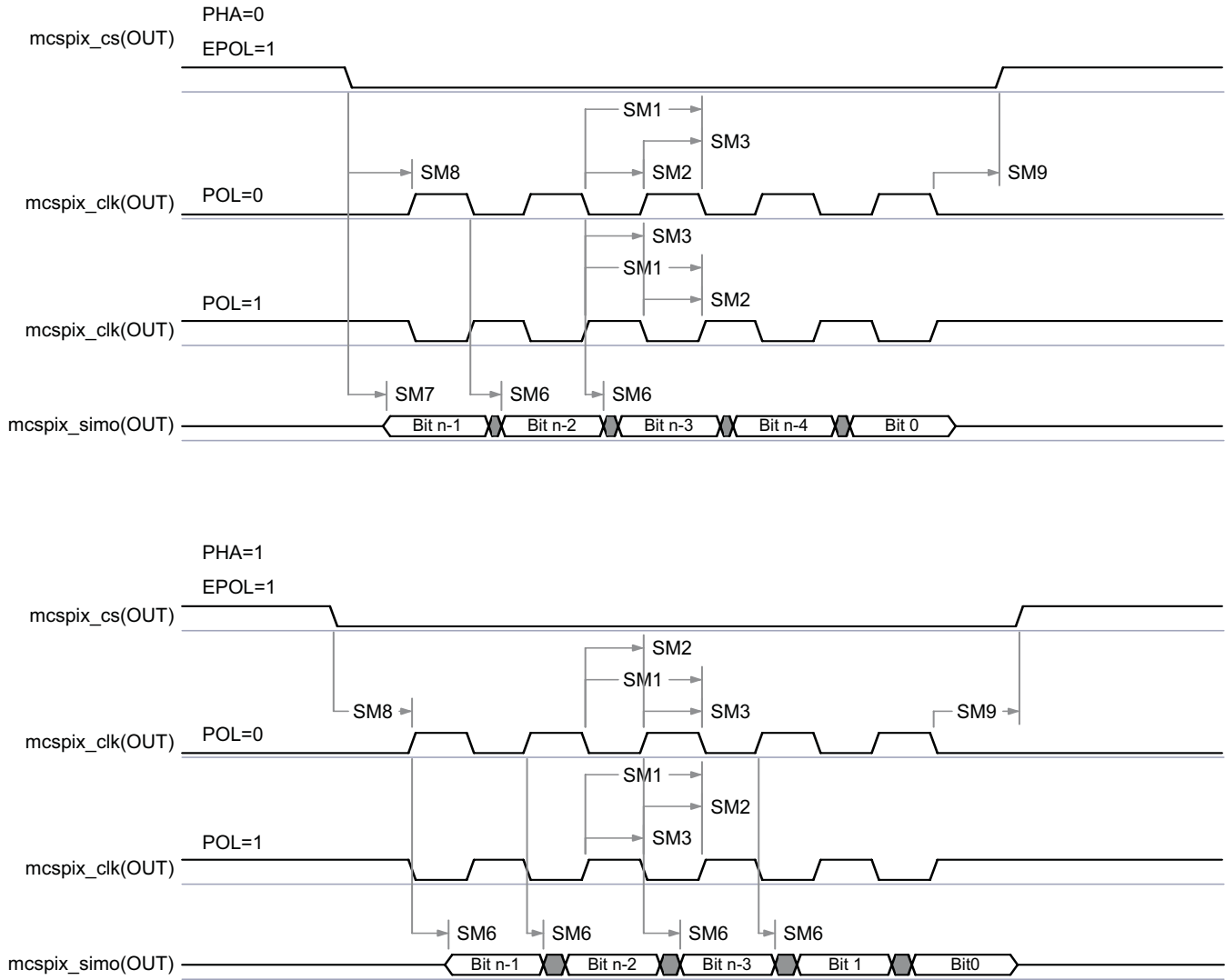
- (7) mcspx_clk phase is programmable with the bit PHA, of MCSPI_CHxCONF register.
- (8) In mcspx_clk, mcspx_simo, x is equal to 1 or 2.
- (9) mcspx_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]
- (10) See Section 4.3 for CORE OPP voltages.



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Figure 6-48. McSPI1 and McSPI2 - Master Mode Receive (1)(2)(3)(4)

- (1) The active clock edge selection of mcspx_clk (rising or falling) on which mcspx_somi data is latched is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.
- (2) The polarity of mcspx_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL
- (3) In mcspx_clk, mcspx_somi, x is equal to 1 or 2
- (4) mcspx_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]



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Figure 6-49. McSPI1 and McSPI2 – Master Mode Transmit (1)(2)(3)(4)

- (1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_somi data is latched is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.
- (2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL
- (3) In mcspix_clk, mcspix_somi, x is equal to 1 or 2
- (4) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]

6.6.3.5 McSPI1 and McSPI2 – 1 Peripheral – SDR – Master – 12 MHz

Table 6-57. McSPI1 and McSPI2 Timing Conditions – Master Mode – 12 MHz

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|-------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t _R | Input signal rise time | 100 | 12000 | ps |
| t _F | Input signal fall time | 100 | 12000 | ps |
| Output Condition | | | | |

- (1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-58](#) and [Table 6-59](#) assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 6-58. McSPI1 and McSPI2 Timing Requirements – Master Mode – 12 MHz ⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------|---|---------|-----|------|
| | | | MIN | MAX | |
| SM4 | $t_{su}(SOMI-CLKAE)$ | Setup time, mcspix_somi ⁽²⁾ valid before mcspix_clk ^{(1) (2)} active edge | 18.87 | | ns |
| SM5 | $t_h(CLKAE-SOMI)$ | Hold time, mcspix_somi ⁽²⁾ valid after mcspix_clk ^{(1) (2)} active edge | -0.99 | | ns |

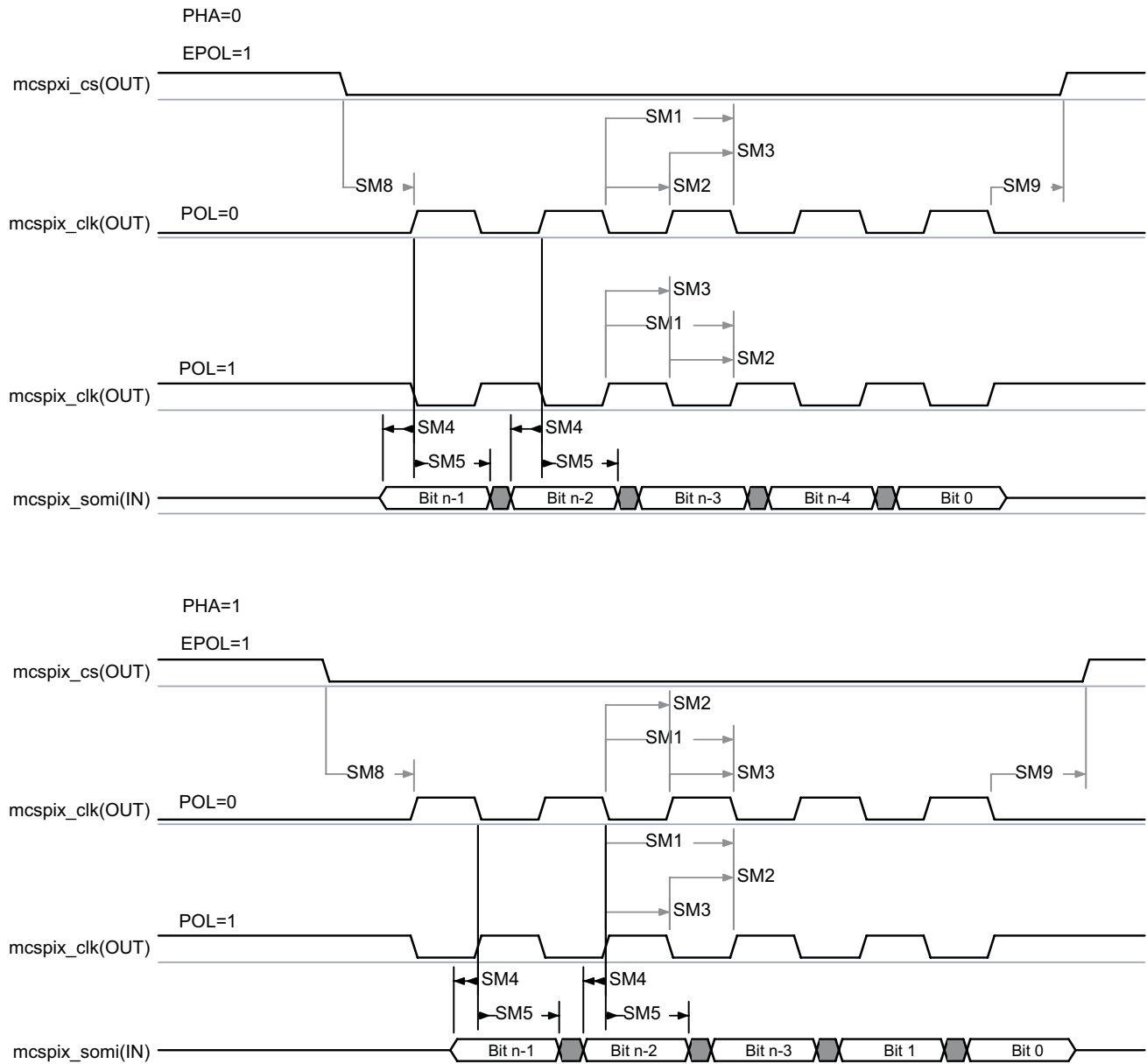
- (1) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.
- (2) In mcspix_clk and mcspix_somi, x is equal to 1 or 2.
- (3) See [Section 4.3](#) for CORE OPP voltages.

Table 6-59. McSPI1 and McSPI2 Switching Requirements – Master Mode – 12 MHz ⁽¹⁰⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT | |
|-----|-----------------|---|----------------------|-----------------------------|------|----|
| | | | MIN | MAX | | |
| SM1 | $1 / t_C(CLK)$ | Frequency ⁽²⁾ , mcspix_clk ⁽¹⁾⁽⁹⁾ | | 12 | MHz | |
| SM2 | $t_W(CLKL)$ | Typical Pulse duration, mcspix_clk ⁽⁴⁾⁽⁸⁾ low | 0.5*P ⁽²⁾ | | ns | |
| SM3 | $t_W(CLKH)$ | Typical Pulse duration, mcspix_clk ⁽⁴⁾⁽⁸⁾ high | 0.5*P ⁽²⁾ | | ns | |
| | $t_{dc}(clk)$ | Duty cycle error, mcspix_clk ⁽⁸⁾ | | 4167 | ps | |
| | $t_{J}(clk)$ | Jitter standard deviation ⁽³⁾ , mcspix_clk ⁽⁸⁾ | | 539 | ps | |
| | $t_{R}(clk)$ | Rise time, mcspix_clk ⁽⁸⁾ | | 4860 | ps | |
| | $t_{F}(clk)$ | Fall time, mcspix_clk ⁽⁸⁾ | | 4140 | ps | |
| SM6 | $t_d(CLK-SIMO)$ | Delay time, mcspix_clk ⁽⁴⁾⁽⁸⁾ active edge to mcspix_simo ⁽⁸⁾ transition | -7.10 | 2.97 | ns | |
| SM7 | $t_{d9CS-SIMO}$ | Delay time, mcspix_cs ⁽⁹⁾ active edge to mcspix_simo ⁽⁸⁾ transition | PHA=0 ⁽⁷⁾ | 2.97 | 3.63 | ns |
| SM8 | $t_d(CS-CLK)$ | Delay time, mcspix_cs ⁽⁹⁾ active to mcspix_clk ⁽⁴⁾ first edge | PHA=1 ⁽⁷⁾ | A ⁽⁵⁾ - 39.49 | | ns |
| | | | PHA=0 ⁽⁷⁾ | B ⁽⁶⁾ - 39.49 | | ns |
| SM9 | $t_d(CLK-CS)$ | Delay time, mcspix_clk ⁽⁴⁾⁽⁸⁾ last edge to mcspix_cs ⁽⁹⁾ inactive | PHA=1 ⁽⁷⁾ | B ⁽⁶⁾ - 43.63 | | ns |
| | | | PHA=0 ⁽⁷⁾ | A ⁽⁵⁾ - 43.63 | | ns |
| | $t_{R}(SIMO)$ | Rise time, mcspix_simo ⁽⁸⁾ | | 4860 | ps | |
| | $t_{F}(SIMO)$ | Fall time, mcspix_simo ⁽⁸⁾ | | 4140 | ps | |
| | $t_{R}(CS)$ | Rise time, mcspix_cs ⁽⁹⁾ | | 4860 | ps | |
| | $t_{F}(CS)$ | Fall time, mcspix_cs ⁽⁹⁾ | | 4140 | ps | |

- (1) Related with the mcspix_clk maximum frequency programmable in the MCSPI module by setting the configuration register MCSPI_CHxCONF.
For more information, see the McSPI environment chapter, Data Format Configurations section of the Device TRM for modes and phase correspondence description.
- (2) P = mcspix_clk clock period
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.
- (5) Case 1/P = 48MHz:
- A=(TCS+1) * T_{SPICLKREF} (TCS is a bit field of MCSPI_CHxCONF register).
Case 1/P < 48MHz
- A=(TCS+0.5) * F_{RATIO} * T_{SPICLKREF} (TCS is a bit field of MCSPI_CHxCONF register).
For more information, see the McSPI chapter of Device TRM.
- (6) B = (TCS+0.5) * T_{SPICLKREF} * F_{RATIO} (TCS is a bit field of MCSPI_CHxCONF register, F_{RATIO}: Even * 2).
For more information, see the McSPI chapter of Device TRM.

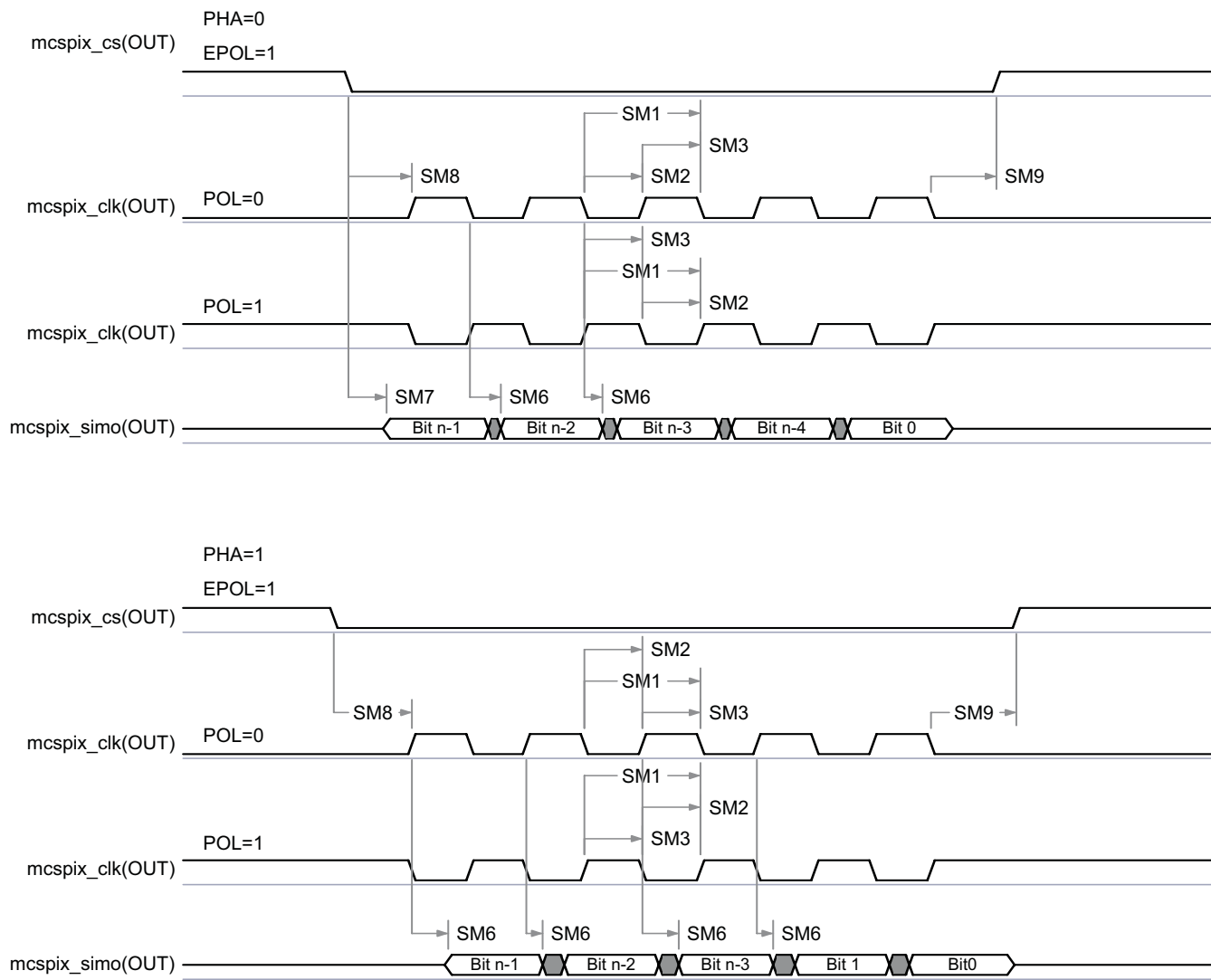
- (7) mcspx_clk phase is programmable with the bit PHA, of MCSPI_CHxCONF register.
- (8) In mcspx_clk, mcspx_simo, x is equal to 1 or 2.
- (9) mcspx_cs is equal to mcspx1_cs[3:0] or mcspx2_cs[1:0].
- (10) See [Section 4.3](#) for CORE OPP voltages.



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Figure 6-50. McSPI1 McSPI2 – Master Mode Receive ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

- (1) The active clock edge selection of `mcspx_clk` (rising or falling) on which `mcspx_somi` data is latched is software configurable with the bit `MCSPI_CHxCONF[1] = POL` and the bit `MCSPI_CHxCONF[0] = PHA`.
- (2) The polarity of `mcspx_cs` is software configurable with the bit `MCSPI_CHxCONF[6] = EPOL`.
- (3) In `mcspx_clk`, `mcspx_somi`, x is equal to 1 or 2.
- (4) `mcspx_cs` is equal to `mcspx1_cs[3:0]` or `mcspx2_cs[1:0]`.



SWPS050_McSPI_02

Figure 6-51. McSPI1 and McSPI2 – Master Mode Transmit (1)(2)(3)(4)

- (1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_simo is driven is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.
- (2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL
- (3) In mcspix_clk, mcspix_simo, x is equal to 1 or 2.
- (4) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]

6.6.3.6 McSPI3 and McSPI4 – 1 Peripheral – SDR – Slave – 24 MHz

Table 6-60. McSPI3 and McSPI4 Timing Conditions – Slave Mode – 24 MHz

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t _R | Input signal rise time | 370 | 1840 | ps |
| t _F | Input signal fall time | 370 | 1840 | ps |
| Output Condition | | | | |

- (1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-61](#) and [Table 6-62](#) assumes testing over the recommended operating conditions and electrical characteristic conditions below.

Table 6-61. McSPI3 and McSPI4 Timing Requirements – Slave Mode – 24 MHz (4)(8)

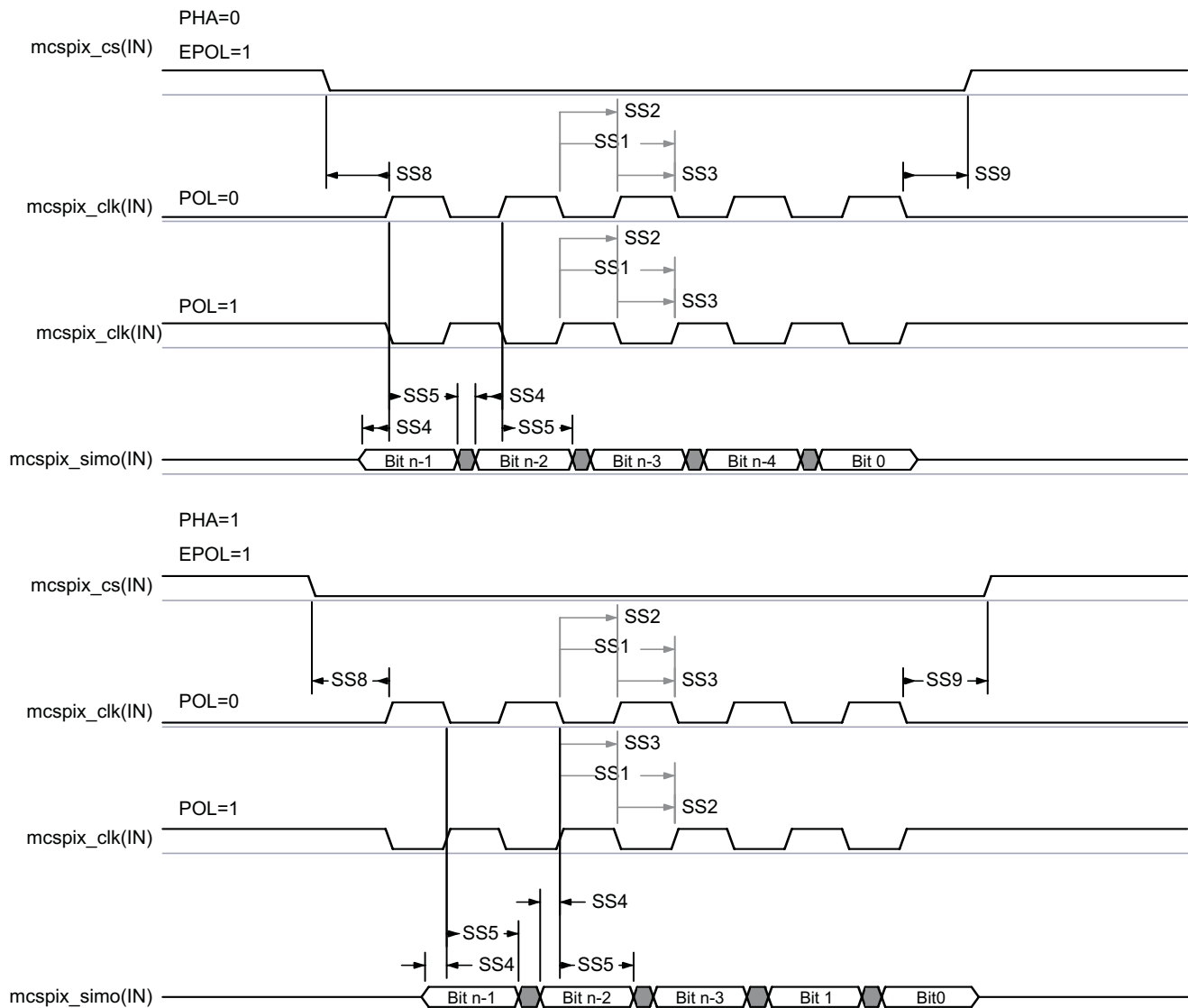
| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------|--|----------------------|------|------|
| | | | MIN | MAX | |
| SS1 | $1 / t_{C(CLK)}$ | Frequency ⁽²⁾ , mcspix_clk ⁽¹⁾⁽⁶⁾ | | 24 | MHz |
| SS2 | $t_{W(CLKL)}$ | Typical Pulse duration, mcspix_clk ⁽⁵⁾⁽⁶⁾ low | 0.5*P ⁽²⁾ | | ns |
| SS3 | $t_{W(CLKH)}$ | Typical Pulse duration, mcspix_clk ⁽⁵⁾⁽⁶⁾ high | 0.5*P ⁽²⁾ | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, mcspix_clk ⁽⁶⁾ | | 2083 | ps |
| | $t_{J(clk)}$ | Jitter standard deviation ⁽³⁾ , mcspix_clk ⁽⁶⁾ | | 1250 | ps |
| | $t_{R(clk)}$ | Rise time, mcspix_clk ⁽⁶⁾ | | 1840 | ps |
| | $t_{F(clk)}$ | Fall time, mcspix_clk ⁽⁶⁾ | | 1840 | ps |
| SS4 | $t_{su(SOMI-CLKAE)}$ | Setup time, mcspix_simo ⁽⁶⁾ valid before mcspix_clk ⁽⁵⁾⁽⁶⁾ active edge | 5.84 | | ns |
| SS5 | $t_{h(CLKAE-SOMI)}$ | Hold time, mcspix_simo ⁽⁶⁾ valid after mcspix_clk ⁽⁵⁾⁽⁶⁾ active edge | 5.84 | | ns |
| SS8 | $t_{su(CS-CLKAE)}$ | Setup time, mcspix_cs ⁽⁷⁾ valid before mcspix_clk ⁽⁵⁾⁽⁶⁾ active edge | 6.05 | | ns |
| SS9 | $t_{h(CLKAE-CS)}$ | Hold time, mcspix_cs ⁽⁷⁾ valid after mcspix_clk ⁽⁵⁾⁽⁶⁾ active edge | 6.05 | | ns |

- (1) Related with the mcspix_clk maximum frequency programmable in the MCSPI module by setting the configuration register MCSPI_CHxCONF.
For more information, see the McSPI environment chapter, Data Format Configurations section of the Device TRM for modes and phase correspondence description.
- (2) P = mcspix_clk clock period
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) The timing requirements are guaranteed till the cycle jitter and duty cycle error conditions specified.
- (5) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.
- (6) In mcspix_clk and mcspix_simo, x is equal to 3 or 4.
- (7) mcspix_cs is equal to mcspi3_cs0 or mcspi4_cs0
- (8) See [Section 4.3](#) for CORE OPP voltages.

Table 6-62. McSPI3 and McSPI4 Switching Requirements – Slave Mode – 24 MHz (5)

| NO. | PARAMETER | | OPP_NOM | | UNIT | |
|-----|-------------------|---|----------------------|------|-------|----|
| | | | MIN | MAX | | |
| SS6 | $t_{d(CLK-SIMO)}$ | Delay time, mcspix_clk ⁽¹⁾⁽³⁾ active edge to mcspix_somi ⁽³⁾ transition | | 1.39 | 10.28 | ns |
| SS7 | $t_{d(CS-SIMO)}$ | Delay time, mcspix_cs ⁽⁴⁾ active edge to mcspix_somi ⁽³⁾ transition | PHA=0 ⁽²⁾ | | 10.28 | ns |
| | $t_{R(SIMO)}$ | Rise time, mcspix_somi ⁽³⁾ | | | 4885 | ps |
| | $t_{F(SIMO)}$ | Fall time, mcspix_somi ⁽³⁾ | | | 4885 | ps |

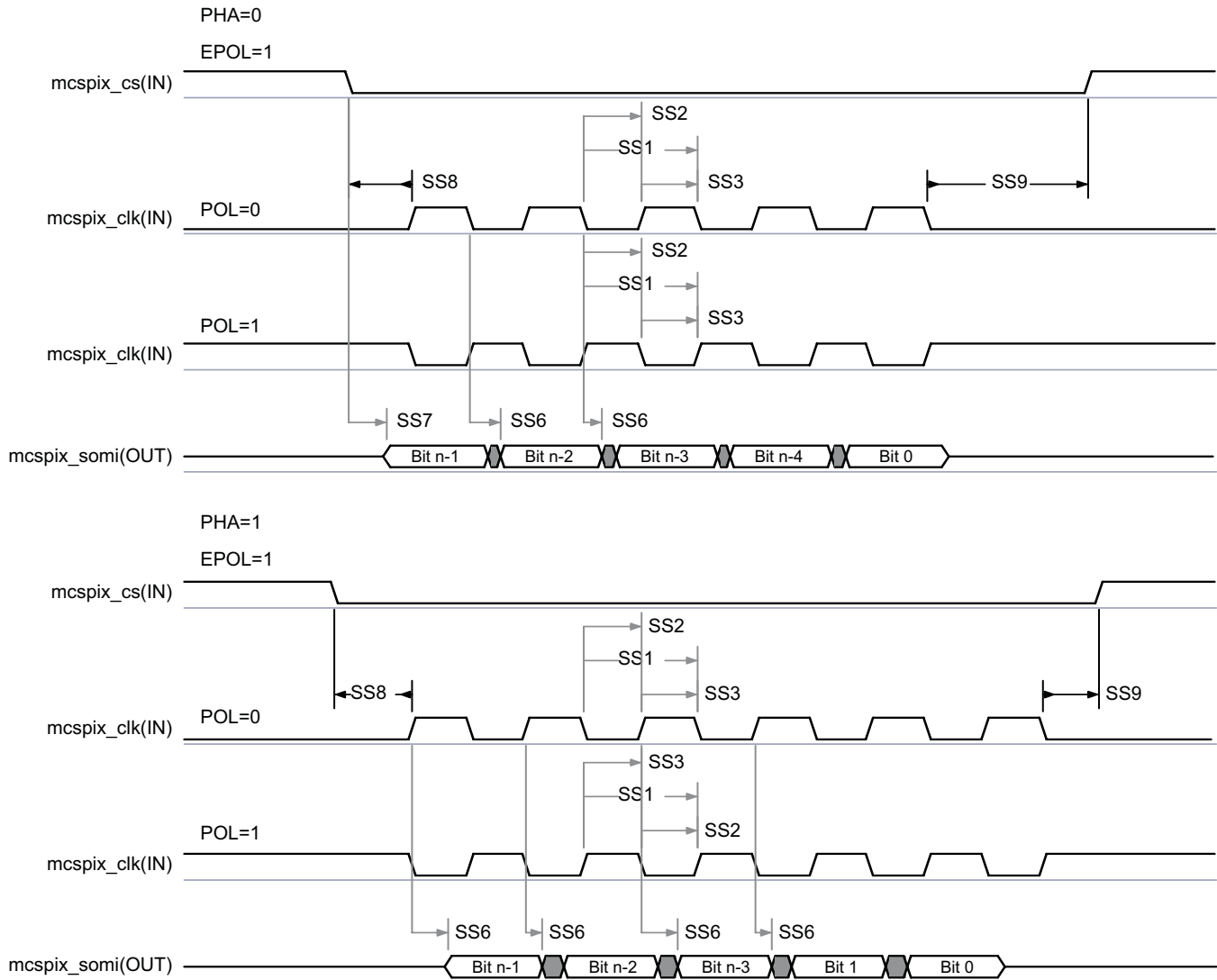
- (1) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.
- (2) mcspix_clk phase is programmable with the bit PHA, of MCSPI_CHxCONF register.
- (3) In mcspix_clk, mcspix_somi, x is equal to 3 or 4.
- (4) mcspix_cs is equal to mcspi3_cs0 or mcspi4_cs0
- (5) See [Section 4.3](#) for CORE OPP voltages.



SWPS050_McSPI_03

Figure 6-52. McSPI3 and McSPI4 – Slave Mode Receive (1)(2)(3)

- (1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_simo is driven is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.
- (2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL
- (3) In mcspix_clk, mcspix_somi, x is equal to 1 or 2
- (4) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]



SWPS050_McSPI_04

Figure 6-53. McSPI3 and McSPI4 – Slave Mode Transmit (1)(2)(3)(4)

- (1) The active clock edge selection of `mcspix_clk` (rising or falling) on which `mcspix_somi` data is latched is software configurable with the bit `MCSPi_CHxCONF[1] = POL` and the bit `MCSPi_CHxCONF[0] = PHA`.
- (2) The polarity of `mcspix_cs` is software configurable with the bit `MCSPi_CHxCONF[6] = EPOL`.
- (3) In `mcspix_clk`, `mcspix_somi`, `x` is equal to 3 or 4.
- (4) `mcspix_cs` is equal to `mcspi3_cs0` or `mcspi4_cs0`.

6.6.4 Digital Microphone (DMIC)—1.8 V

NOTE

For more information, see the Digital Microphone Controller chapter in the Device TRM.

The module consists in an audio module dedicated to mobile telephone terminal. The DMIC module allows supporting up to three pairs of digital microphones. Digital microphone generates a pulse-density modulated (PDM) stream of bits. The data are transferred from the external microphone on one half-period of the clock (DDR) provided by the DMIC module.

Table 6-63. DMIC Timing Conditions—DDR—Master/Receive Mode—1.8 V

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|-------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | | 10.00 | ns |
| t_F | Input signal fall time | | 10.00 | ns |
| Output Condition | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding Device VDDS power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-64](#) and [Table 6-65](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-64. DMIC Timing Requirements—DDR—Master/Receive Mode—1.8 V

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|-------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| DMIC4 | $t_{su(dV-clkH)}$ | Setup time, data valid before clk rising or falling edge | 56.0 | | MHz |
| DMIC5 | $t_{h(clkH-dV)}$ | Hold time, data valid after clk rising or falling edge | -0.7 | | ns |

Table 6-65. DMIC Switching Characteristics—DDR—Master/Receive Mode—1.8 V⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|------------------|---|------------------------|------|------|
| | | | MIN | MAX | |
| DMIC1 | $1 / t_{c(clk)}$ | Frequency, output abedmic_clk | | 3.84 | MHz |
| DMIC2 | $t_{w(clkL)}$ | Typical pulse duration, output abedmic_clk low | 0.5 * P ⁽¹⁾ | | ns |
| DMIC3 | $t_{w(clkH)}$ | Typical pulse duration, output abedmic_clk high | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output abedmic_clk | | 13 | ps |
| | $t_{j(clk)}$ | Jitter standard deviation ⁽²⁾ , output abedmic_clk | | 67 | ps |
| | $t_{R(clk)}$ | Rise time, output abedmic_clk | | 10 | ns |
| | $t_{F(clk)}$ | Fall time, output abedmic_clk | | 10 | ns |

- (1) P = output clk period in ns
- (2) The jitter probability density can be approximated by a Gaussian function.
- (3) See [Section 4.3](#) for CORE OPP voltages.

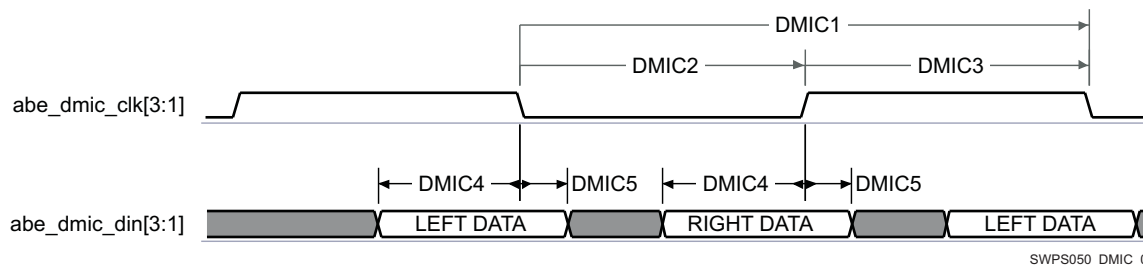


Figure 6-54. DMIC—DDR—Master/Receive Mode—1.8 V⁽¹⁾

- (1) RIGHT/LEFT DATA capturing edges depend on the TLV1310 DOS pin implementation (Data Output Select, selects the data output for the rising or falling edge of CLK). In this figure, RIGHT DATA is on rising clock edge (DOS high for right digital microphone) and LEFT DATA is on falling clock edge (DOS low for left digital microphone).

6.6.5 Multichannel Pulse Density Modulation (McPDM), 1.8 V

NOTE

For more information, see the Multichannel Pulse Density Modulation Controller chapter in the Device TRM.

Multichannel pulse density modulation interface (McPDM) is an audio module dedicated to mobile telephone terminal. It is composed of uplink and downlink paths both communicating with the audio companion chip through a dedicated interface.

Table 6-66. McPDM Timing Conditions—Master Mode—1.8 V

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 1.00 | 6.00 | ns |
| t_F | Input signal fall time | 1.00 | 6.00 | ns |
| Output Condition | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding Device VDDS power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-67](#) and [Table 6-68](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-67. McPDM Timing Requirements—Master Mode—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|------------------------------|---|---------|-------|------|
| | | | MIN | MAX | |
| | $1 / t_{c(\text{clk})}$ | Frequency, input abe_clks | | 19.20 | MHz |
| PDM6 | $t_{su(\text{ulV-clkH})}$ | Setup time, abemcpdm_ul_data valid before abemcpdm_lb_clk rising edge | 21.68 | | ns |
| PDM7 | $t_{h(\text{clkH-ulV})}$ | Hold time, abemcpdm_ul_data valid after abemcpdm_lb_clk rising edge | 0.10 | | ns |
| PDM8 | $t_{su(\text{frameV-clkH})}$ | Setup time, abemcpdm_frame valid before abemcpdm_lb_clk rising edge | 21.68 | | ns |
| PDM9 | $t_{h(\text{clkH-frameV})}$ | Hold time, abemcpdm_frame valid after abemcpdm_lb_clk rising edge | 0.10 | | ns |

(1) See [Section 4.3](#) for CORE OPP voltages.

Table 6-68. McPDM Switching Characteristics—Master Mode—1.8 V⁽³⁾⁽⁴⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|-----------------------------|--|------------------------|-------|------|
| | | | MIN | MAX | |
| PDM1 | $1 / t_{c(\text{clk})}$ | Frequency, output abemcpdm_lb_clk | | 19.20 | MHz |
| PDM2 | $t_{w(\text{clkH})}$ | Typical pulse duration, output abemcpdm_lb_clk high | 0.5 * P ⁽¹⁾ | | ns |
| PDM3 | $t_{w(\text{clkL})}$ | Typical pulse duration, output abemcpdm_lb_clk low | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output abemcpdm_lb_clk | | 2604 | ps |
| | $t_{j(\text{clk})}$ | Jitter standard deviation ⁽²⁾ , output abemcpdm_lb_clk | | 434 | ps |
| | $t_{R(\text{clk})}$ | Rise time, output abemcpdm_lb_clk | | 5 | ns |
| | $t_{F(\text{clk})}$ | Fall time, output abemcpdm_lb_clk | | 5 | ns |
| PDM4 | $t_{d(\text{clkH-dlV})}$ | Delay time, output abemcpdm_lb_clk high to output abemcpdm_dl_data valid | 1.45 | 33.03 | ns |
| PDM5 | $t_{d(\text{clkH-frameV})}$ | Delay time, output abemcpdm_lb_clk high to output abemcpdm_frame valid | 1.45 | 33.03 | ns |
| | $t_{R(\text{dl})}$ | Rise time, output abemcpdm_dl_data | | 5 | ns |
| | $t_{F(\text{dl})}$ | Fall time, output abemcpdm_dl_data | | 5 | ns |
| | $t_{R(\text{frame})}$ | Rise time, output abemcpdm_frame | | 5 | ns |

- (1) P = output clk period in ns
- (2) The jitter probability density can be approximated by a Gaussian function.
- (3) The timing requirements are assured for the Jitter standard deviation and duty cycle error conditions specified.
- (4) See [Section 4.3](#) for CORE OPP voltages.

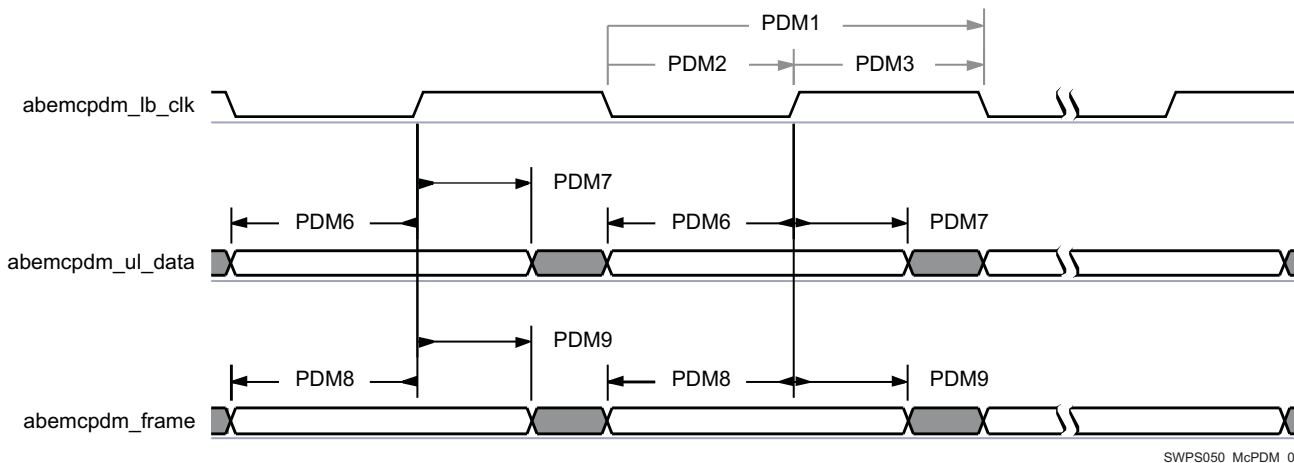


Figure 6-55. McPDM—SDR—Master Mode—Receiver—1.8 V

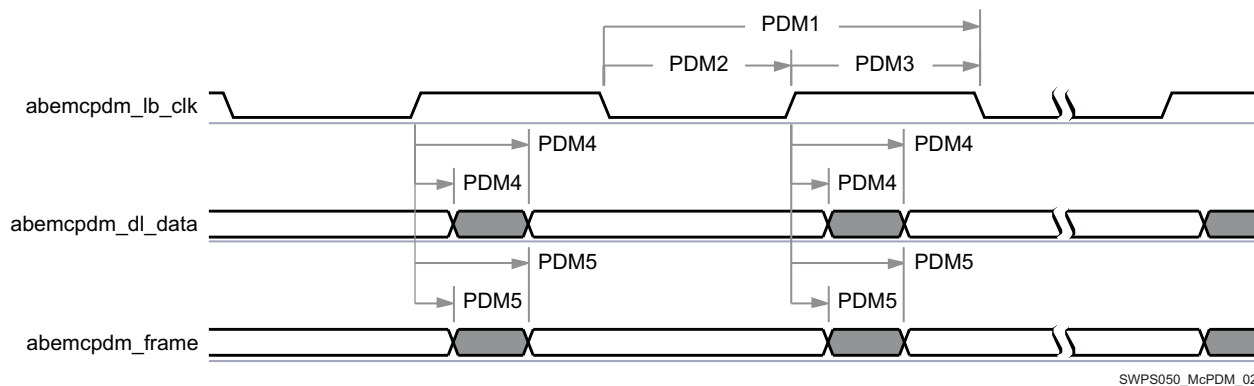


Figure 6-56. McPDM—SDR—Master Mode—Transmitter—1.8 V

6.6.6 MIPI HSI2 (High-Speed Synchronous Interface), 1.8 V

NOTE

The HSI1 interface is not available in the OMAP5432 device. For more information, see the Device TRM.

NOTE

For more information, see the MIPI HSI chapter in the Device TRM.

The HSI1 and HSI2 interfaces are compliant with the MIPI HSI protocol and typically used for communication with a modem. The HSI1 and HSI2 interfaces support maximum data rates of:

- In receive mode, 225.2 Mbps @OPP_NOM.
- In transmit mode, 192 Mbps @OPP_NOM.

Table 6-69. HSI2 Timing Conditions—1.8 V

| SYSTEM CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|-----------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input rise time | 611 | 1366 | ps |
| t_F | Input fall time | 611 | 1366 | ps |
| Output Conditions | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-70](#) and [Table 6-71](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-70. HSI2 Timing Requirements—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|---------------------|--|---------|------|------|
| | | | MIN | MAX | |
| HSI1 | $1 / t_{c(NomBit)}$ | Frequency, nominal bit | 225.2 | | MHz |
| HSI2 | $t_d(DAT-FLAG)$ | Delay time, hsi_cadata transition to hsi_caflag transition | 1.56 | | ns |
| | $t_d(FLAG-DAT)$ | Delay time, hsi_caflag transition to hsi_cadata transition | 1.56 | | ns |
| HSI3 | $t_d(DAT)$ | Duration time, hsi_cadata low level or high level duration | 4.22 | | ns |
| | $t_d(FLAG)$ | Duration time, hsi_caflag low level or high level duration | 4.22 | | ns |
| HSI4 | t_R | Rise time, hsi_cadata and hsi_caflag (20% to 80%) | 0.61 | 1.37 | ns |
| HSI5 | t_F | Fall time, hsi_cadata and hsi_caflag (80% to 20%) | 0.61 | 1.37 | ns |

(1) See [Section 4.3](#) for CORE OPP voltages.

Table 6-71. HSI2 Switching Characteristics—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|---------------------|--|---------|------|------|
| | | | MIN | MAX | |
| HSI1 | $1 / t_{c(NomBit)}$ | Frequency, nominal bit | 192 | | MHz |
| HSI6 | $t_d(DAT-FLAG)$ | Delay time, hsi_acdata transition to hsi_acflag transition | 2.08 | | ns |
| | $t_d(FLAG-DAT)$ | Delay time, hsi_acflag transition to hsi_acdata transition | 2.08 | | ns |
| HSI7 | $t_d(DAT)$ | Duration time, hsi_acdata low level or high level duration | 4.95 | | ns |
| | $t_d(FLAG)$ | Duration time, hsi_acflag low level or high level duration | 4.95 | | ns |
| HSI8 | t_R | Rise time, hsi_acdata and hsi_acflag (20% to 80%) | 1.0 | 1.84 | ns |
| HSI9 | t_F | Fall time, hsi_acdata and hsi_acflag (80% to 20%) | 1.0 | 1.84 | ns |

(1) See Section 4.3 for CORE OPP voltages.

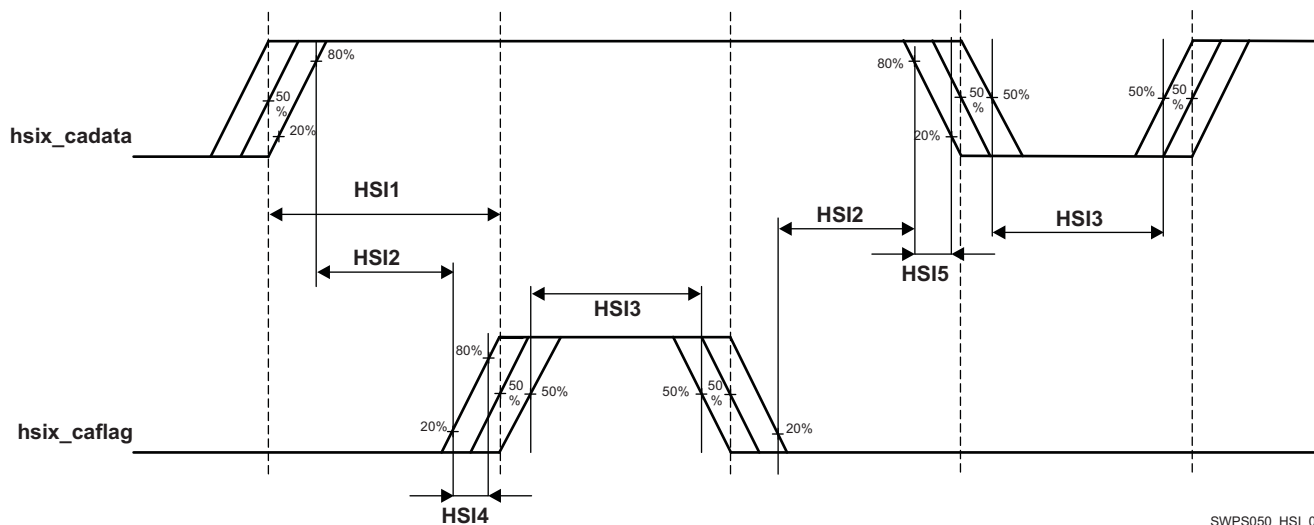


Figure 6-57. HSI2—1.8 V—Receive Mode

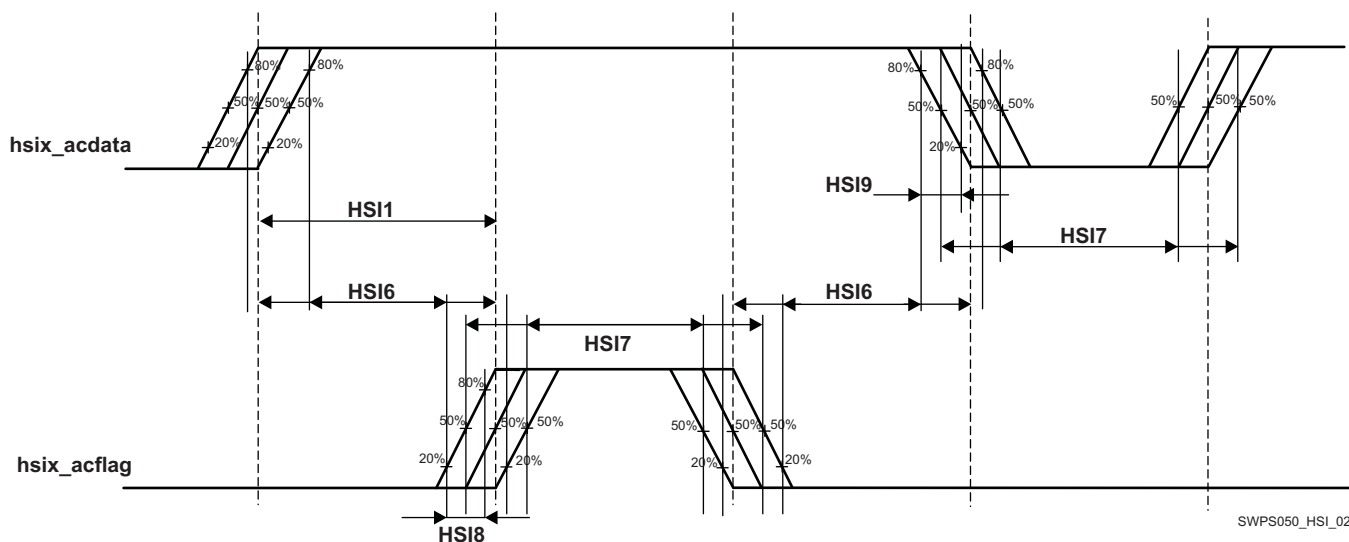


Figure 6-58. HSI 2—1.8 V—Transmit Mode

6.6.7 Universal Serial Bus (USB)

6.6.7.1 Super-Speed USB Dual-Role Device—USBD0—1.8 V and 3.3 V

NOTE

The following interfaces are not available in the OMAP5432 device:

- USB (Port D0) – ULPI 8-bit
- USB (Port B1) – HSIC1
- USB (Port B2) – ULPI 8-bit
- USB (Port B2) – Full Speed / Low Speed

For more information, see the Device TRM.

NOTE

For more information, see the Serial Communication Interface / Super-Speed USB Dual-Role Subsystem chapter in the Device TRM.

6.6.7.1.1 USBD0 DRD PHY

The USBD0 DRD interface supports the following applications:

- USB2.0 High-Speed PHY port (1.8 V and 3.3 V): this asynchronous high-speed interface is compliant with the USB2.0 PHY standard with an internal transceiver (USB2.0 standard v2.0), for a maximum data rate of 480 Mbps at OPP_NOM.
- USB3.0 Super-Speed PHY port (1.8 V): this asynchronous differential super-speed interface is compliant with the USB3.0 RX/TX PHY standard (USB3.0 standard v1.0) for a maximum data bit rate of 5Gbps at OPP_NOM.

6.6.7.1.2 USBD0 DRD ULPI—SDR—Slave Mode—12-pin Mode—1.8 V

The USBD0 DRD interface supports the following application:

- USB ULPI port (1.8 V): this synchronous interface is compliant with the USB2.0 ULPI SDR standard (UTMI+ v1.22), for alternative off-chip USB2.0 PHY interface; that is, with external transceiver with a maximum frequency of 60 MHz at OPP_NOM (synchronous slave mode, SDR, 12-pin, 8-data-bit).

Table 6-72. HS USBD0 ULPI Timing Conditions—SDR—Slave Mode—12-pin Mode—1.8 V

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t _R | Input signal rise time | 1.00 | 3.00 | ns |
| t _F | Input signal fall time | 1.00 | 3.00 | ns |
| Output Condition | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding Device VDDS power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-73](#) and [Table 6-74](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-73. HS USBD0 ULPI Timing Requirements—SDR—Slave Mode—12-pin Mode—1.8 V⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|--------------------------|--|------------------------|-----|------|
| | | | MIN | MAX | |
| US1 | 1 / t _c (clk) | Frequency, input usbd0_ulpiphy_clk | | 60 | MHz |
| US2 | t _w (clkH) | Typical pulse duration, usbd0_ulpiphy_clk high | 0.5 * P ⁽¹⁾ | | ns |
| US3 | t _w (clkL) | Typical pulse duration, usbd0_ulpiphy_clk low | 0.5 * P ⁽¹⁾ | | ns |

Table 6-73. HS USBD0 ULPI Timing Requirements—SDR—Slave Mode—12-pin Mode—1.8 V⁽³⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| | $t_{dc}(clk)$ | Duty cycle error, usbd0_ulpiphy_clk | | 833 | ps |
| | $t_{j}(clk)$ | Jitter standard deviation ⁽²⁾ , usbd0_ulpiphy_clk | | 500 | ps |
| US5 | $t_{su}(ctrlV-clkH)$ | Setup time, DIR and NXT valid before usbd0_ulpiphy_clk rising edge | 6.73 | | ns |
| US6 | $t_{h}(clkH-ctrlV)$ | Hold time, DIR and NXT valid after usbd0_ulpiphy_clk rising edge | 0.00 | | ns |
| US7 | $t_{su}(dV-clkH)$ | Setup time, Data valid before usbd0_ulpiphy_clk rising edge | 6.73 | | ns |
| US8 | $t_{h}(clkH-dV)$ | Hold time, Data valid after usbd0_ulpiphy_clk rising edge | 0.00 | | ns |

(1) P = clk period in ns

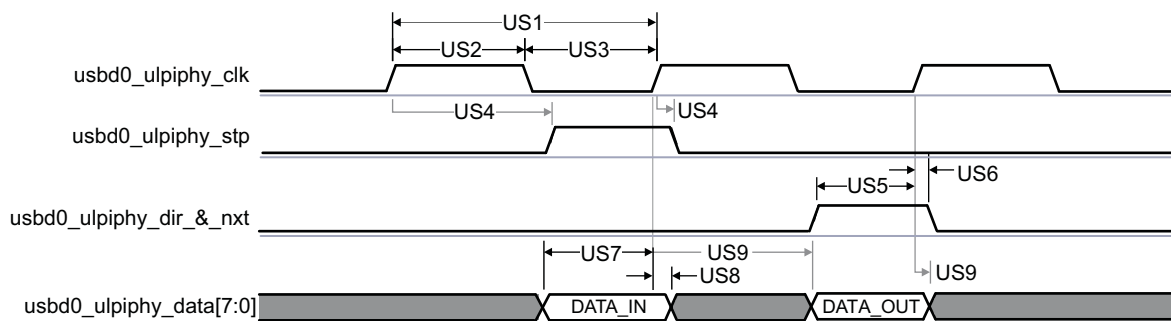
(2) Maximum cycle jitter supported by input clock.

(3) See Section 4.3 for CORE OPP voltages.

Table 6-74. HS USBD0 ULPI Switching Characteristics—SDR—Slave Mode—12-pin Mode—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|---------------------|---|---------|------|------|
| | | | MIN | MAX | |
| US4 | $t_{d}(clkL-ctrlV)$ | Delay time, output clk rising edge high to output STP valid | 0.44 | 8.35 | ns |
| | $t_{R}(ctrl)$ | Rise time, output STP | | 3.0 | ps |
| | $t_{F}(ctrl)$ | Fall time, output STP | | 3.0 | ps |
| US9 | $t_{d}(clkL-doV)$ | Delay time, output clk rising edge to output Data valid | 0.44 | 8.35 | ns |
| | $t_{R}(do)$ | Rise time, output Data | | 3.0 | ps |
| | $t_{F}(do)$ | Fall time, output Data | | 3.0 | ps |

(1) See Section 4.3 for CORE OPP voltages.



SWPS050_USB_01

Figure 6-59. HS USBD0 ULPI —SDR—Slave Mode—12-pin Mode—1.8 V

6.6.7.2 USB Host High-Speed (USB HOST HS)—USB_{B1}, 1.8 V (1.2 V for HSIC)

NOTE

For more information, see the Serial Communication Interface / High-Speed Multiport USB Host Subsystem chapter in the Device TRM.

6.6.7.2.1 HS USB_{B1} ULPI—SDR—Slave Mode—12-pin Mode—1.8 V

The USB_{B1} interface supports the following application:

- USB ULPI (1.8 V): this synchronous interface follows the USB2.0 ULPI SDR standard (UTMI+ v1.22), for USB ULPI external transceiver, with a maximum frequency of 60 MHz at OPP_NOM (synchronous slave mode, SDR, 12-pin, 8 data bits).

Table 6-75. HS USBB1 ULPI Timing Conditions—SDR—Slave Mode—12-pin Mode—1.8 V

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 1.00 | 3.00 | ns |
| t_F | Input signal fall time | 1.00 | 3.00 | ns |
| Output Condition | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-76](#) and [Table 6-77](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-76. HS USBB1 ULPI Timing Requirements—SDR—Slave Mode—12-pin Mode—1.8 V⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|-----------------------------|--|------------------------|-----|------|
| | | | MIN | MAX | |
| US1 | $1 / t_{c(\text{clk})}$ | Frequency, input usbb1_ulpiphy_clk | | 60 | MHz |
| US2 | $t_{w(\text{clkH})}$ | Typical pulse duration, usbb1_ulpiphy_clk high | 0.5 * P ⁽¹⁾ | | ns |
| US3 | $t_{w(\text{clkL})}$ | Typical pulse duration, usbb1_ulpiphy_clk low | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, usbb1_ulpiphy_clk | | 833 | ps |
| | $t_j(\text{clk})$ | Jitter standard deviation ⁽²⁾ , usbb1_ulpiphy_clk | | 500 | ps |
| US5 | $t_{su(\text{ctrlV-clkH})}$ | Setup time, DIR and NXT valid before usbb1_ulpiphy_clk rising edge | 6.73 | | ns |
| US6 | $t_{h(\text{clkH-clkV})}$ | Hold time, DIR and NXT valid after usbb1_ulpiphy_clk rising edge | 0 | | ns |
| US7 | $t_{su(\text{dV-clkH})}$ | Setup time, data valid before usbb1_ulpiphy_clk rising edge | 6.73 | | ns |
| US8 | $t_{h(\text{clkH-dV})}$ | Hold time, data valid after usbb1_ulpiphy_clk rising edge | 0 | | ns |

(1) P = clk period in ns

(2) Maximum cycle jitter supported by input clock.

(3) See [Section 4.3](#) for CORE OPP voltages.

Table 6-77. HS USBB1 ULPI Switching Characteristics—SDR—Slave Mode—12-pin Mode—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|---------------------------|---|---------|------|------|
| | | | MIN | MAX | |
| US4 | $t_{d(\text{clkL-clkV})}$ | Delay time, output clk rising edge high to output STP valid | 0.44 | 8.35 | ns |
| | $t_{R(\text{ctrl})}$ | Rise time, output STP | | 3.0 | ps |
| | $t_{F(\text{ctrl})}$ | Fall time, output STP | | 3.0 | ps |
| US9 | $t_{d(\text{clkL-doV})}$ | Delay time, output clk rising edge to output data valid | 0.44 | 8.35 | ns |
| | $t_{R(\text{do})}$ | Rise time, output data | | 3.0 | ps |
| | $t_{F(\text{do})}$ | Fall time, output data | | 3.0 | ps |

(1) See Section 4.3 for CORE OPP voltages.

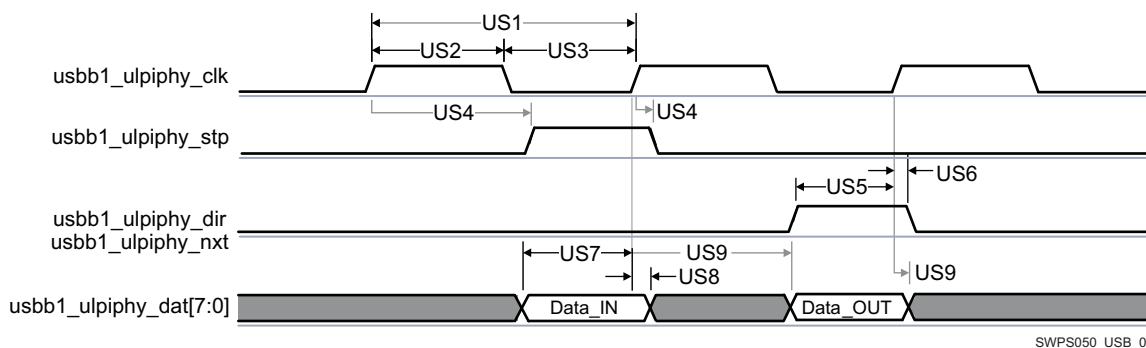


Figure 6-60. HS USBB1 ULPI —SDR—Slave Mode—12-pin Mode—1.8 V

6.6.7.2.2 HS USBB1 HSIC—DDR—2-pin Mode—1.2 V

The USBB1 interface supports the following application:

- USB HSIC (high-speed interchip) (1.2 V): this synchronous application for USB chip-to-chip interconnect (without transceiver) supports a maximum data rate of 480Mbps (240 MHz) at OPP_NOM (synchronous, DDR, 2-pin, data/strobe).

Table 6-78. HS USBB1 HSIC Timing Conditions—DDR—2-pin Mode—1.2 V

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | | 0.60 | ns |
| t_F | Input signal fall time | | 0.60 | ns |
| Output Condition | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

Table 6-79 and Table 6-80 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-79. HS USBB1 HSIC Timing Requirements—DDR—2-pin Mode—1.2 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|-------------------------------|--|------------------------|------|------|
| | | | MIN | MAX | |
| HSIC1 | $1 / t_{c(\text{clki})}$ | Frequency, input usbb1_hsic_strobe | | 240 | MHz |
| HSIC2 | $t_{w(\text{clkiH})}$ | Typical pulse duration, usbb1_hsic_strobe high | 0.5 * P ⁽¹⁾ | | ns |
| HSIC3 | $t_{w(\text{clkiL})}$ | Typical pulse duration, usbb1_hsic_strobe low | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{R(\text{clki})}$ | Rise time, usbb1_hsic_strobe (30% to 70%) | | 0.60 | ns |
| | $t_{F(\text{clki})}$ | Fall time, usbb1_hsic_strobe (70% to 30%) | | 0.60 | ns |
| | $t_{R(\text{di})}$ | Rise time, input data usbb1_hsic_data (30% to 70%) | | 0.60 | ns |
| | $t_{F(\text{di})}$ | Fall time, input data usbb1_hsic_data (70% to 30%) | | 0.60 | ns |
| HSIC5 | $t_{su(\text{strobe-dataV})}$ | Setup time, usbb1_hsic_data valid before usbb1_hsic_strobe low or high | 0.301 | | ns |
| HSIC6 | $t_h(\text{strobe-dataV})$ | Hold time, usbb1_hsic_data valid after usbb1_hsic_strobe low or high | 0.301 | | ns |

- (1) P = usbb1_hsic_strobe period in ns
- (2) See Section 4.3 for CORE OPP voltages.

Table 6-80. HS USBB1 HSIC Switching Characteristics—DDR—2-pin Mode—1.2 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|---------------------------|--|-----------------|-------|------|
| | | | MIN | MAX | |
| HSIC1 | $1 / t_{C(\text{clko})}$ | Frequency, output usbb1_hsic_strobe | | 240 | MHz |
| HSIC2 | $t_{w(\text{clkoH})}$ | Typical pulse duration, usbb1_hsic_strobe high | $0.5 * P^{(1)}$ | | ns |
| HSIC3 | $t_{w(\text{clkoL})}$ | Typical pulse duration, usbb1_hsic_strobe low | $0.5 * P^{(1)}$ | | ns |
| | $t_{dc(\text{clko})}$ | Duty cycle error, usbb1_hsic_strobe | | 83 | ps |
| | $t_{R(\text{clko})}$ | Slew rate rise, usbb1_hsic_strobe | 0.65 | 1.60 | V/ns |
| | $t_{F(\text{clko})}$ | Slew rate fall, usbb1_hsic_strobe | 0.65 | 1.60 | V/ns |
| HSIC4 | $t_{d(\text{clk-dataV})}$ | Delay time, usbb1_hsic_strobe low or high to usbb1_hsic_data valid | -0.422 | 0.422 | ns |
| | $t_{R(\text{do})}$ | Slew rate rise, output data usbb1_hsic_data | 0.65 | 1.60 | V/ns |
| | $t_{F(\text{do})}$ | Slew rate fall, output data usbb1_hsic_data | 0.65 | 1.60 | V/ns |

- (1) P = usbb1_hsic_strobe period in ns
- (2) See Section 4.3 for CORE OPP voltages.

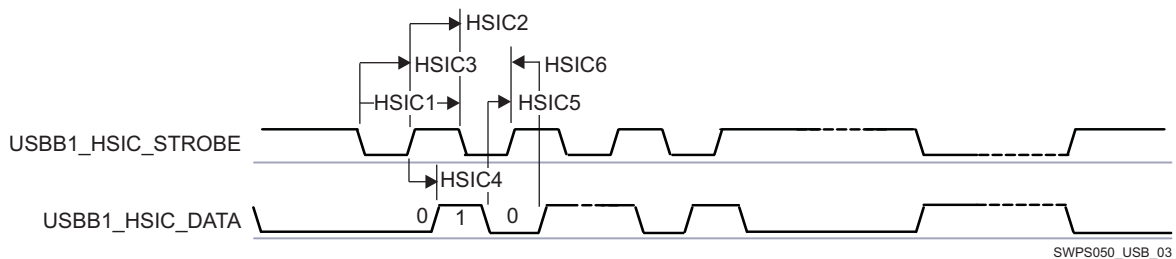


Figure 6-61. HS USBB1 HSIC —DDR—2-pin Mode—1.2 V

6.6.7.3 USB Host High-Speed (USB HOST HS)—USB2, 1.8 V (1.2 V for HSIC)

NOTE

For more information, see the Serial Communication Interface / High-Speed Multiport USB Host Subsystem chapter in the Device TRM.

6.6.7.3.1 HS USBB2 ULPI TLL—SDR—Master Mode —12-pin Mode—1.8 V

The USBB2 interface supports the following application:

- USB ULPI TLL (1.8 V): this synchronous application for USB ULPI device without transceiver (TLL: transceiverless link), with a maximum frequency of 60 MHz at OPP_NOM (synchronous master mode, SDR, 12-pin, 8-data-bit).

Table 6-81. HS USBB2 ULPI TLL Timing Conditions —SDR—Master Mode—12-pin Mode—1.8 V

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 1.00 | 3.00 | ns |
| t_F | Input signal fall time | 1.00 | 3.00 | ns |
| Output Condition | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-82](#) and [Table 6-83](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-82. HS USBB2 ULPI TLL Timing Requirements—SDR—Master Mode—12-pin Mode—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|----------------------|---|---------|-----|------|
| | | | MIN | MAX | |
| UT4 | $t_{su(ctrIV-clkH)}$ | Setup time, STP valid before usbb2_ulpitll_clk rising edge | 5.86 | | ns |
| UT5 | $t_{h(clkH-ctrIV)}$ | Hold time, STP valid after usbb2_ulpitll_clk rising edge | 0.02 | | ns |
| UT6 | $t_{su(dV-clkH)}$ | Setup time, data valid before usbb2_ulpitll_clk rising edge | 5.86 | | ns |
| UT7 | $t_{h(clkH-dV)}$ | Hold time, data valid after usbb2_ulpitll_clk rising edge | 0.02 | | ns |

(1) See [Section 4.3](#) for CORE OPP voltages.

Table 6-83. HS USBB2 ULPI TLL Switching Characteristics—SDR—Master Mode—12-pin Mode—1.8 V⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|--------------------------|---|-----------------|------|------|
| | | | MIN | MAX | |
| UT1 | $1 / t_c(\text{clk})$ | Frequency, usbb2_ulpitll_clk | | 60 | MHz |
| UT2 | $t_w(\text{clkH})$ | Typical pulse duration, usbb2_ulpitll_clk high | $0.5 * P^{(1)}$ | | ns |
| UT3 | $t_w(\text{clkL})$ | Typical pulse duration, usbb2_ulpitll_clk low | $0.5 * P^{(1)}$ | | ns |
| | $t_{dc}(\text{clk})$ | Duty cycle error, usbb2_ulpitll_clk | | 833 | ps |
| | $t_j(\text{clk})$ | Jitter standard deviation ⁽²⁾ , usbb2_ulpitll_clk | | 400 | ps |
| | $t_R(\text{clk})$ | Rise time, usbb2_ulpitll_clk | | 3.0 | ps |
| | $t_F(\text{clk})$ | Fall time, usbb2_ulpitll_clk | | 3.0 | ps |
| UT8 | $t_d(\text{clkL-ctrIV})$ | Delay time, usbb2_ulpitll_clk rising edge to output DIR and NXT valid | 0.04 | 9.12 | ns |
| | $t_R(\text{ctrl})$ | Rise time, output DIR and NXT | | 3.0 | ps |
| | $t_F(\text{ctrl})$ | Fall time, output DIR and NXT | | 3.0 | ps |
| UT9 | $t_d(\text{clkL-doV})$ | Delay time, usbb2_ulpitll_clk rising edge to output data valid | 0.04 | 9.12 | ns |
| | $t_R(\text{do})$ | Rise time, output data | | 3.0 | ps |
| | $t_F(\text{do})$ | Fall time, output data | | 3.0 | ps |

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See [Section 4.3](#) for CORE OPP voltages.

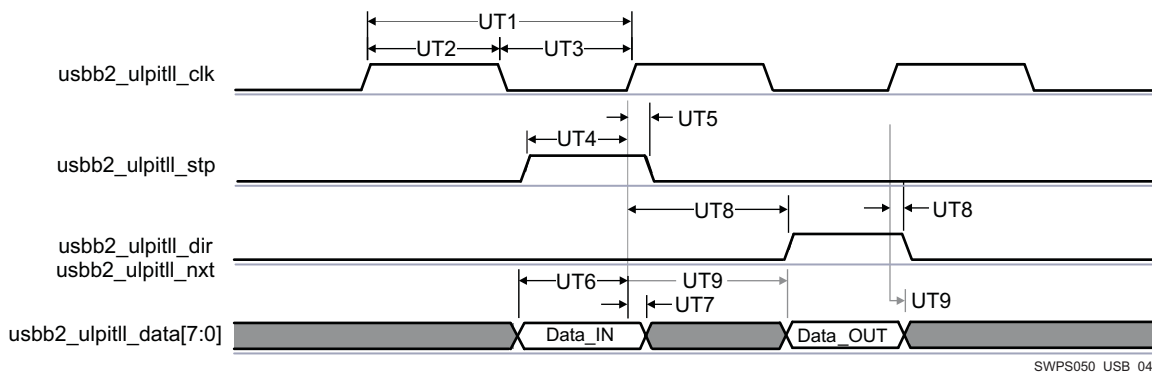


Figure 6-62. HS USBB2 ULPI TLL—SDR—Master Mode—12-pin Mode—1.8 V

6.6.7.3.2 HS USBB2 HSIC—DDR—2-pin Mode—1.2 V

The USBB2 interface supports the following application:

- USB HSIC (1.2 V): this synchronous application for USB chip-to-chip interconnect (without transceiver) supports a maximum data rate of 480Mbps (240 MHz) at OPP_NOM (synchronous, DDR, 2-pin, data/strobe)

Table 6-84. HS USBB2 HSIC Timing Conditions—DDR—2-pin Mode—1.2 V

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|-----|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | | 0.6 | ns |
| t_F | Input signal fall time | | 0.6 | ns |
| Output Condition | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding Device VDDS power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-85](#) and [Table 6-86](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-85. HS USBB2 HSIC Timing Requirements—DDR—2-pin Mode—1.2 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|-------------------------------|--|------------------------|-----|------|
| | | | MIN | MAX | |
| HSIC1 | $1 / t_{C(\text{clki})}$ | Frequency, input usbb2_hsic_strobe | | 240 | MHz |
| HSIC2 | $t_{W(\text{clkIH})}$ | Typical pulse duration, usbb2_hsic_strobe high | 0.5 * P ⁽¹⁾ | | ns |
| HSIC3 | $t_{W(\text{clkIL})}$ | Typical pulse duration, usbb2_hsic_strobe low | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{R(\text{clki})}$ | Rise time, usbb2_hsic_strobe (30% to 70%) | | 0.6 | ns |
| | $t_{F(\text{clki})}$ | Fall time, usbb2_hsic_strobe (70% to 30%) | | 0.6 | ns |
| | $t_{R(\text{di})}$ | Rise time, input usbb2_data_hsic_data (30% to 70%) | | 0.6 | ns |
| | $t_{F(\text{di})}$ | Fall time, input data usbb2_hsic_data (70% to 30%) | | 0.6 | ns |
| HSIC5 | $t_{su(\text{strobe-dataV})}$ | Setup time, usbb2_hsic_data valid before usbb2_hsic_strobe low or high | 0.301 | | ns |
| HSIC6 | $t_{h(\text{strobe-dataV})}$ | Hold time, usbb2_hsic_data valid after usbb2_hsic_strobe low or high | 0.301 | | ns |

(1) P = usbb2_hsic_strobe period in ns

(2) See [Section 4.3](#) for CORE OPP voltages.

Table 6-86. HS USBB2 HSIC Switching Characteristics—DDR—2-pin Mode—1.2 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|---------------------------|--|------------------------|-------|------|
| | | | MIN | MAX | |
| HSIC1 | $1 / t_{C(\text{clkO})}$ | Frequency, output usbb2_hsic_strobe | | 240 | MHz |
| HSIC2 | $t_{W(\text{clkOH})}$ | Typical pulse duration, usbb2_hsic_strobe high | 0.5 * P ⁽¹⁾ | | ns |
| HSIC3 | $t_{W(\text{clkOL})}$ | Typical pulse duration, usbb2_hsic_strobe low | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{dc(\text{clkO})}$ | Duty cycle error, usbb2_hsic_strobe | | 83 | ps |
| | $t_{R(\text{clkO})}$ | Slew rate rise, usbb2_hsic_strobe | 0.65 | 1.6 | V/ns |
| | $t_{F(\text{clkO})}$ | Slew rate fall, usbb2_hsic_strobe | 0.65 | 1.6 | V/ns |
| HSIC4 | $t_{d(\text{clk-dataV})}$ | Delay time, usbb2_hsic_strobe low or high to usbb2_hsic_data valid | -0.422 | 0.422 | ns |
| | $t_{R(\text{do})}$ | Slew rate rise, output data usbb2_hsic_data | 0.65 | 1.6 | V/ns |
| | $t_{F(\text{do})}$ | Slew rate fall, output data usbb2_hsic_data | 0.65 | 1.6 | V/ns |

- (1) P = usbb2_hsic_strobe period in ns
- (2) See Section 4.3 for CORE OPP voltages.

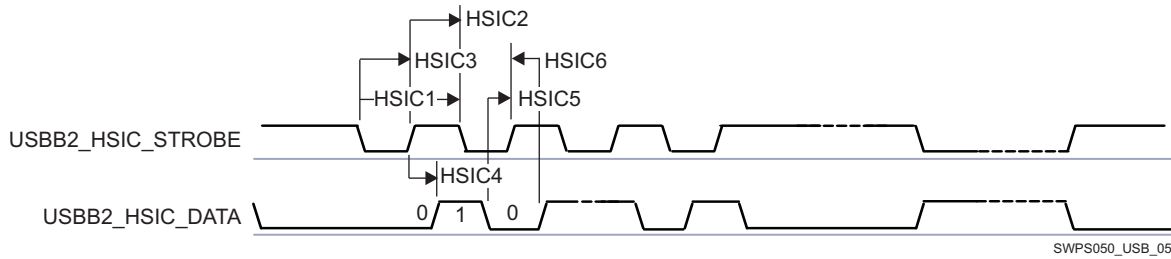


Figure 6-63. HS USB2 HSIC —DDR—2-pin Mode—1.2 V

6.6.7.3.3 Low- and Full-Speed USB2

The USB2 interface supports the low-speed and full-speed standard (1.8 V) for USB TLL peripheral applications with maximum data rate of 1.5Mbps (LS) and 12Mbps (FS).

6.6.7.3.3.1 Low- and Full-Speed USB2—Unidirectional TLL 2-pin Mode—1.8 V

Table 6-87. Low- and Full-Speed USB2 Timing Conditions—Unidirectional TLL 2-pin Mode—1.8 V

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|----------------------------|------------------------|-------|------|
| Input Conditions | | | |
| t _R | Input signal rise time | 2 | ns |
| t _F | Input signal fall time | 2 | ns |
| Output Condition | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

Table 6-88 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-88. Low- and Full-Speed USB2 Timing Requirements—Unidirectional TLL 2-pin Mode—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|-----------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| FSU1 | t _{d(Vp,Vm)} | Time duration, usbb2_mm_rxdp and usbb2_mm_rxdm low together during transition | | 14 | ns |
| FSU2 | t _{d(Vp,Vm)} | Time duration, usbb2_mm_rxdp and usbb2_mm_rxdm high together during transition | | 8 | ns |

(1) See Section 4.3 for CORE OPP voltages.



Figure 6-64. Low- and Full-Speed USB—Unidirectional TLL 2-pin Mode—1.8 V

6.6.7.3.3.2 Low- and Full-Speed USB2—Bidirectional TLL 3-pin Mode—1.8 V

Table 6-89. Low/Full-Speed USB2 Timing Conditions—Bidirectional TLL 3-pin Mode—1.8 V

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|----------------------------|--|-------|------|
| Input Conditions | | | |

Table 6-89. Low/Full-Speed USB2 Timing Conditions—Bidirectional TLL 3-pin Mode—1.8 V (continued)

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|----------------------------|------------------------|-------|------|
| t_R | Input signal rise time | 2 | ns |
| t_F | Input signal fall time | 2 | ns |
| Output Condition | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding Device VDDS power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

Table 6-90 and Table 6-91 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-90. Low- and Full-Speed USB2 Timing Requirements—Bidirectional TLL 3-pin Mode—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|--------|------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| FSUT17 | $t_{d(DAT,SE0)}$ | Time duration, usbb2_mm_txdat and usbb2_mm_txse0 low together during transition | | 14 | ns |
| FSUT18 | $t_{d(DAT,SE0)}$ | Time duration, usbb2_mm_txdat and usbb2_mm_txse0 high together during transition | | 8 | ns |

(1) See Section 4.3 for CORE OPP voltages.

Table 6-91. Low- and Full-Speed USB2 Switching Characteristics—Bidirectional TLL 3-pin Mode—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|--------|---------------------|---|---------|------|------|
| | | | MIN | MAX | |
| FSUT19 | $t_{d(TXENH-DATV)}$ | Delay time usbb2_mm_txen high to usbb2_mm_txdat valid | 81.8 | 84.8 | ns |
| FSUT20 | $t_{d(TXENH-SE0V)}$ | Delay time usbb2_mm_txen high to usbb2_mm_txse0 valid | 81.8 | 84.8 | ns |
| FSUT21 | $t_{s(DAT-SE0)}$ | Skew between usbb2_mm_txdat and usbb2_mm_txse0 transition | | 1.5 | ns |
| FSUT22 | $t_{d(DATI-TXENL)}$ | Delay time usbb2_mm_txdat invalid usbb2_mm_txen low | 81.8 | | ns |
| FSUT23 | $t_{d(SE0I-TXENL)}$ | Delay time usbb2_mm_txse0 invalid usbb2_mm_txen low | 81.8 | | ns |

(1) See Section 4.3 for CORE OPP voltages.

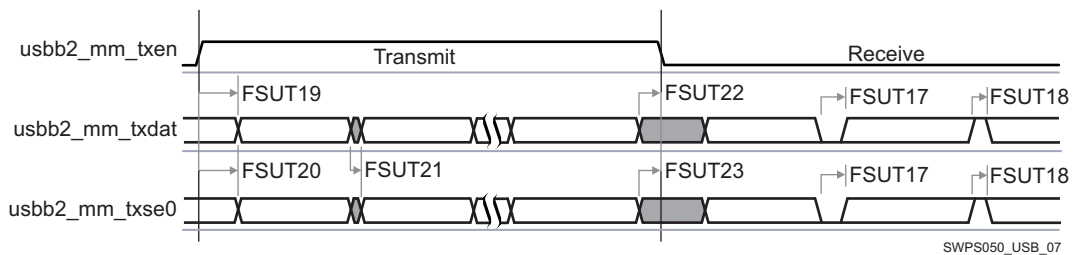


Figure 6-65. Low- and Full-Speed USB—Bidirectional TLL 3-pin Mode—1.8 V

6.6.7.3.3.3 Low- and Full-Speed USB2—Bidirectional TLL 4-pin Mode—1.8 V

Table 6-92. Low- and Full-Speed USB2 Timing Conditions—Bidirectional TLL 4-pin Mode—1.8 V

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|----------------------------|------------------------|-------|------|
| Input Conditions | | | |
| t_R | Input signal rise time | 2 | ns |
| t_F | Input signal fall time | 2 | ns |
| Output Condition | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDD5. For more information on the corresponding Device VDD5 power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-93](#) and [Table 6-94](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-93. Low- and Full-Speed USB2 Timing Requirements—Bidirectional TLL 4-pin Mode—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|--------|------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| FSUT9 | $t_{d(DAT,SE0)}$ | Time duration, usbb2_mm_txdat and usbb2_mm_txse0 low together during transition | | 14 | ns |
| FSUT10 | $t_{d(DAT,SE0)}$ | Time duration, usbb2_mm_tsdat and usbb2_mm_txse0 high together during transition | | 8 | ns |

(1) See [Section 4.3](#) for CORE OPP voltages.

Table 6-94. Low- and Full-Speed USB2 Switching Characteristics—Bidirectional TLL 4-pin Mode—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|--------|---------------------|---|---------|------|------|
| | | | MIN | MAX | |
| FSUT11 | $t_{d(TXENL-DATV)}$ | Delay time usbb2_mm_txen active to usbb2_mm_txdat valid | 81.8 | 84.8 | ns |
| FSUT12 | $t_{d(TXENL-SE0V)}$ | Delay time usbb2_mm_txen active to usbb2_mm_txse0 valid | 81.8 | 84.8 | ns |
| FSUT13 | $t_{s(DAT-SE0)}$ | Skew between usbb2_mm_txdat and usbb2_mm_txse0 transition | | 1.5 | ns |
| FSUT14 | $t_{s(DP,DM-RCV)}$ | Skew between usbb2_mm_ and usbb2_mm_rxrcv transition | | 1.5 | ns |
| FSUT15 | $t_{d(DATI-TXENL)}$ | Delay time usbb2_mm_txse0 invalid to usbb2_mm_txen low | 81.8 | | ns |
| FSUT16 | $t_{d(SE0I-TXENL)}$ | Delay time usbb2_mm_txdat invalid to usbb2_mm_txen low | 81.8 | | ns |

(1) See [Section 4.3](#) for CORE OPP voltages.

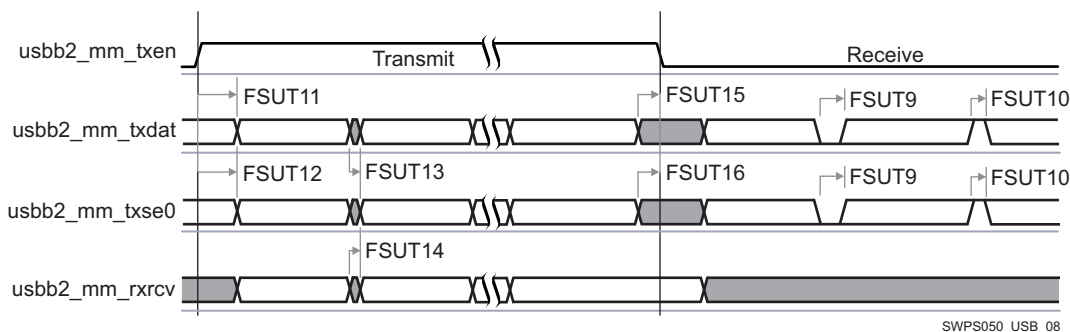


Figure 6-66. Low- and Full-Speed USB—Bidirectional TLL 4-pin Mode—1.8 V

6.6.7.3.3.4 Low- and Full-Speed USB2—Unidirectional TLL 6-pin Mode—1.8 V

Table 6-95. Low- and Full-Speed USB2 Timing Conditions—Unidirectional TLL 6-pin Mode—1.8 V

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|----------------------------|------------------------|-------|------|
| Input Conditions | | | |
| t_R | Input signal rise time | 2 | ns |
| t_F | Input signal fall time | 2 | ns |
| Output Condition | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding Device VDDS power supply name, see Table 3-1, POWER NAME [9] column with the ball name.

Table 6-96 and Table 6-97 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-96. Low- and Full-Speed USB2 Timing Requirements—Unidirectional TLL 6-pin Mode—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| FSUT1 | $t_{d(SE0,DAT)}$ | Time duration, usbb2_mm_txse0 and usbb2_mm_txdat low together during transition | | 14 | ns |
| FSUT2 | $t_{d(SE0,DAT)}$ | Time duration, usbb2_mm_txse0 and usbb2_mm_txdat high together during transition | | 8 | ns |

(1) See Section 4.3 for CORE OPP voltages.

Table 6-97. Low- and Full-Speed USB2 Switching Characteristics—Unidirectional TLL 6-pin Mode—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|--------------------|---|---------|------|------|
| | | | MIN | MAX | |
| FSUT3 | $t_{d(TXENH-DPV)}$ | Delay time usbb2_mm_txen high to usbb2_mm_rxdp valid | 81.8 | 84.8 | ns |
| FSUT4 | $t_{d(TXENH-DMV)}$ | Delay time usbb2_mm_txen high to usbb2_mm_rxdm valid | 81.8 | 84.8 | ns |
| FSUT5 | $t_{d(DPI-TXENL)}$ | Delay time usbb2_mm_rxdp invalid usbb2_mm_txen low | 81.8 | | ns |
| FSUT6 | $t_{d(DMI-TXENL)}$ | Delay time usbb2_mm_rxdm invalid usbb2_mm_txen low | 81.8 | | ns |
| FSUT7 | $t_{s(DP-DM)}$ | Skew between usbb2_mm_rxdp and usbb2_mm_rxdm transition | | 1.5 | ns |
| FSUT8 | $t_{s(DP,DM-RCV)}$ | Skew between usbb2_mm_rxdp, usbb2_mm_rxdm and mmx_rxcv transition | | 1.5 | ns |

(1) See Section 4.3 for CORE OPP voltages.

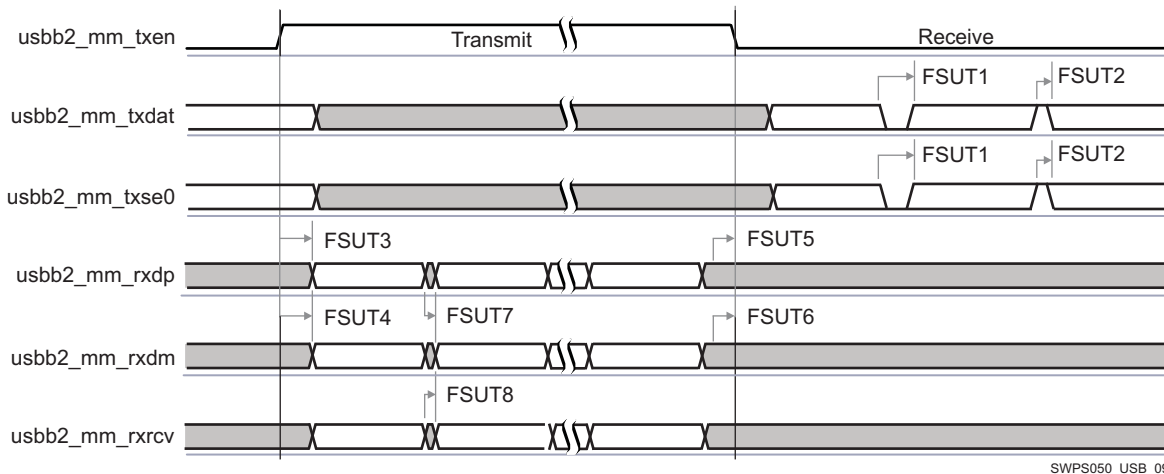


Figure 6-67. Low- and Full-Speed USB—Unidirectional TLL 6-pin Mode—1.8 V

6.6.7.4 USB Host High-Speed (USB HOST HS)—USBB3, HSIC 1.2 V

NOTE

For more information, see the Serial Communication Interface / High-Speed Multiport USB Host Subsystem chapter in the Device TRM.

6.6.7.4.1 HS USBB3 HSIC—2-pin Mode—1.2 V

The USBB3 interface supports the following application:

- USB HSIC (1.2 V): this synchronous application for USB chip-to-chip interconnect (without transceiver) supports a maximum data rate of 480Mbps (240 MHz) at OPP_NOM (synchronous, DDR, 2-pin, data/strobe).

Table 6-98. HS USBB3 HSIC Timing Conditions—DDR—2-pin Mode—1.2 V

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|------|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | | 0.60 | ns |
| t_F | Input signal fall time | | 0.60 | ns |
| Output Condition | | | | |

(1) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding Device VDDS power supply name, see [Table 3-1](#), POWER NAME [9] column with the ball name.

[Table 6-99](#) and [Table 6-100](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-99. HS USBB3 HSIC Timing Requirements—DDR—2-pin Mode—1.2 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|-------------------------------|--|------------------------|------|------|
| | | | MIN | MAX | |
| HSIC1 | $1 / t_{c(\text{clki})}$ | Frequency, input usbb3_hsic_strobe | | 240 | MHz |
| HSIC2 | $t_{w(\text{clkiH})}$ | Typical pulse duration, usbb3_hsic_strobe high | 0.5 * P ⁽¹⁾ | | ns |
| HSIC3 | $t_{w(\text{clkiL})}$ | Typical pulse duration, usbb3_hsic_strobe low | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{R(\text{clki})}$ | Rise time, usbb3_hsic_strobe (30% to 70%) | | 0.60 | ns |
| | $t_{F(\text{clki})}$ | Fall time, usbb3_hsic_strobe (70% to 30%) | | 0.60 | ns |
| | $t_{R(\text{di})}$ | Rise time, input usbb3_data_hsic_data (30% to 70%) | | 0.60 | ns |
| | $t_{F(\text{di})}$ | Fall time, input data usbb3_hsic_data (70% to 30%) | | 0.60 | ns |
| HSIC5 | $t_{su(\text{strobe-dataV})}$ | Setup time, usbb3_hsic_data valid before usbb3_hsic_strobe low or high | 0.301 | | ns |
| HSIC6 | $t_{h(\text{strobe-dataV})}$ | Hold time, usbb3_hsic_data valid after usbb3_hsic_strobe low or high | 0.301 | | ns |

(1) P = usbb3_hsic_strobe period in ns

(2) See [Section 4.3](#) for CORE OPP voltages.

Table 6-100. HS USBB3 HSIC Switching Characteristics—DDR—2-pin Mode—1.2 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|--------------------------|--|------------------------|-----|------|
| | | | MIN | MAX | |
| HSIC1 | $1 / t_{c(\text{clko})}$ | Frequency, output usbb3_hsic_strobe | | 240 | MHz |
| HSIC2 | $t_{w(\text{clkoH})}$ | Typical pulse duration, usbb3_hsic_strobe high | 0.5 * P ⁽¹⁾ | | ns |
| HSIC3 | $t_{w(\text{clkoL})}$ | Typical pulse duration, usbb3_hsic_strobe low | 0.5 * P ⁽¹⁾ | | ns |
| | $t_{dc(\text{clko})}$ | Duty cycle error, usbb3_hsic_strobe | | 83 | ps |
| | $t_{R(\text{clko})}$ | Slew Rate rise, usbb3_hsic_strobe | 0.65 | 1.6 | V/ns |
| | $t_{F(\text{clko})}$ | Slew rate fall, usbb3_hsic_strobe | 0.65 | 1.6 | V/ns |

Table 6-100. HS USBB3 HSIC Switching Characteristics—DDR—2-pin Mode—1.2 V⁽²⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|---------------------------|--|---------|-------|------|
| | | | MIN | MAX | |
| HSIC4 | $t_{d(\text{clk-dataV})}$ | Delay time, usbb3_hsic_strobe low or high to usbb3_hsic_data valid | -0.422 | 0.422 | ns |
| | $t_{R(\text{do})}$ | Slew Rate rise, output data usbb3_hsic_data | 0.65 | 1.6 | V/ns |
| | $t_{F(\text{do})}$ | Slew Rate fall, output data usbb3_hsic_data | 0.65 | 1.6 | V/ns |

(1) P = usbb3_hsic_strobe period in ns

(2) See Section 4.3 for CORE OPP voltages.

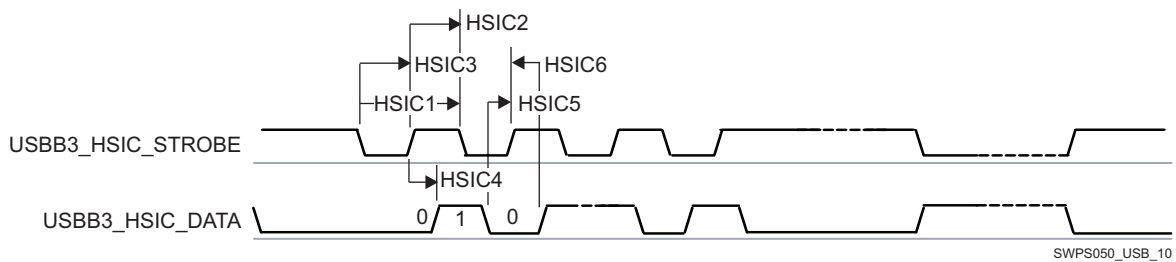


Figure 6-68. HS USBB3 HSIC —DDR—2-pin mode—1.2 V

6.6.8 Inter-Integrated Circuit Interface (I²C), 1.8 V

NOTE

For more information, see the Serial Communication Interface / Multimaster High-Speed I²C Controller / HS I²C Functional Description section of the Device TRM.

The I²C interface is compliant with the I²C standard version 2.1.

6.6.9 HDQ / 1-Wire Interface (HDQ/1-Wire), 1.8 V

NOTE

For more information, see the Serial Communication Interface / HDQ1W section of the Device TRM.

The HDQ / 1-Wire interface is intended to work with both HDQ and 1-Wire protocols. The protocols use a single wire to communicate between the master (HDQ1W controller) and the slaves (HDQ/1-Wire external compliant devices). The HDQ/1-Wire typical application is the communication with battery monitor (gas gauge) integrated devices.

6.6.9.1 HDQ Mode

Table 6-101 through Table 6-103 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-101. HDQ Timing Requirements⁽³⁾

| PARAMETER | | OPP_NOM | | UNIT |
|-------------------|--|-------------------|--------------------|------|
| | | MIN | MAX | |
| t _{CYCH} | Read bit window timing | 190 | 250 | μs |
| t _{HW1} | Read one data valid after HDQ low | 32 ⁽²⁾ | 66 ⁽²⁾ | |
| t _{HW0} | Read zero data hold after HDQ low | 70 ⁽²⁾ | 145 ⁽²⁾ | |
| t _{RSPS} | Response time from HDQ slave device ⁽¹⁾ | 190 | 320 | |

(1) Defined by software.

(2) If HDQ slave device drives a logic-low state after t_{HW0} max, it can be interpreted as a break pulse. For more information see Table 6-103 below and the HDQ1W section of the Device TRM.

(3) See Section 4.3 for CORE OPP voltages.

Table 6-102. HDQ Sampling Cases⁽¹⁾

| CASE | FIRST SAMPLING (at 68 μs) | SECOND SAMPLING (at 180 μs) |
|------|---------------------------|-----------------------------|
| 1 | L (logic-low state) | L (logic-low state) |
| 2 | L (logic-low state) | H (logic-high state) |
| 3 | H (logic-high state) | L (logic-low state) |
| 4 | H (logic-high state) | H (logic-high state) |

(1) The different cases can be interpreted as follow:

- Case 1: If a logic-low state is present at the first sampling time and also at the second sampling time, the receive data can be interpreted as a break pulse.
- Case 2: If a logic-low state is present at the first sampling time and a logic-high state is present at the second sampling time, the receive data on the line is a zero (data).
- Case 3: Undefined.
- Case 4: If a logic-high state is present at the first sampling time and also at the second sampling time, the receive data on the line is a one (data).

Table 6-103. HDQ Switching Characteristics⁽¹⁾

| PARAMETER | | OPP_NOM | | UNIT |
|-------------------|------------------------------------|---------|-----|------|
| | | MIN | MAX | |
| t _B | Break timing | 190 | | μs |
| t _{BR} | Break recovery time | 40 | | |
| t _{CYCD} | Write bit windows timing | 190 | | |
| t _{DW1} | Write one data valid after HDQ low | 0.5 | 50 | |
| t _{DW0} | Write zero data hold after HDQ low | 86 | 145 | |

(1) See Section 4.3 for CORE OPP voltages.

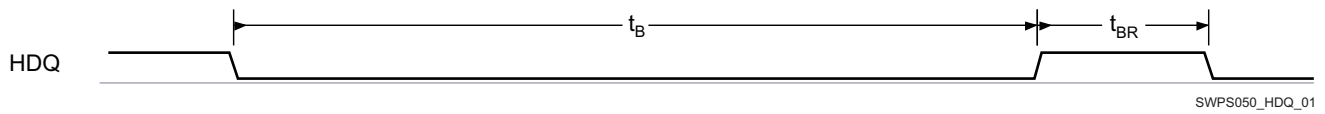


Figure 6-69. HDQ Break and Break Recovery Timing—OMAP HDQ Interface Writing Slave

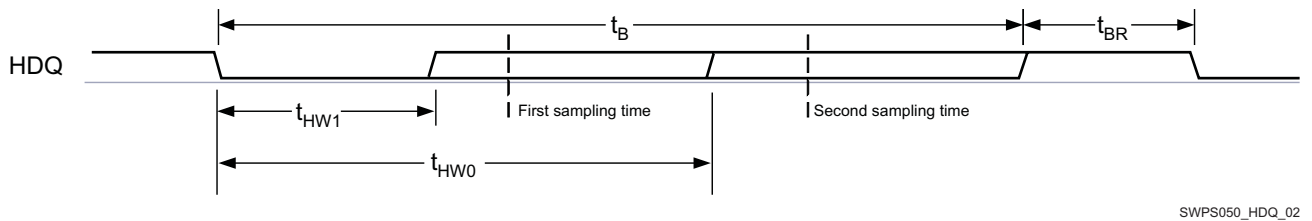


Figure 6-70. HDQ Break Detection Timing—OMAP HDQ Interface Reading Slave

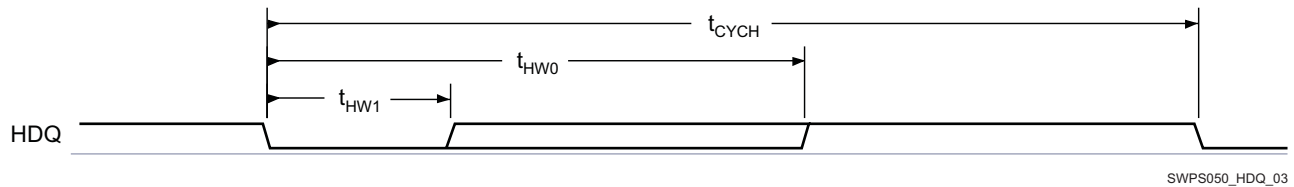


Figure 6-71. HDQ Bit Read Timing (Data)

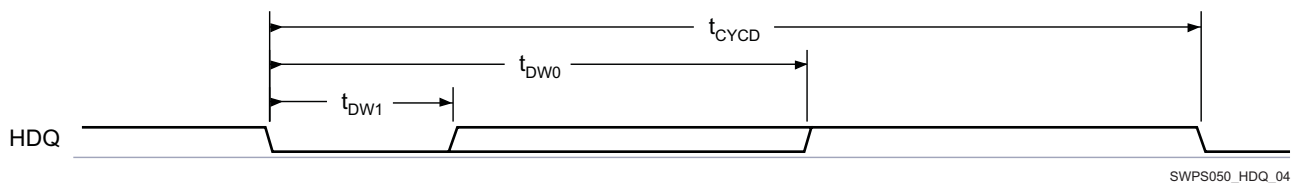


Figure 6-72. HDQ Bit Write Timing (Command / Address / Data)

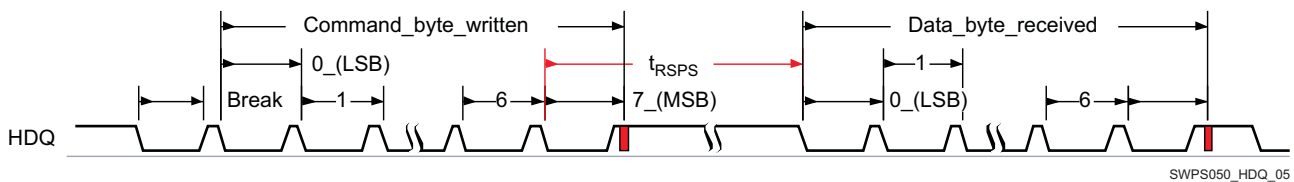


Figure 6-73. HDQ Communication Timing

6.6.9.2 1-Wire Mode

Table 6-104 and Table 6-105 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-104. 1-Wire Timing Requirements⁽¹⁾

| PARAMETER | | OPP_NOM | | UNIT |
|------------------|---------------------------|-------------------|-----|------|
| | | MIN | MAX | |
| t _{PDH} | Presence pulse delay high | 15 | 60 | μs |
| t _{PDL} | Presence pulse delay low | 60 | 240 | |
| t _{RDV} | Read data valid time | t _{LOWR} | 15 | |
| t _{REL} | Read data release time | 0 | 45 | |

(1) See Section 4.3 for CORE OPP voltages.

Table 6-105. 1-Wire Switching Characteristics⁽³⁾

| PARAMETER | | OPP_NOM | | UNIT |
|------------|-------------------------------------|---------|-----|---------|
| | | MIN | MAX | |
| t_{RSTL} | Reset time low | 480 | 960 | μ s |
| t_{RSTH} | Reset time high | 480 | | μ s |
| t_{SLOT} | Bit cycle time | 60 | 120 | μ s |
| t_{LOW1} | Write bit-one time | 1 | 15 | μ s |
| t_{LOW0} | Write bit-zero time ⁽²⁾ | 60 | 120 | μ s |
| t_{REC} | Recovery time | 1 | | μ s |
| t_{LOWR} | Read bit strobe time ⁽¹⁾ | 1 | 15 | μ s |

(1) t_{LOWR} (low pulse sent by the master) must be short as possible to maximize the master sampling window.

(2) t_{LOW0} must be less than t_{SLOT} .

(3) See Section 4.3 for CORE OPP voltages.

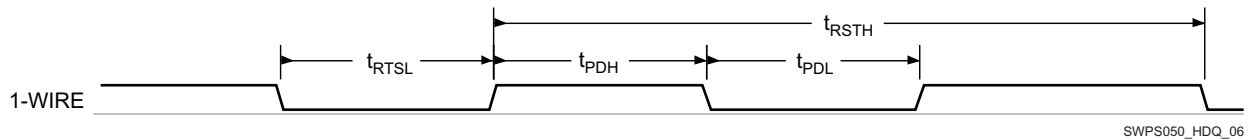


Figure 6-74. 1-Wire Reset Timing

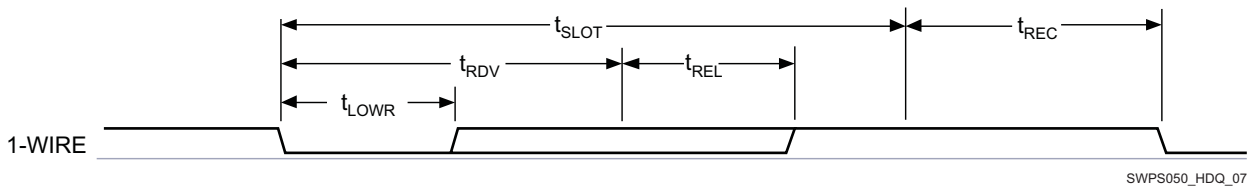


Figure 6-75. 1-Wire Bit Read Timing (Data)

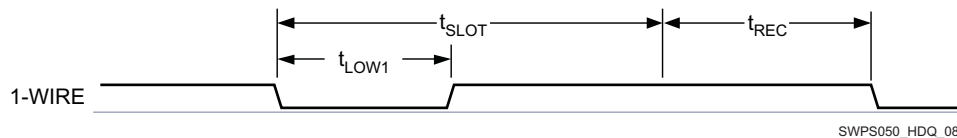


Figure 6-76. 1-Wire Bit-One Write Timing (Command / Address / Data)

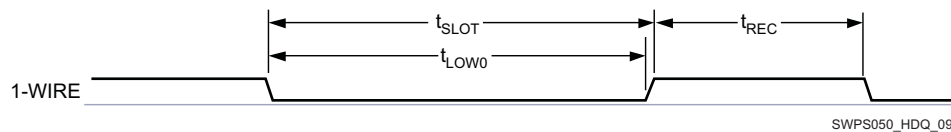


Figure 6-77. 1-Wire Bit-Zero Write Timing (Command / Address / Data)

6.6.10 Universal Asynchronous Receiver Transmitter (UART), 1.8 V

NOTE

The UART4 and UART6 interfaces are not available in the OMAP5432 device. For more information, see the Device TRM.

NOTE

For more information, see the Serial Communication Interface section of the Device TRM.

6.6.10.1 UART1, UART2, and UART5

Table 6-106. UART1 Switching Characteristics

| SIGNAL NAME | MUX MODE | DESCRIPTION | MIN | NOM | MAX | UNIT | |
|--|----------|---|---------------------------------------|-----|-----|------|----|
| uart1_tx (D10/AF3), uart1_rx (D9/AE3), uart1_cts (E9/AF2), uart1_rts(E10/AE2) | 0 or 2 | Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 40 Ω and CLOAD = 10 pF | SC[1:0] = 00 (slowest) | 1.6 | | 3.6 | ns |
| | | | SC[1:0] = 01 (slow) | 0.9 | | 2.0 | |
| | | | SC[1:0] = 10 (fast) | 0.6 | | 1.1 | |
| | | | SC[1:0] = 11 (fastest) ⁽¹⁾ | NA | | NA | |
| | | Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 60 Ω and CLOAD = 10 pF | SC[1:0] = 00 (slowest) | 1.6 | | 3.75 | |
| | | | SC[1:0] = 01 (slow) | 1.0 | | 2.25 | |
| | | | SC[1:0] = 10 (fast) | 0.7 | | 1.4 | |
| | | | SC[1:0] = 11 (fastest) ⁽¹⁾ | N/A | | N/A | |

(1) SC[1:0] = 11 is the fastest bit setting. It is not supported.

Table 6-107. UART2 Switching Characteristics

| SIGNAL NAME | MUX MODE | DESCRIPTION | MIN | NOM | MAX | UNIT | |
|--|----------|---|---------------------------------------|-----|-----|------|----|
| uart2_tx (B6), uart2_rx (C6), uart2_cts (B5), uart2_rts(C5) | 0 | Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 40 Ω and CLOAD = 10 pF | SC[1:0] = 00 (slowest) | 1.6 | | 3.6 | ns |
| | | | SC[1:0] = 01 (slow) | 0.9 | | 2.0 | |
| | | | SC[1:0] = 10 (fast) | 0.6 | | 1.1 | |
| | | | SC[1:0] = 11 (fastest) ⁽¹⁾ | N/A | | N/A | |
| | | Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 60 Ω and CLOAD = 10 pF | SC[1:0] = 00 (slowest) | 1.6 | | 3.75 | |
| | | | SC[1:0] = 01 (slow) | 1.0 | | 2.25 | |
| | | | SC[1:0] = 10 (fast) | 0.7 | | 1.4 | |
| | | | SC[1:0] = 11 (fastest) ⁽¹⁾ | N/A | | N/A | |

(1) SC[1:0] = 11 is the fastest bit setting. It is not supported.

(1) SC[1:0] = 11 is the fastest bit setting. It is not supported.

Table 6-108. UART5 Switching Characteristics

| SIGNAL NAME | MUX MODE | DESCRIPTION | MIN | NOM | MAX | UNIT | |
|---|----------|---|---------------------------------------|-----|-----|------|----|
| uart5_tx (AE29), uart5_rx (AD30), uart5_cts (AE30), uart5_rts (AD29) | 0 | Output transition time (t _R or t _F evaluated between 10% and 90% of VPAD) for drive strength = 40 Ω and CLOAD = 10 pF | SC[1:0] = 00 (slowest) | 1.6 | | 3.6 | ns |
| | | | SC[1:0] = 01 (slow) | 0.9 | | 2.0 | |
| | | | SC[1:0] = 10 (fast) | 0.6 | | 1.1 | |
| | | | SC[1:0] = 11 (fastest) ⁽¹⁾ | N/A | | N/A | |
| | | Output transition time (t _R or t _F evaluated between 10% and 90% of VPAD) for drive strength = 60 Ω and CLOAD = 10 pF | SC[1:0] = 00 (slowest) | 1.6 | | 3.75 | |
| | | | SC[1:0] = 01 (slow) | 1.0 | | 2.25 | |
| | | | SC[1:0] = 10 (fast) | 0.7 | | 1.4 | |
| | | | SC[1:0] = 11 (fastest) ⁽¹⁾ | N/A | | N/A | |

(1) SC[1:0] = 11 is the fastest bit setting. It is not supported.

(1) SC[1:0] = 11 is the fastest bit setting. It is not supported.

6.6.10.2 UART3 IrDA

The IrDA module can operate in the following three modes:

- Slow infrared (SIR) (≤ 115.2 Kbits/s)
- Medium infrared (MIR) (0.576 Mbits/s and 1.152 Mbits/s)
- Fast infrared (FIR) (4 Mbits/s)

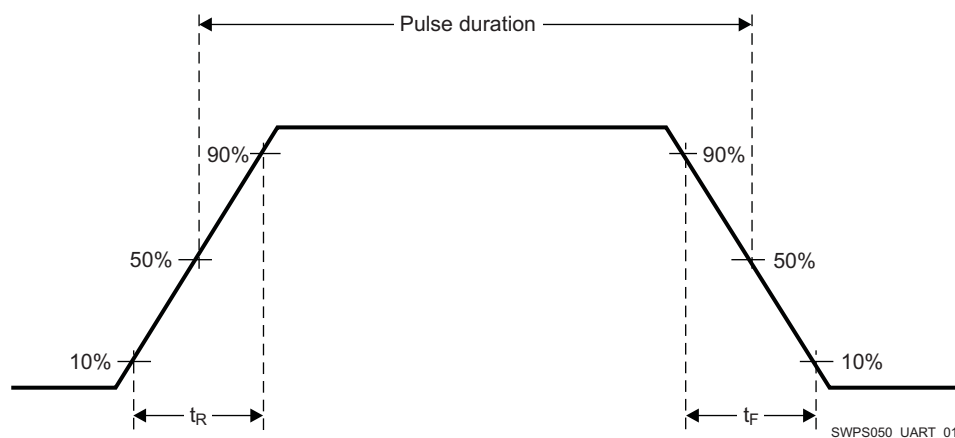


Figure 6-78. UART IrDA Pulse Parameters

6.6.10.2.1 UART3 IrDA – Receive Mode

Table 6-109. UART3 IrDA Signaling Rate and Pulse Duration with 3/16th Encoding – Receive Mode

| SIGNALING RATE | ELECTRICAL PULSE DURATION | | | UNIT |
|----------------|---------------------------|-------|--------|------|
| | MIN | TYP | MAX | |
| SIR | | | | |
| 2.4 Kbit/s | 52.17 | 78.13 | 208.33 | μs |
| 9.6 Kbit/s | 13.10 | 19.53 | 52.08 | μs |
| 19.2 Kbit/s | 6.59 | 9.77 | 26.04 | μs |
| 38.4 Kbit/s | 3.34 | 4.88 | 13.02 | μs |
| 57.6 Kbit/s | 2.25 | 3.26 | 8.68 | μs |

Table 6-109. UART3 IrDA Signaling Rate and Pulse Duration with 3/16th Encoding – Receive Mode (continued)

| SIGNALING RATE | ELECTRICAL PULSE DURATION | | | UNIT |
|---------------------------|---------------------------|--------|--------|------|
| | MIN | TYP | MAX | |
| 115.2 Kbit/s | 1.17 | 1.63 | 4.34 | μs |
| MIR | | | | |
| 0.576 Mbit/s | 300.55 | 416.67 | 867.86 | ns |
| 1.152 Mbit/s | 192.04 | 208.33 | 433.83 | ns |
| FIR | | | | |
| 4.0 Mbit/s (Single pulse) | 62.70 | 125.00 | 170.63 | ns |
| 4.0 Mbit/s (Double pulse) | 208.53 | 250.00 | 291.47 | ns |

NOTE

In SIR Receive mode, both the 3/16th and the 1.6μs pulse duration methods are supported. For more information, see the UART/IrDA/CIR section of the Serial Communication Interface chapter in the Device TRM.

Table 6-110. UART3 IrDA Rise and Fall Times – Receive Mode

| PARAMETER | | MIN | TYP | MAX | UNIT |
|----------------|-------------------------------------|-----|-----|-----|------|
| t _R | Rise time, input data uart3_rx_irrx | | | 200 | ns |
| t _F | Fall time, input data uart3_rx_irrx | | | 200 | ns |

6.6.10.2.2 UART3 IrDA – Transmit Mode
Table 6-111. UART3 IrDA Signaling Rate and Pulse Duration with 3/16th Encoding – Transmit Mode

| SIGNALING RATE | ELECTRICAL PULSE DURATION | | | UNIT |
|---------------------------|---------------------------|------|-----|------|
| | MIN | TYP | MAX | |
| SIR | | | | |
| 2.4 Kbit/s | | 78.1 | | μs |
| 9.6 Kbit/s | | 19.5 | | μs |
| 19.2 Kbit/s | | 9.75 | | μs |
| 38.4 Kbit/s | | 4.87 | | μs |
| 57.6 Kbit/s | | 3.25 | | μs |
| 115.2 Kbit/s | | 1.62 | | μs |
| MIR | | | | |
| 0.576 Mbit/s | 414 | 416 | 419 | ns |
| 1.152 Mbit/s | 206 | 208 | 211 | ns |
| FIR | | | | |
| 4.0 Mbit/s (Single pulse) | 123 | 125 | 128 | ns |
| 4.0 Mbit/s (Double pulse) | 248 | 250 | 253 | ns |

NOTE

In SIR Receive mode, both the 3/16th and the 1.6μs pulse duration methods are supported. For more information, see the UART/IrDA/CIR section of the Serial Communication Interface chapter in the Device TRM.

6.6.11 Serial Advanced Technology Attachment (SATA), 1.8 V

NOTE

For more information, see the SATA Controller section of the Device TRM.

The SATA RX/TX PHY interface is compliant with the SATA standard v2.6 for a maximum data rate:

- Gen2i, Gen2m, Gen2x: 3Gbps at OPP_NOM.
- Gen1i, Gen1m, Gen1x: 1.5Gbps at OPP_NOM.

6.6.12 MMC2—eMMC, 1.8 V

NOTE

For more information, see the MMC/SDIO chapter of the Device TRM.

MMC2 interface is compliant with the JC64 eMMC Standard v4.5 and it supports the following eMMC applications:

- Standard JC64 SDR at 24 MHz, 8-bit data, half cycle, 1.8 V
- High-speed JC64 SDR at 48 MHz, 8-bit data, half cycle, 1.8 V
- High-speed JC64 DDR at 48 MHz, 8-bit data, and 1.8 V
- High-speed HS200 JC64 SDR at 192 MHz, 8-bit data, half cycle, 1.8 V

6.6.12.1 eMMC, Standard JC64 SDR, 24 MHz, Half Cycle, 1.8 V

Table 6-112 and Table 6-113 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-112. Standard JC64 SDR eMMC Timing Requirements—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|---------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| STDeMMC5 | $t_{su(cmdV-clkH)}$ | Setup time, emmc_cmd valid before emmc_clk rising edge | 12.38 | | ns |
| STDeMMC6 | $t_{h(clkH-cmdV)}$ | Hold time, emmc_cmd valid after emmc_clk rising edge | 1.73 | | ns |
| STDeMMC7 | $t_{su(dV-clkH)}$ | Setup time, emmc_data[7:0] valid before emmc_clk rising edge | 12.38 | | ns |
| STDeMMC8 | $t_{h(clkH-dV)}$ | Hold time, emmc_data[7:0] valid after emmc_clk rising edge | 1.73 | | ns |

(1) See Section 4.3 for CORE OPP voltages.

Table 6-113. Standard JC64 SDR eMMC Switching Characteristics—1.8 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|--------------------|--|------------------------------|-------|------|
| | | | MIN | MAX | |
| STDeMMC1 | $1 / t_{c(clk)}$ | Frequency, output emmc_clk | | 24 | MHz |
| STDeMMC2 | $t_{W(clkH)}$ | Pulse duration, output emmc_clk high | 0.5 * P-0.172 ⁽¹⁾ | | ns |
| STDeMMC2 | $t_{W(clkL)}$ | Pulse duration, output emmc_clk low | 0.5 * P-0.172 ⁽¹⁾ | | ns |
| STDeMMC3 | $t_{d(clkL-cmdV)}$ | Delay time, emmc_clk falling edge to emmc_cmd transition | -15.32 | 15.32 | ns |
| STDeMMC4 | $t_{d(clkL-doV)}$ | Delay time, emmc_clk falling edge to emmc_data[7:0] transition | -15.32 | 15.32 | ns |

- (1) P = output emmc_clk period in ns
 (2) See Section 4.3 for CORE OPP voltages.

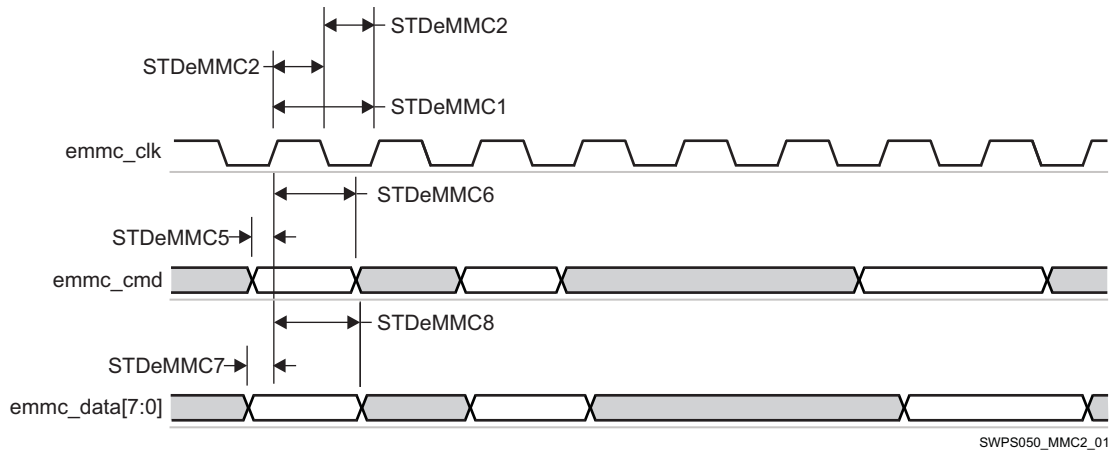


Figure 6-79. Standard JC64 SDR eMMC, 1.8 V—Receiver Mode

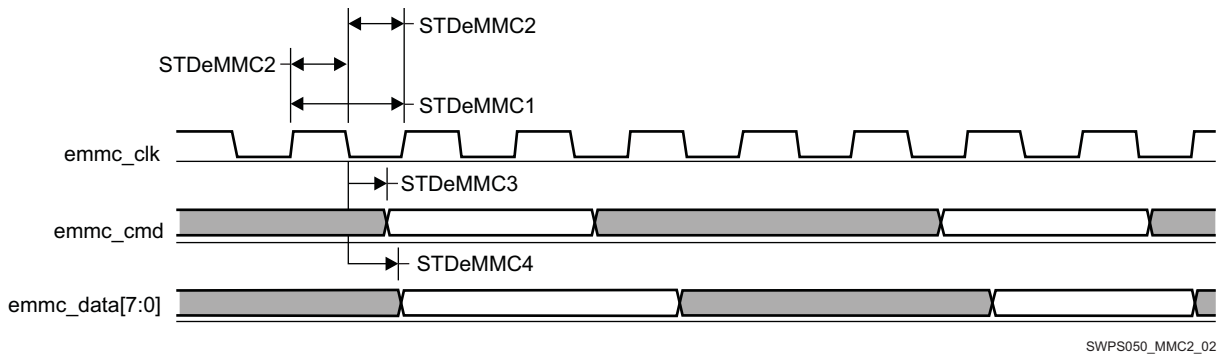


Figure 6-80. Standard JC64 SDR eMMC, 1.8 V—Transmitter Mode

6.6.12.2 eMMC, High-Speed JC64 SDR, 48 MHz, Half Cycle, 1.8 V

Table 6-114 and Table 6-115 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-114. High-Speed JC64 SDR eMMC Timing Requirements—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|---------|---------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| HSeMMC3 | $t_{su}(cmdV-clkH)$ | Setup time, emmc_cmd valid before emmc_clk rising edge | 5.02 | | ns |
| HSeMMC4 | $t_{h}(clkH-cmdV)$ | Hold time, emmc_cmd valid after emmc_clk rising edge | 2.14 | | ns |
| HSeMMC7 | $t_{su}(dV-clkH)$ | Setup time, emmc_data[7:0] valid before emmc_clk rising edge | 5.02 | | ns |
| HSeMMC8 | $t_{h}(clkH-dV)$ | Hold time, emmc_data[7:0] valid after emmc_clk rising edge | 2.14 | | ns |

- (1) See Section 4.3 for CORE OPP voltages.

Table 6-115. High-Speed JC64 SDR eMMC Switching Characteristics—1.8 V⁽³⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|---------|------------------|--|-------------------------|-----|------|
| | | | MIN | MAX | |
| HSeMMC1 | $1 / t_{c}(clk)$ | Frequency, output emmc_clk | | 48 | MHz |
| HSeMMC2 | $t_{W}(clkH)$ | Typical pulse duration, output emmc_clk high | $0.5 * P - 0.172^{(1)}$ | | ns |

Table 6-115. High-Speed JC64 SDR eMMC Switching Characteristics—1.8 V⁽³⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|---------|--------------------------|--|------------------------------|------|------|
| | | | MIN | MAX | |
| HSeMMC2 | $t_{W(\text{clkL})}$ | Typical pulse duration, output emmc_clk low | 0.5 * P-0.172 ⁽¹⁾ | | ns |
| HSeMMC5 | $t_{d(\text{clkL-dOv})}$ | Delay time, emmc_clk falling edge to emmc_cmd transition | -5.32 | 5.32 | ns |
| HSeMMC6 | $t_{d(\text{clkL-dOV})}$ | Delay time, emmc_clk falling edge to emmc_data[7:0] transition | -5.32 | 5.32 | ns |

- (1) P = output emmc_clk period in ns
- (2) The jitter probability density can be approximated by a Gaussian function.
- (3) See Section 4.3 for CORE OPP voltages.

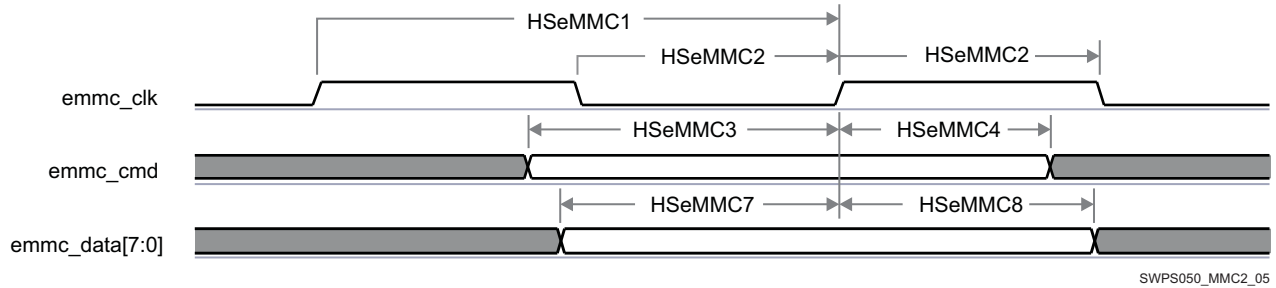


Figure 6-81. High-Speed JC64 SDR eMMC, 1.8 V—Receiver Mode

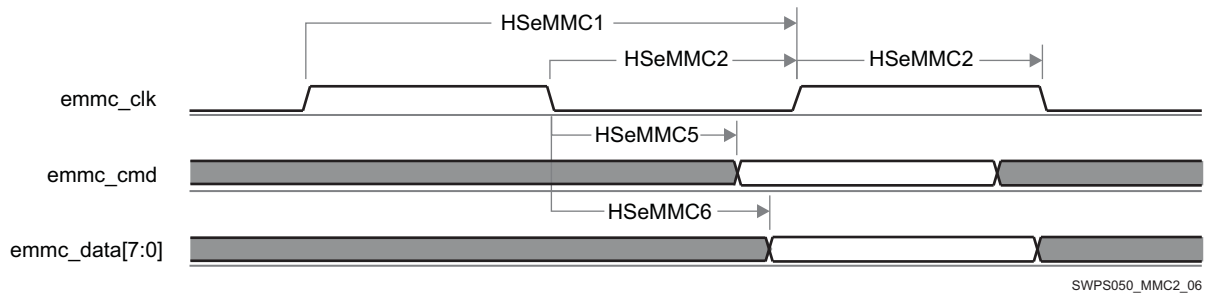


Figure 6-82. High-Speed JC64 SDR eMMC, 1.8 V—Transmitter Mode

6.6.12.3 eMMC, High-Speed JC64 DDR, 48 MHz, 1.8 V

Table 6-116 and Table 6-117 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-116. High-Speed JC64 DDR eMMC Timing Requirements—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|----------------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| DDReMMC3 | $t_{su(\text{cmdV-clkH})}$ | Setup time, emmc_cmd valid before emmc_clk rising edge | 5.14 | | ns |
| DDReMMC4 | $t_{h(\text{clkH-cmdV})}$ | Hold time, emmc_cmd valid after emmc_clk rising edge | 2.24 | | ns |
| DDReMMC7 | $t_{su(\text{dV-clkH})}$ | Setup time, emmc_data[7:0] valid before emmc_clk falling/rising edge | 1.35 | | ns |
| DDReMMC8 | $t_{h(\text{clkH-dV})}$ | Hold time, emmc_data[7:0] valid after emmc_clk falling/rising edge | 1.25 | | ns |

- (1) See Section 4.3 for CORE OPP voltages.

Table 6-117. High-Speed JC64 DDR eMMC Switching Characteristics—1.8 V⁽²⁾

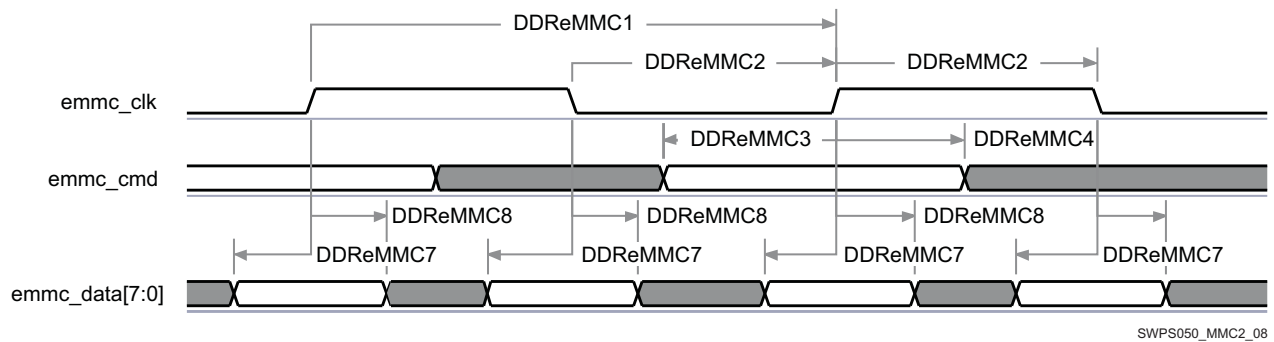
| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|-------------------------|----------------------------|---------|-----|------|
| | | | MIN | MAX | |
| DDReMMC1 | $1 / t_{c(\text{clk})}$ | Frequency, output emmc_clk | | 48 | MHz |

Table 6-117. High-Speed JC64 DDR eMMC Switching Characteristics—1.8 V⁽²⁾ (continued)

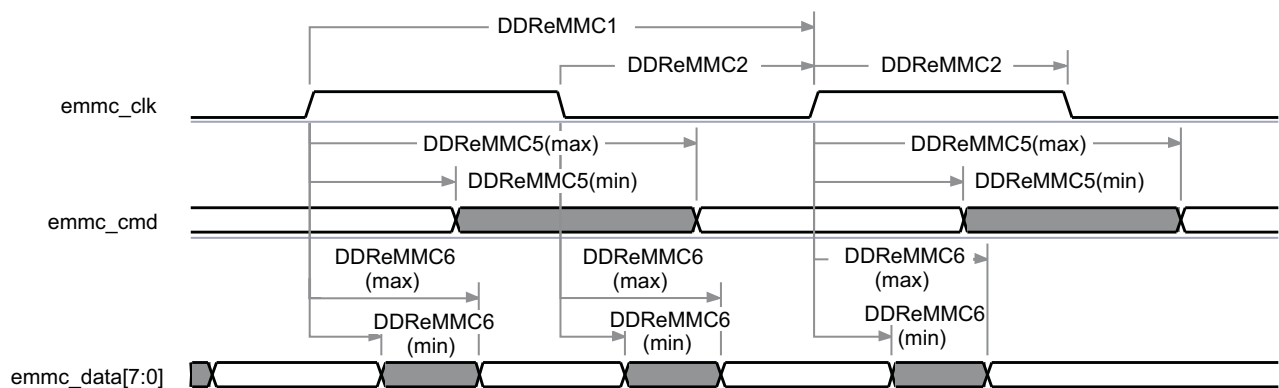
| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|---------------------------|---|-------------------------|-------|------|
| | | | MIN | MAX | |
| DDReMMC2 | $t_{W(\text{clkH})}$ | Typical pulse duration, output emmc_clk high | $0.5 * P - 0.172^{(1)}$ | | ns |
| DDReMMC2 | $t_{W(\text{clkL})}$ | Typical pulse duration, output emmc_clk low | $0.5 * P - 0.172^{(1)}$ | | ns |
| DDReMMC5 | $t_{d(\text{clkL-cmdV})}$ | Delay time, emmc_clk rising edge to emmc_cmd transition | 4.56 | 15.79 | ns |
| DDReMMC6 | $t_{d(\text{clkL-doV})}$ | Delay time, emmc_clk falling/rising edge to emmc_data[7:0] transition | 4.06 | 5.82 | ns |

(1) P = output emmc_clk period in ns

(2) See Section 4.3 for CORE OPP voltages.



SWPS050_MMC2_08

Figure 6-83. High-Speed JC64 DDR eMMC, 1.8 V—Receiver Mode

SWPS050_MMC2_09

Figure 6-84. High-Speed JC64 DDR eMMC, 1.8 V—Transmitter Mode**6.6.12.4 eMMC, High-Speed HS200 JC64 SDR, 192 MHz, Half Cycle, 1.8 V**

Table 6-118 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-118. High-Speed HS200 JC64 SDR eMMC Switching Characteristics—1.8 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------------|-------------------------|--|-------------------------|-----|------|
| | | | MIN | MAX | |
| HS200eMMC1 | $1 / t_{c(\text{clk})}$ | Frequency, output emmc_clk | | 192 | MHz |
| HS200eMMC2 | $t_{W(\text{clkH})}$ | Typical pulse duration, output emmc_clk high | $0.5 * P - 0.172^{(1)}$ | | ns |
| HS200eMMC2 | $t_{W(\text{clkL})}$ | Typical pulse duration, output emmc_clk low | $0.5 * P - 0.172^{(1)}$ | | ns |

Table 6-118. High-Speed HS200 JC64 SDR eMMC Switching Characteristics—1.8 V⁽²⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------------|--------------------------|--|---------|------|------|
| | | | MIN | MAX | |
| HS200eMMC5 | $t_{d(\text{clkL-d0V})}$ | Delay time, emmc_clk falling edge to emmc_cmd transition | -1.13 | 0.53 | ns |
| HS200eMMC6 | $t_{d(\text{clkL-d0V})}$ | Delay time, emmc_clk falling edge to emmc_data[7:0] transition | -1.13 | 0.53 | ns |

(1) P = output emmc_clk period in ns

(2) See Section 4.3 for CORE OPP voltages.

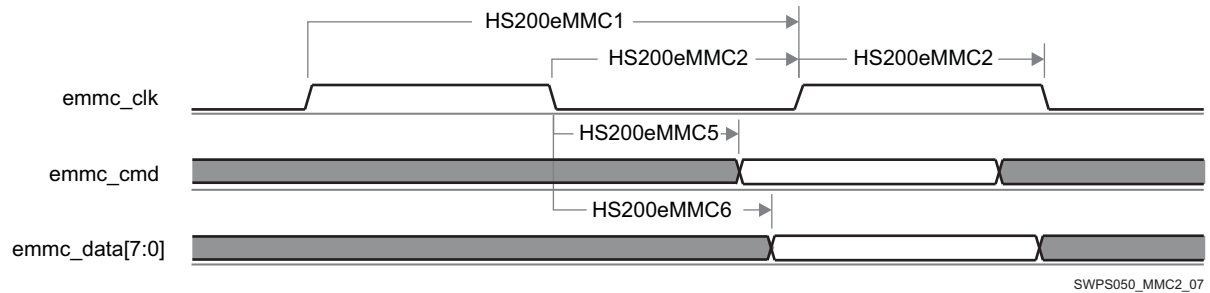


Figure 6-85. High-Speed HS200 JC64 SDR eMMC, 1.8 V—Transmitter Mode

6.6.13 MMC3 and MMC4—SDIO, 1.8 V

NOTE

For more information, see the MMC/SDIO chapter of the Device TRM.

MMC3 and MMC4 interfaces are compliant with the SDIO3.0 standard v1.0, SD Part E1 and for generic SDIO devices, it supports the following applications:

- SDIO Standard speed at 24 MHz (SDR12 mode of the SD Standard v3.01), 4-bit data, SDR, half cycle, 1.8 V
- SDIO High speed at 48 MHz (SDR25 mode of the SD Standard v3.01), 4-bit data, SDR, half cycle, 1.8 V

6.6.13.1 MMC3 and MMC4 SDIO Standard Speed (SDR12), 24 MHz, Half Cycle, 1.8 V

Table 6-119 and Table 6-120 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-119. SDIO Standard Speed (SDR12) Timing Requirements—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|---------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| SDIO5 | $t_{su(cmdV-clkH)}$ | Setup time, sdio_cmd valid before sdio_clk rising edge | 25.6 | | ns |
| SDIO6 | $t_{h(clkH-cmdV)}$ | Hold time, sdio_cmd valid after sdio_clk rising edge | 1.21 | | ns |
| SDIO7 | $t_{su(dV-clkH)}$ | Setup time, sdio_data[3:0] valid before sdio_clk rising edge | 25.6 | | ns |
| SDIO8 | $t_{h(clkH-dV)}$ | Hold time, sdio_data[3:0] valid after sdio_clk rising edge | 1.21 | | ns |

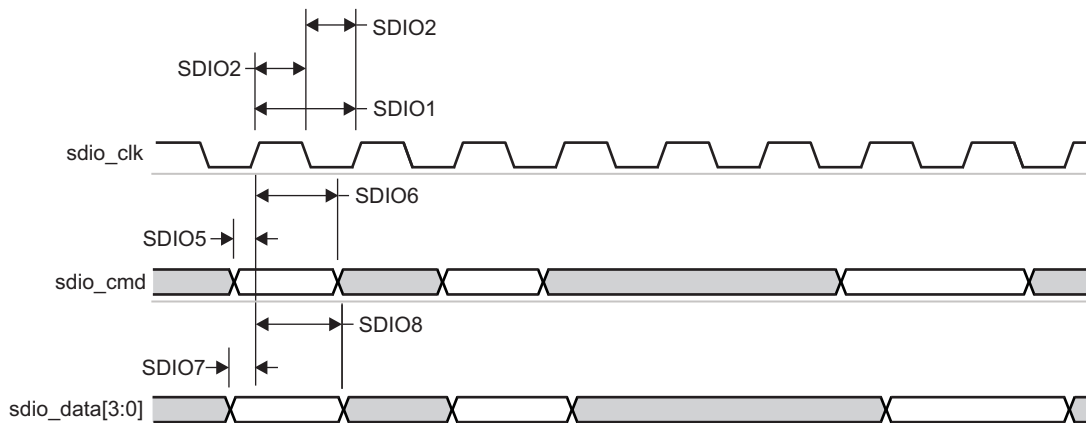
(1) See Section 4.3 for CORE OPP voltages.

Table 6-120. SDIO Standard Speed (SDR12) Switching Characteristics—1.8 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|--------------------|--|------------------|------|------|
| | | | MIN | MAX | |
| SDIO1 | $1 / t_{c(clk)}$ | Frequency, output sdio_clk | | 24 | MHz |
| SDIO2 | $t_{W(clkH)}$ | Typical pulse duration, output sdio_clk high | $0.45 * P^{(1)}$ | | ns |
| SDIO2 | $t_{W(clkL)}$ | Typical pulse duration, output sdio_clk low | $0.45 * P^{(1)}$ | | ns |
| SDIO3 | $t_{d(clkL-cmdV)}$ | Delay time, sdio_clk falling edge to sdio_cmd transition | -15.4 | 13.2 | ns |
| SDIO4 | $t_{d(clkL-doV)}$ | Delay time, sdio_clk falling edge to sdio_data[3:0] transition | -15.4 | 13.2 | ns |

(1) P = output sdio_clk period in ns

(2) See Section 4.3 for CORE OPP voltages.



SWPS050_SDIO_01

Figure 6-86. SDIO Standard Speed, 1.8 V—Receiver Mode

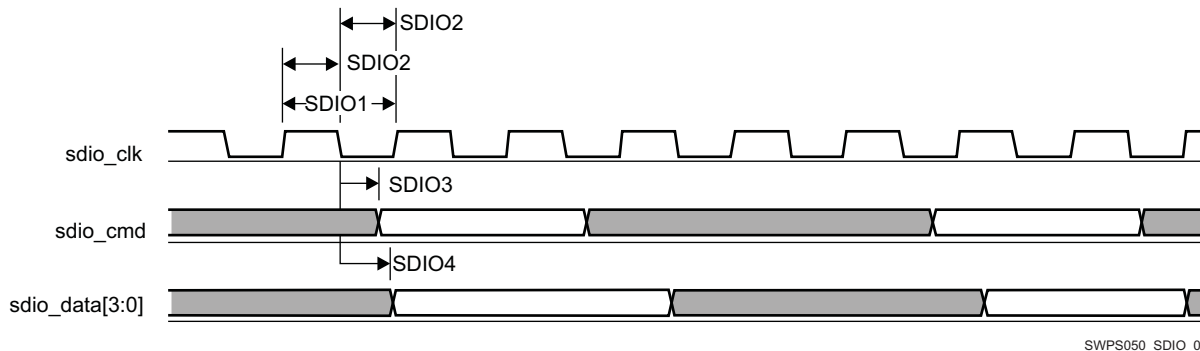


Figure 6-87. SDIO Standard Speed, 1.8 V—Transmitter Mode

6.6.13.2 MMC3 and MMC4 SDIO High-Speed (SDR25), 48 MHz, Half Cycle, 1.8 V

Table 6-121 and Table 6-122 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-121. SDIO High-Speed (SDR25) Timing Requirements—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|---------|---------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| HSSDIO3 | $t_{su(cmdV-clkH)}$ | Setup time, sdio_cmd valid before sdio_clk rising edge | 5.21 | | ns |
| HSSDIO4 | $t_{h(clkH-cmdV)}$ | Hold time, sdio_cmd valid after sdio_clk rising edge | 1.63 | | ns |
| HSSDIO7 | $t_{su(dV-clkH)}$ | Setup time, sdio_data[3:0] valid before sdio_clk rising edge | 5.21 | | ns |
| HSSDIO8 | $t_{h(clkH-dV)}$ | Hold time, sdio_data[3:0] valid after sdio_clk rising edge | 1.63 | | ns |

(1) See Section 4.3 for CORE OPP voltages.

Table 6-122. SDIO High-Speed (SDR25) Switching Characteristics—1.8 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|---------|-------------------|--|-------------------------|------|------|
| | | | MIN | MAX | |
| HSSDIO1 | $f_{c(clk)}$ | Frequency, output sdio_clk | | 48 | MHz |
| HSSDIO2 | $t_{W(clkH)}$ | Typical pulse duration, output sdio_clk high | 0.45 * P ⁽¹⁾ | | ns |
| HSSDIO2 | $t_{W(clkL)}$ | Typical pulse duration, output sdio_clk low | 0.45 * P ⁽¹⁾ | | ns |
| HSSDIO5 | $t_{d(clkL-doV)}$ | Delay time, sdio_clk falling edge to sdio_cmd transition | -6.48 | 4.28 | ns |
| HSSDIO6 | $t_{d(clkL-doV)}$ | Delay time, sdio_clk falling edge to sdio_data[3:0] transition | -6.48 | 4.28 | ns |

(1) P = output sdio_clk period in ns

(2) See Section 4.3 for CORE OPP voltages.

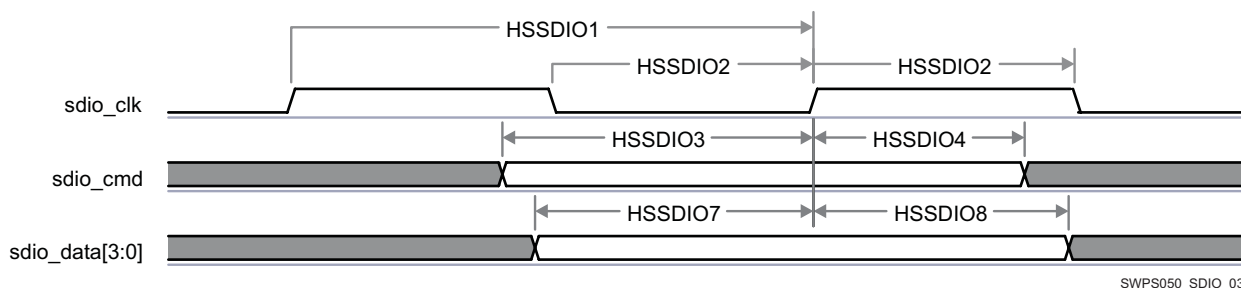
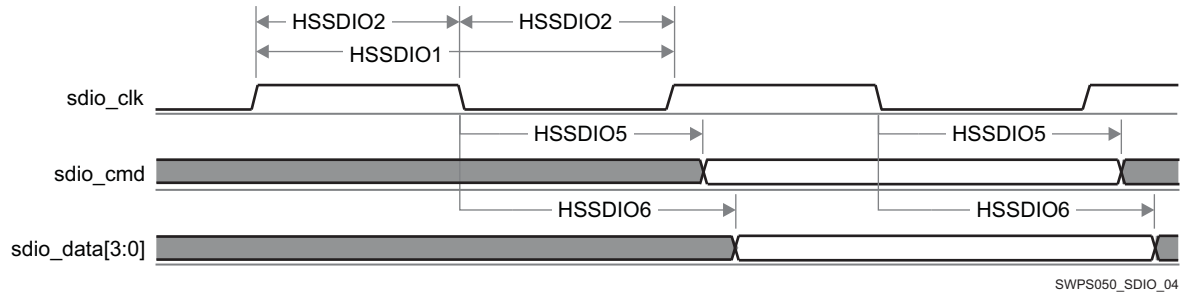


Figure 6-88. SDIO High-Speed, 1.8 V—Receiver Mode

**Figure 6-89. SDIO High-Speed, 1.8 V—Transmitter Mode**

6.7 Removable Media Interfaces

6.7.1 MMC1—SD Card Interface, 1.8 V and 3.0 V

NOTE

For more information, see the MMC/SDIO chapter of the Device TRM.

MMC1 interface is compliant with the SD Standard v3.01 and it supports the following SD Card applications:

- Default speed at 24 MHz, 4-bit data, SDR, half-cycle, 3.3 V
- High speed at 48 MHz, 4-bit data, SDR, half-cycle, 3.3 V
- SDR12 at 24 MHz, 4-bit data, half-cycle, 1.8 V
- SDR25 at 48 MHz, 4-bit data, half-cycle, 1.8 V
- UHS-I SDR50 at 96 MHz, 4-bit data, half-cycle, 1.8 V
- UHS-I SDR104 at 192 MHz, 4-bit data, half-cycle, 1.8 V
- UHS-I DDR50 at 48 MHz, 4-bit data, 1.8 V

6.7.1.1 SD Card, Default Speed (DS), SDR, 24 MHz, Half-Cycle Mode, 3.3 V

Table 6-123 and Table 6-124 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-123. Default Speed SD Card Timing Requirements—3.3 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|---------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| SSD5 | $t_{su(cmdV-clkH)}$ | Setup time, sdcard_cmd valid before sdcard_clk rising edge | 3.35 | | ns |
| SSD6 | $t_h(clkH-cmdV)$ | Hold time, sdcard_cmd valid after sdcard_clk rising edge | 18.7 | | ns |
| SSD7 | $t_{su(dV-clkH)}$ | Setup time, sdcard_data[3:0] valid before sdcard_clk rising edge | 3.35 | | ns |
| SSD8 | $t_h(clkH-dV)$ | Hold time, sdcard_data[3:0] valid after sdcard_clk rising edge | 18.7 | | ns |

(1) See Section 4.3 for CORE OPP voltages.

Table 6-124. Default Speed SD Card Switching Characteristics—3.3 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|------------------|--|----------------------------|-------|------|
| | | | MIN | MAX | |
| SSD0 | $1 / t_{c(clk)}$ | Frequency, output sdcard_clk | | 24 | MHz |
| SSD1 | $t_w(clkH)$ | Pulse duration, output sdcard_clk high | 0.5*P-0.185 ⁽¹⁾ | | ns |
| SSD2 | $t_w(clkL)$ | Pulse duration, output sdcard_clk low | 0.5*P-0.185 ⁽¹⁾ | | ns |
| SSD3 | $t_d(clkL-cmdV)$ | Delay time, sdcard_clk falling edge to sdcard_cmd transition | -11.52 | 11.52 | ns |
| SSD4 | $t_d(clkL-doV)$ | Delay time, sdcard_clk falling edge to sdcard_data[3:0] transition | -11.52 | 11.52 | ns |

- (1) P = output sdcard_clk period in ns
 (2) See [Section 4.3](#) for CORE OPP voltages.

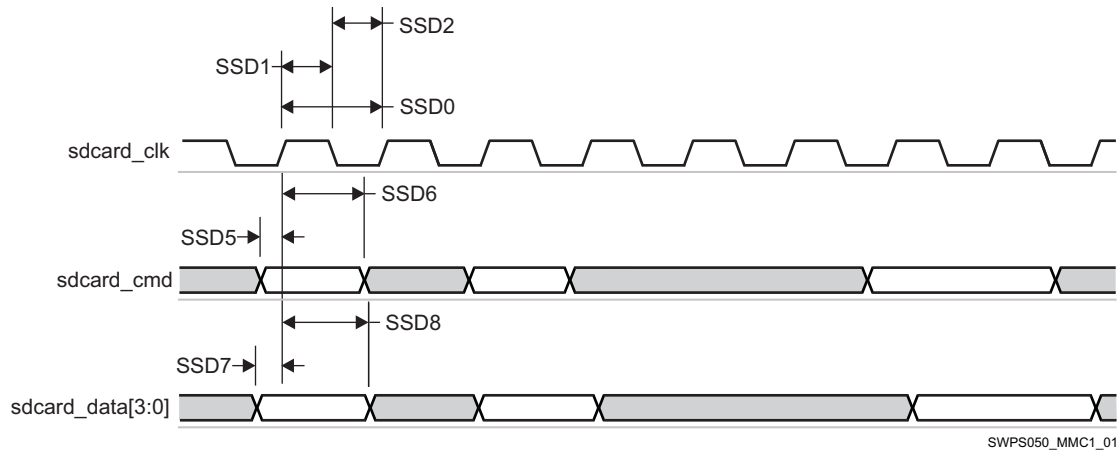


Figure 6-90. Default Speed SD Card, 3.3 V—Receiver Mode

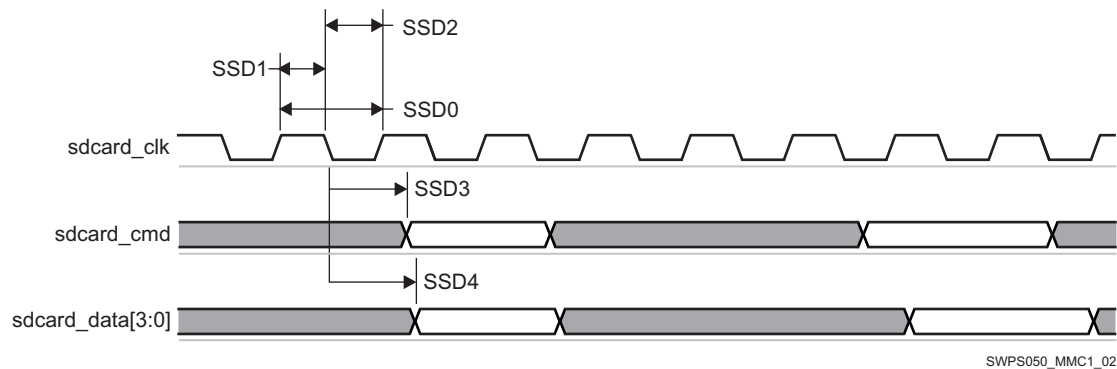


Figure 6-91. Default Speed SD Card, 3.3 V—Transmitter Mode

6.7.1.2 SD Card, High Speed (HS), SDR, 48 MHz, Half-Cycle Mode, 3.3 V

[Table 6-125](#) and [Table 6-126](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-125. High Speed SD Card Timing Requirements—3.3 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|---------|---------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| HSSD333 | $t_{su(cmdV-clkH)}$ | Setup time, sdcard_cmd valid before sdcard_clk rising edge | 5.33 | | ns |
| HSSD334 | $t_{h(clkH-cmdV)}$ | Hold time, sdcard_cmd valid after sdcard_clk rising edge | 2.76 | | ns |
| HSSD337 | $t_{su(dV-clkH)}$ | Setup time, sdcard_data[3:0] valid before sdcard_clk rising edge | 5.33 | | ns |
| HSSD338 | $t_{h(clkH-dV)}$ | Hold time, sdcard_data[3:0] valid after sdcard_clk rising edge | 2.76 | | ns |

- (1) See [Section 4.3](#) for CORE OPP voltages.

Table 6-126. High Speed SD Card Switching Characteristics—3.3 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|---------|------------------|------------------------------|---------|-----|------|
| | | | MIN | MAX | |
| HSSD331 | $1 / t_{c(clk)}$ | Frequency, output sdcard_clk | | 48 | MHz |

Table 6-126. High Speed SD Card Switching Characteristics—3.3 V⁽²⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|---------|---------------------------|--|-------------------------|------|------|
| | | | MIN | MAX | |
| HSSD332 | $t_{w(\text{clkH})}$ | Pulse duration, output sdcard_clk high | $0.5 * P - 0.185^{(1)}$ | | ns |
| HSSD332 | $t_{w(\text{clkL})}$ | Pulse duration, output sdcard_clk low | $0.5 * P - 0.185^{(1)}$ | | ns |
| HSSD335 | $t_{d(\text{clkL-cmdV})}$ | Delay time, sdcard_clk falling edge to sdcard_cmd transition | -6.01 | 2.01 | ns |
| HSSD336 | $t_{d(\text{clkL-dV})}$ | Delay time, sdcard_clk falling edge to sdcard_data[3:0] transition | -6.01 | 2.01 | ns |

(1) P = output sdcard_clk period in ns

(2) See Section 4.3 for CORE OPP voltages.



Figure 6-92. High Speed SD Card, 3.3 V—Receiver Mode

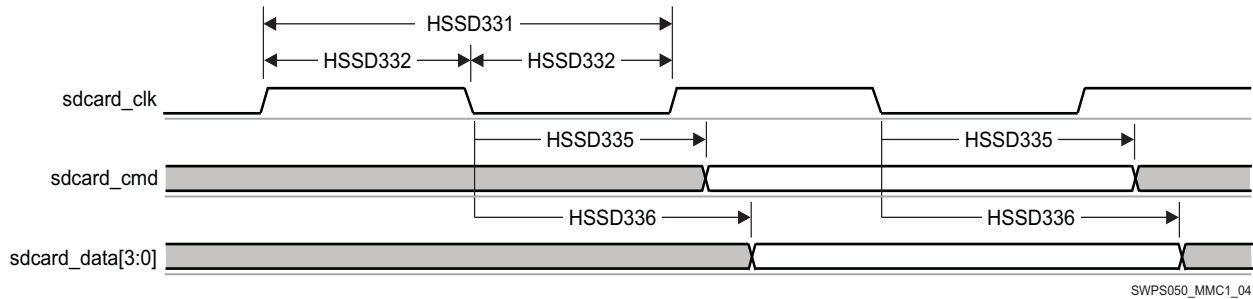


Figure 6-93. High Speed SD Card, 3.3 V—Transmitter Mode

6.7.1.3 SD Card, SDR12, 24 MHz, Half-Cycle Mode, 1.8 V

Table 6-127 and Table 6-128 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-127. SDR12 SD Card Timing Requirements—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|----------------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| HSSDR125 | $t_{su(\text{cmdV-clkH})}$ | Setup time, sdcard_cmd valid before sdcard_clk rising edge | 25.6 | | ns |
| HSSDR126 | $t_{h(\text{clkH-cmdV})}$ | Hold time, sdcard_cmd valid after sdcard_clk rising edge | 1.21 | | ns |
| HSSDR127 | $t_{su(\text{dV-clkH})}$ | Setup time, sdcard_data[3:0] valid before sdcard_clk rising edge | 25.6 | | ns |
| HSSDR128 | $t_{h(\text{clkH-dV})}$ | Hold time, sdcard_data[3:0] valid after sdcard_clk rising edge | 1.21 | | ns |

(1) See Section 4.3 for CORE OPP voltages.

Table 6-128. SDR12 SD Card Switching Characteristics—1.8 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|---------------------------|--|-------------------------|-------|------|
| | | | MIN | MAX | |
| HSSDR120 | $1 / t_{c(\text{clk})}$ | Frequency, output sdcard_clk | | 24 | MHz |
| HSSDR121 | $t_{w(\text{clkH})}$ | Typical pulse duration, output sdcard_clk high | $0.5 * P - 0.185^{(1)}$ | | ns |
| HSSDR122 | $t_{w(\text{clkL})}$ | Typical pulse duration, output sdcard_clk low | $0.5 * P - 0.185^{(1)}$ | | ns |
| HSSDR123 | $t_{d(\text{clkL-cmdV})}$ | Delay time, sdcard_clk falling edge to sdcard_cmd transition | -17.34 | 15.14 | ns |
| HSSDR124 | $t_{d(\text{clkL-doV})}$ | Delay time, sdcard_clk falling edge to sdcard_data[3:0] transition | -17.34 | 15.14 | ns |

(1) P = output sdcard_clk period in ns

(2) See Section 4.3 for CORE OPP voltages.

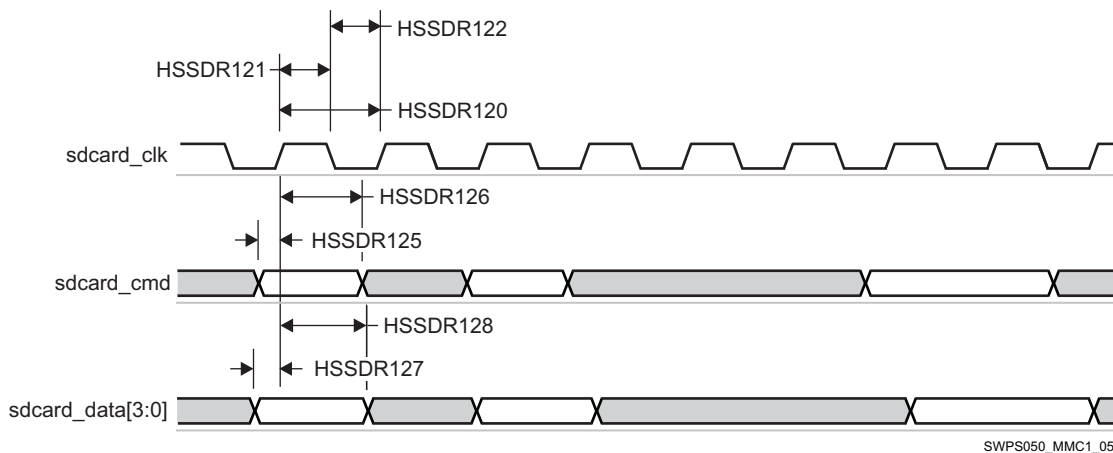


Figure 6-94. SDR12 SD Card, 1.8-V—Receiver Mode

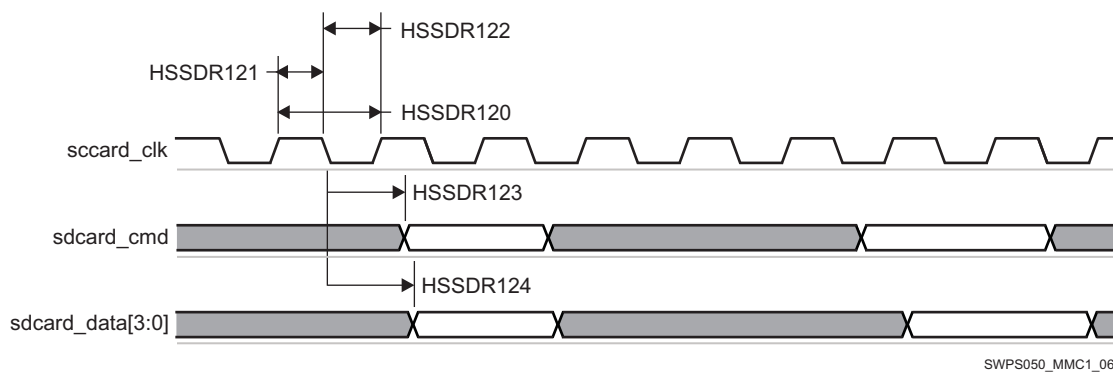


Figure 6-95. SDR12 SD Card, 1.8-V—Transmitter Mode

6.7.1.4 SD Card, SDR25, 48 MHz, Half-Cycle Mode, 1.8 V

Table 6-129 and Table 6-130 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-129. SDR25 SD Card Timing Requirements—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|---------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| HSSDR253 | $t_{su}(cmdV-clkH)$ | Setup time, sdcard_cmd valid before sdcard_clk rising edge | 5.21 | | ns |
| HSSDR254 | $t_{h}(clkH-cmdV)$ | Hold time, sdcard_cmd valid after sdcard_clk rising edge | 1.63 | | ns |
| HSSDR257 | $t_{su}(dV-clkH)$ | Setup time, sdcard_data[3:0] valid before sdcard_clk rising edge | 5.21 | | ns |
| HSSDR258 | $t_{h}(clkH-dV)$ | Hold time, sdcard_data[3:0] valid after sdcard_clk rising edge | 1.63 | | ns |

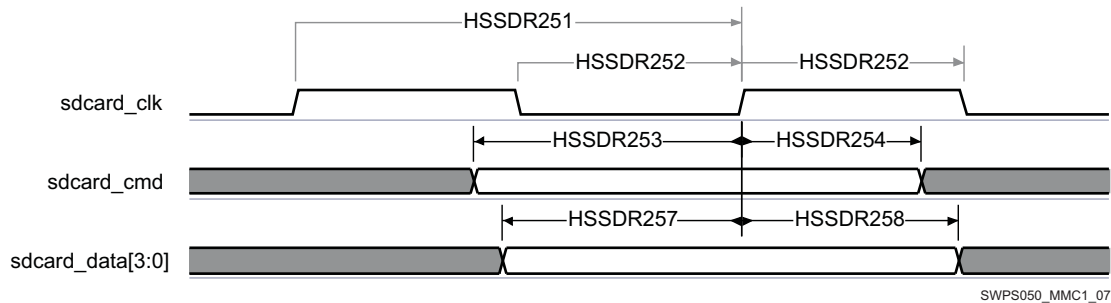
(1) See Section 4.3 for CORE OPP voltages.

Table 6-130. SDR25 SD Card Switching Characteristics—1.8 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|--------------------|--|-------------------------|------|------|
| | | | MIN | MAX | |
| HSSDR251 | $1 / t_{c}(clk)$ | Frequency, output sdcard_clk | | 48 | MHz |
| HSSDR252 | $t_{w}(clkH)$ | Typical pulse duration, output sdcard_clk high | $0.5 * P - 0.185^{(1)}$ | | ns |
| HSSDR252 | $t_{w}(clkL)$ | Typical pulse duration, output sdcard_clk low | $0.5 * P - 0.185^{(1)}$ | | ns |
| HSSDR255 | $t_{d}(clkL-cmdV)$ | Delay time, sdcard_clk falling edge to sdcard_cmd transition | -7.34 | 5.14 | ns |
| HSSDR256 | $t_{d}(clkL-doV)$ | Delay time, sdcard_clk falling edge to sdcard_data[3:0] transition | -7.34 | 5.14 | ns |

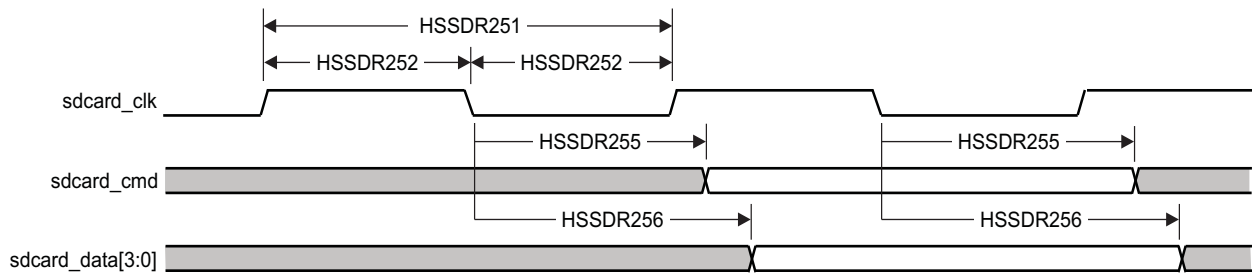
(1) P = output sdcard_clk period in ns

(2) See Section 4.3 for CORE OPP voltages.



SWPS050_MMC1_07

Figure 6-96. SDR25 SD Card, 1.8 V—Receiver Mode



SWPS050_MMC1_08

Figure 6-97. SDR25 SD Card, 1.8 V—Transmitter Mode

6.7.1.5 SD Card, UHS-I SDR50, 96 MHz, Half-Cycle Mode, 1.8 V

Table 6-131 and Table 6-132 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-131. UHS-I SDR50 SD Card Timing Requirements—1.8 V⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|---------------------|--|---------|-----|------|
| | | | MIN | MAX | |
| HSSDR503 | $t_{su(cmdV-clkH)}$ | Setup time, sdcard_cmd valid before sdcard_clk rising edge | 1.26 | | ns |
| HSSDR504 | $t_{h(clkH-cmdV)}$ | Hold time, sdcard_cmd valid after sdcard_clk rising edge | 1.6 | | ns |
| HSSDR507 | $t_{su(dV-clkH)}$ | Setup time, sdcard_data[3:0] valid before sdcard_clk rising edge | 1.26 | | ns |
| HSSDR508 | $t_{h(clkH-dV)}$ | Hold time, sdcard_data[3:0] valid after sdcard_clk rising edge | 1.6 | | ns |

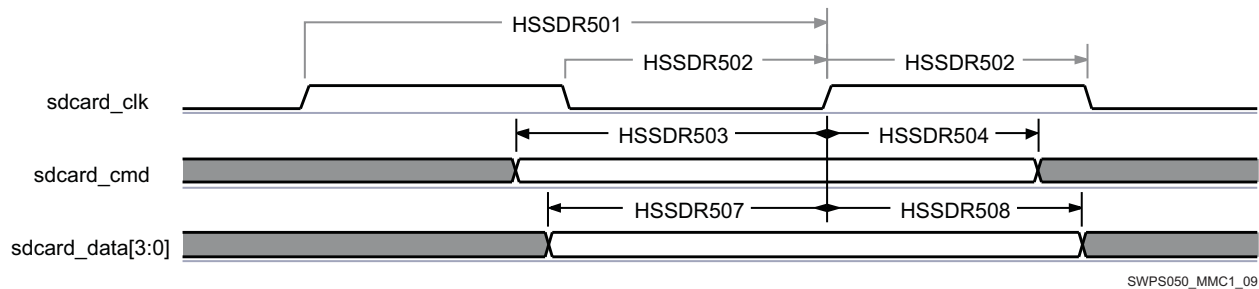
(1) See Section 4.3 for CORE OPP voltages.

Table 6-132. UHS-I SDR50 SD Card Switching Characteristics—1.8 V⁽²⁾

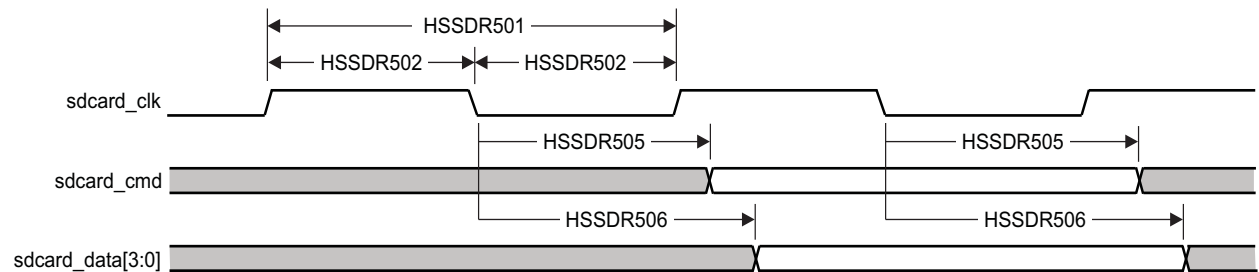
| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|--------------------|--|-------------------------|------|------|
| | | | MIN | MAX | |
| HSSDR501 | $1 / t_{c(clk)}$ | Frequency, output sdcard_clk | | 96 | MHz |
| HSSDR502 | $t_{w(clkH)}$ | Typical pulse duration, output sdcard_clk high | $0.5 * P - 0.185^{(1)}$ | | ns |
| HSSDR502 | $t_{w(clkL)}$ | Typical pulse duration, output sdcard_clk low | $0.5 * P - 0.185^{(1)}$ | | ns |
| HSSDR505 | $t_{d(clkL-cmdV)}$ | Delay time, sdcard_clk falling edge to sdcard_cmd transition | -2.68 | 0.48 | ns |
| HSSDR506 | $t_{d(clkL-dV)}$ | Delay time, sdcard_clk falling edge to sdcard_data[3:0] transition | -2.68 | 0.48 | ns |

(1) P = output sdcard_clk period in ns

(2) See Section 4.3 for CORE OPP voltages.



SWPS050_MMC1_09

Figure 6-98. UHS-I SDR50 SD Card, 1.8 V—Receiver Mode

SWPS050_MMC1_10

Figure 6-99. UHS-I SDR50 SD Card, 1.8 V—Transmitter Mode**6.7.1.6 SD Card, UHS-I SDR104, 192 MHz, Half-Cycle Mode, 1.8 V**

Table 6-133 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-133. UHS-I SDR104 SD Card Switching Characteristics—1.8 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----------|---------------------------|--|-------------------------|-------|------|
| | | | MIN | MAX | |
| HSSDR1041 | $1 / t_{c(\text{clk})}$ | Frequency, output sdcard_clk | | 192 | MHz |
| HSSDR1042 | $t_{w(\text{clkH})}$ | Typical pulse duration, output sdcard_clk high | $0.5 * P - 0.185^{(1)}$ | | ns |
| HSSDR1042 | $t_{w(\text{clkL})}$ | Typical pulse duration, output sdcard_clk low | $0.5 * P - 0.185^{(1)}$ | | ns |
| HSSDR1045 | $t_{d(\text{clkL-cmdV})}$ | Delay time, sdcard_clk falling edge to sdcard_cmd transition | -0.56 | -0.05 | ns |
| HSSDR1046 | $t_{d(\text{clkL-doV})}$ | Delay time, sdcard_clk falling edge to sdcard_data[3:0] transition | -0.56 | -0.05 | ns |

(1) P = output sdcard_clk period in ns.

(2) See Section 4.3 for CORE OPP voltages.

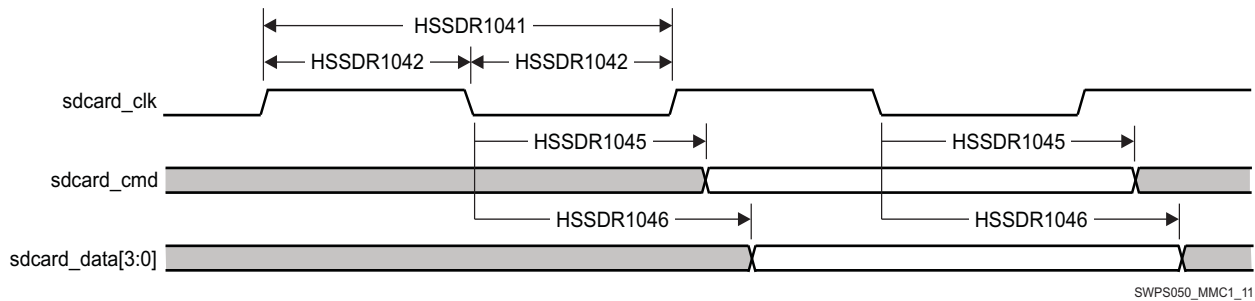


Figure 6-100. UHS-I SDR104 SD Card, 1.8 V—Transmitter Mode

6.7.1.7 SD Card, UHS-I DDR50, 48 MHz, Half-Cycle Mode, 1.8 V

Table 6-134 and Table 6-135 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-134. UHS-I DDR50 SD Card Timing Requirements—1.8 V⁽¹⁾

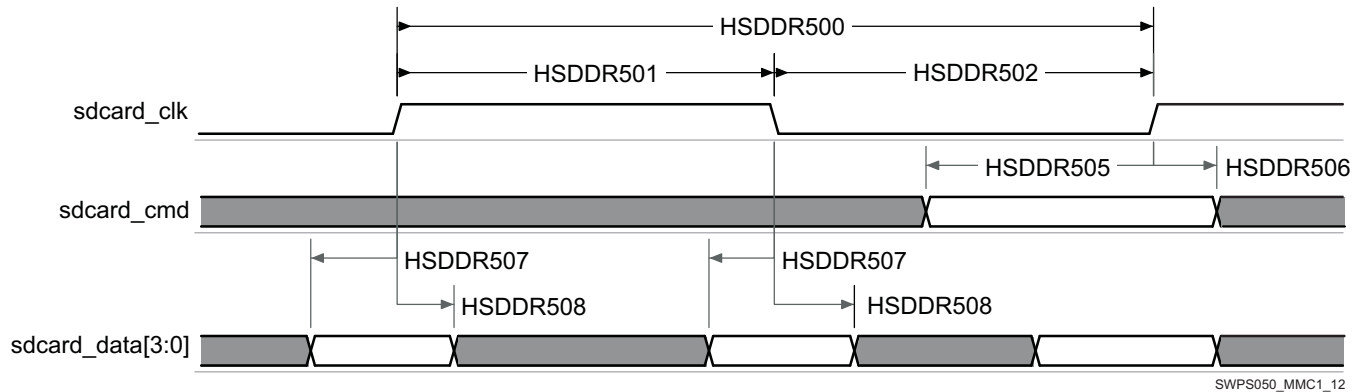
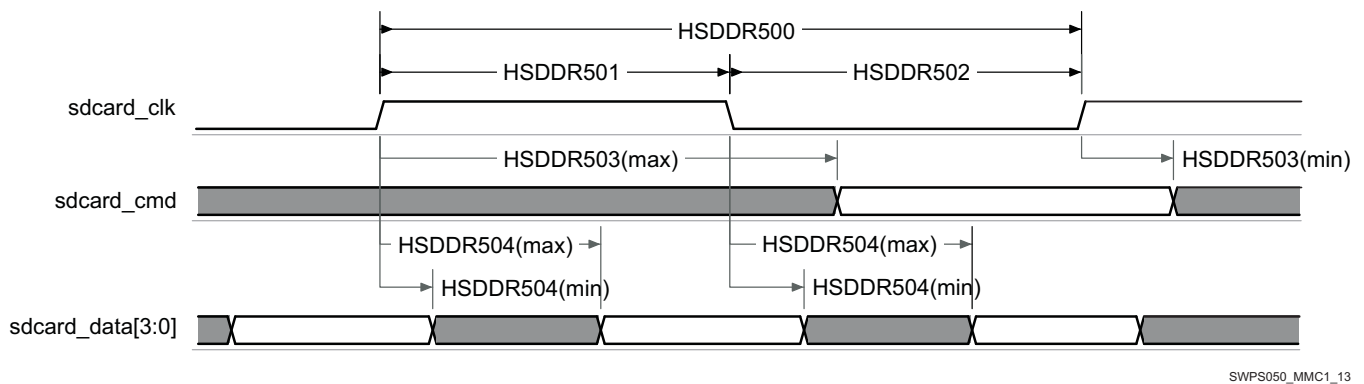
| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|----------------------------|---|---------|-----|------|
| | | | MIN | MAX | |
| HSDDR505 | $t_{su(\text{cmdV-clkH})}$ | Setup time, sdcard_cmd valid before sdcard_clk rising edge | 1.14 | | ns |
| HSDDR506 | $t_{h(\text{clkH-cmdV})}$ | Hold time, sdcard_cmd valid after sdcard_clk rising edge | 1.39 | | ns |
| HSDDR507 | $t_{su(\text{dV-clkH})}$ | Setup time, sdcard_data[3:0] valid before sdcard_clk rising or falling edge | 1.14 | | ns |
| HSDDR508 | $t_{h(\text{clkH-dV})}$ | Hold time, sdcard_data[3:0] valid after sdcard_clk rising or falling edge | 1.39 | | ns |

(1) See Section 4.3 for CORE OPP voltages.

Table 6-135. UHS-I DDR50 SD Card Switching Characteristics—1.8 V⁽²⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------|--------------------------|--|-------------------------|------|------|
| | | | MIN | MAX | |
| HSDDR500 | $1 / t_{c(\text{clk})}$ | Frequency, output sdcard_clk | | 48 | MHz |
| HSDDR501 | $t_{w(\text{clkH})}$ | Typical pulse duration, output sdcard_clk high | $0.5 * P - 0.185^{(1)}$ | | ns |
| HSDDR502 | $t_{w(\text{clkL})}$ | Typical pulse duration, output sdcard_clk low | $0.5 * P - 0.185^{(1)}$ | | ns |
| HSDDR503 | $t_{d(\text{clkL-doV})}$ | Delay time, sdcard_clk rising edge to sdcard_cmd transition | 2.61 | 15.6 | ns |
| HSDDR504 | $t_{d(\text{clkL-doV})}$ | Delay time, sdcard_clk rising or falling edge to sdcard_data[3:0] transition | 2.61 | 15.6 | ns |

- (1) P = output sdcard_clk period in ns
 (2) See Section 4.3 for CORE OPP voltages.

**Figure 6-101. UHS-I SDCard DDR, 1.8 V—Receiver Mode****Figure 6-102. UHS-I SDCard DDR, 1.8 V—Transmitter Mode**

6.8 Debug and Trace Interface, 1.8 V

6.8.1 JTAG Interface (JTAG)

The JTAG TAP controller handles standard IEEE JTAG interfaces. The following section defines the Timing requirements for several tools used to test the Device as:

- Free-running clock tool, like XDS560 and XDS510 tools
- Adaptive clock tool, like RealView® ICE tool and Lauterbach™ tool

6.8.1.1 JTAG—Free-Running Clock Mode

Table 6-137 and Table 6-138 assume testing over the recommended operating conditions and electrical characteristic conditions below .

Table 6-136. JTAG Timing Conditions—Free-running Clock Mode

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|-----|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 5 | | ns |
| t_F | Input signal fall time | 5 | | ns |
| PCB Conditions | | | | |
| | Far end load | | 30 | pF |

(1) In this table the rise and fall times are calculated for the VIL / VIH described in Table 4-24, Other Balls DC Electrical Characteristics.

Table 6-137. JTAG Timing Requirements—Free-running Clock Mode⁽⁴⁾⁽⁵⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|----------------------|---|----------------------|--------|------|
| | | | MIN | MAX | |
| JT4 | $1 / t_{c(tck)}$ | Frequency ⁽¹⁾ , input clock jtag_tck | | 13.5 | MHz |
| JT5 | $t_{w(tckL)}$ | Pulse duration, input clock jtag_tck low | $0.5 \times P^{(2)}$ | | ns |
| JT6 | $t_{w(tckH)}$ | Pulse duration, input clock jtag_tck high | $0.5 \times P^{(2)}$ | | ns |
| | $t_{dc(tck)}$ | Duty cycle error, input clock jtag_tck | | 3703.5 | ps |
| | $t_{j(tck)}$ | Cycle jitter ⁽³⁾ , input clock jtag_tck | | 3703.5 | ps |
| JT7 | $t_{su(tdiV-rtckH)}$ | Setup time, input data jtag_tdi valid before output clock jtag_rtck high | 1.8 | | ns |
| JT8 | $t_{h(tdiV-rtckH)}$ | Hold time, input data jtag_tdi valid after output clock jtag_rtck high | 0.7 | | ns |
| JT9 | $t_{su(tmsV-rtckH)}$ | Setup time, input mode select jtag_tms_tmssc valid before output clock jtag_rtck high | 1.8 | | ns |
| JT10 | $t_{h(tmsV-rtckH)}$ | Hold time, input mode select jtag_tms_tmssc valid after output clock jtag_rtck high | 0.7 | | ns |

(1) Related to the input maximum frequency supported by the JTAG module.

(2) $P = jtag_tck$ period in ns

(3) Maximum cycle jitter supported by jtag_tck input clock.

(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(5) See Section 4.3 for CORE OPP voltages.

Table 6-138. JTAG Switching Characteristics—Free-running Clock Mode⁽⁴⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|---------------------|--|-----------------------|--------|------|
| | | | MIN | MAX | |
| JT1 | $1 / t_{c(rtck)}$ | Frequency ⁽¹⁾ , output clock jtag_rtck | | 13.5 | MHz |
| JT2 | $t_{w(rtckL)}$ | Pulse duration, output clock jtag_rtck low | $0.5 \times PO^{(2)}$ | | ns |
| JT3 | $t_{w(rtckH)}$ | Pulse duration, output clock jtag_rtck high | $0.5 \times PO^{(2)}$ | | ns |
| | $t_{dc(rtck)}$ | Duty cycle error, output clock jtag_rtck | | 3703.5 | ps |
| | $t_{j(rtck)}$ | Jitter standard deviation ⁽³⁾ , output clock jtag_rtck | | 33.3 | ps |
| | $t_{R(rtck)}$ | Rise time, output clock jtag_rtck | | 4.0 | ns |
| | $t_{F(rtck)}$ | Fall time, output clock jtag_rtck | | 4.0 | ns |
| JT11 | $t_{d(rtckL-tdoV)}$ | Delay time, output clock jtag_rtck low to output data jtag_tdo valid | | 5.8 | ns |
| | $t_{R(tdo)}$ | Rise time, output data jtag_tdo | | 4.0 | ns |
| | $t_{F(tdo)}$ | Fall time, output data jtag_tdo | | 4.0 | ns |

- (1) Related to the jtag_rtkc maximum frequency.
- (2) $PO = \text{jtag_rtck period in ns}$
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) See [Section 4.3](#) for CORE OPP voltages.

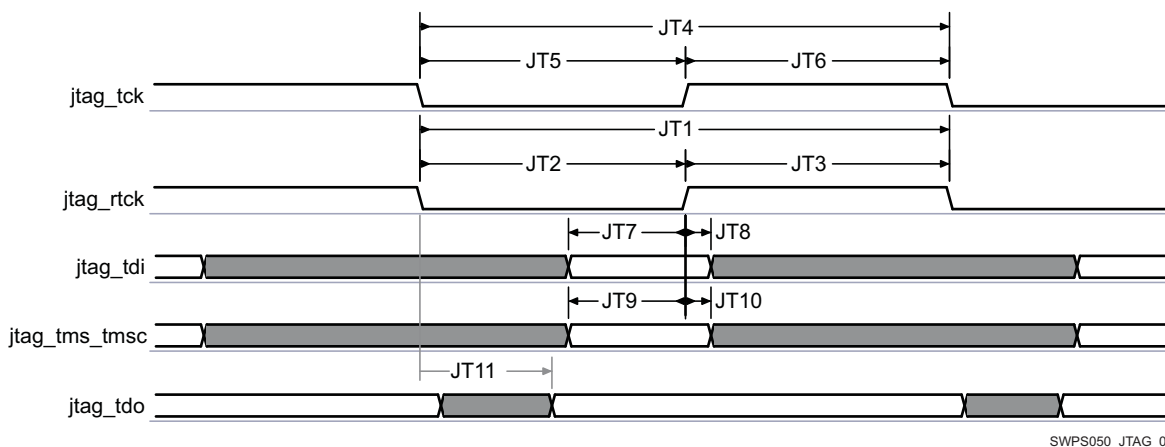


Figure 6-103. JTAG Interface Timing—Free-running Clock Mode

6.8.1.2 JTAG—Adaptive Clock Mode - JTAG interface

[Table 6-140](#) and [Table 6-141](#) assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 6-139. JTAG Timing Conditions—Adaptive Clock Mode - JTAG interface

| TIMING CONDITION PARAMETER | | OPP_NOM | | UNIT |
|----------------------------|------------------------|---------|-----|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | 5 | | ns |
| t_F | Input signal fall time | 5 | | ns |
| PCB Conditions | | | | |
| | Far end load | | 30 | pF |

(1) In this table the rise and fall times are calculated for the V_{IL} / V_{IH} described in [Table 4-24](#), Other Balls DC Electrical Characteristics.

Table 6-140. JTAG Timing Requirements—Adaptive Clock Mode - JTAG interface⁽⁴⁾⁽⁵⁾

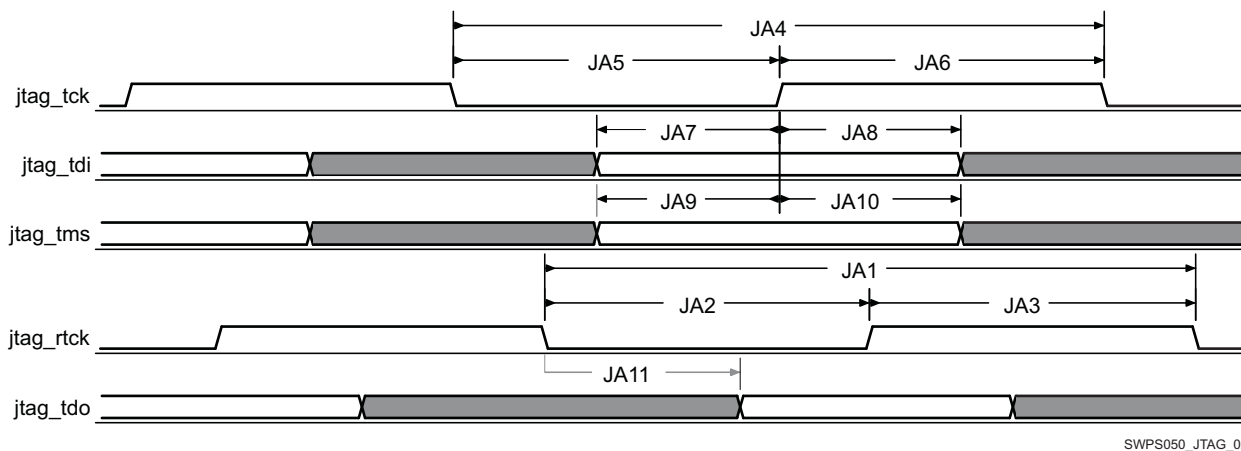
| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|----------------------------|--|----------------------|--------|------|
| | | | MIN | MAX | |
| JA4 | $1 / t_c(\text{tck})$ | Frequency ⁽¹⁾ , input clock jtag_tck | | 15 | MHz |
| JA5 | $t_w(\text{tckL})$ | Pulse duration, input clock jtag_tck low | $0.5 \times P^{(2)}$ | | ns |
| JA6 | $t_w(\text{tckH})$ | Pulse duration, input clock jtag_tck high | $0.5 \times P^{(2)}$ | | ns |
| | $t_{dc}(\text{lclk})$ | Duty cycle error, input clock jtag_tck | | 3333.0 | ps |
| | $t_j(\text{lclk})$ | Cycle jitter ⁽³⁾ , input clock jtag_tck | | 2000.0 | ps |
| JA7 | $t_{su}(\text{tdiV-tckH})$ | Setup time, input data jtag_tdi valid before input clock jtag_tck high | 13.8 | | ns |
| JA8 | $t_h(\text{tdiV-tckH})$ | Hold time, input data jtag_tdi valid after input clock jtag_tck high | 13.8 | | ns |
| JA9 | $t_{su}(\text{tmsV-tckH})$ | Setup time, jtag_tms valid before jtag_tck high | 13.8 | | ns |
| JA10 | $t_h(\text{tmsV-tckH})$ | Hold time, jtag_tms valid after jtag_tck high | 13.8 | | ns |

- (1) Related to the input maximum frequency supported by the JTAG module.
- (2) $P = \text{jtag_tck}$ period in ns
- (3) Maximum cycle jitter supported by jtag_tck input clock.
- (4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
- (5) See Section 4.3 for CORE OPP voltages.

Table 6-141. JTAG Switching Characteristics—Adaptive Clock Mode - JTAG interface⁽⁴⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|----------------------------|--|-----------------------|--------|------|
| | | | MIN | MAX | |
| JA1 | $1 / t_{c(\text{rtck})}$ | Frequency ⁽¹⁾ , output clock jtag_rtck | | 15 | MHz |
| JA2 | $t_{w(\text{rtckL})}$ | Pulse duration, output clock jtag_rtck low | $0.5 \times PO^{(2)}$ | | ns |
| JA3 | $t_{w(\text{rtckH})}$ | Pulse duration, output clock jtag_rtck high | $0.5 \times PO^{(2)}$ | | ns |
| | $t_{dc(\text{rtck})}$ | Duty cycle error, output clock jtag_rtck | -3333.0 | 3333.0 | ps |
| | $t_{j(\text{rtck})}$ | Jitter standard deviation ⁽³⁾ , output clock jtag_rtck | | 33.3 | ps |
| | $t_{R(\text{rtck})}$ | Rise time, output clock jtag_rtck | | 4.0 | ns |
| | $t_{F(\text{rtck})}$ | Fall time, output clock jtag_rtck | | 4.0 | ns |
| JA11 | $t_{d(\text{rtckL-tdoV})}$ | Delay time, output clock jtag_rtck low to output data jtag_tdo valid | -14.6 | 14.6 | ns |
| | $t_{R(\text{tdo})}$ | Rise time, output data jtag_tdo | | 4.0 | ns |
| | $t_{F(\text{tdo})}$ | Fall time, output data jtag_tdo | | 4.0 | ns |

- (1) Related to the jtag_rtck maximum frequency.
- (2) $PO = \text{jtag_rtck}$ period in ns
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) See Section 4.3 for CORE OPP voltages.



SWPS050_JTAG_02

Figure 6-104. JTAG Interface Timing—Adaptive Clock Mode - JTAG interface

6.8.1.3 JTAG—Adaptive Clock Mode - SD Card Interface (MIPI NIDnT)

Table 6-143 and Table 6-144 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 6-142. JTAG Timing Conditions—Adaptive Clock Mode - SD Card Interface (MIPI NIDnT)

| TIMING CONDITION PARAMETER | | OPP_NOM | | UNIT |
|----------------------------|------------------------|---------|-----|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t_R | Input signal rise time | | 5 | ns |
| t_F | Input signal fall time | | 5 | ns |

Table 6-142. JTAG Timing Conditions—Adaptive Clock Mode - SD Card Interface (MIPI NIDnT) (continued)

| TIMING CONDITION PARAMETER | | OPP_NOM | | UNIT |
|----------------------------|--------------|---------|-----|------|
| | | MIN | MAX | |
| PCB Conditions | | | | |
| | Far end load | | 30 | pF |

(1) In this table the rise and fall times are calculated for the V_{IL} / V_{IH} described in Table 4-24, Other Balls DC Electrical Characteristics.

Table 6-143. JTAG Timing Requirements—Adaptive Clock Mode - SD Card Interface (MIPI NIDnT)⁽⁴⁾⁽⁵⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|---------------------|--|----------------------|--------|------|
| | | | MIN | MAX | |
| JA4 | $1 / t_c(tck)$ | Frequency ⁽¹⁾ , input clock jtag_tck | | 15 | MHz |
| JA5 | $t_w(tckL)$ | Pulse duration, input clock jtag_tck low | $0.5 \times P^{(2)}$ | | ns |
| JA6 | $t_w(tckH)$ | Pulse duration, input clock jtag_tck high | $0.5 \times P^{(2)}$ | | ns |
| | $t_{dc}(lclk)$ | Duty cycle error, input clock jtag_tck | | 3333.0 | ps |
| | $t_j(lclk)$ | Cycle jitter ⁽³⁾ , input clock jtag_tck | | 2000.0 | ps |
| JA7 | $t_{su}(tdiV-tckH)$ | Setup time, input data jtag_tdi valid before input clock jtag_tck high | 13.8 | | ns |
| JA8 | $t_h(tdiV-tckH)$ | Hold time, input data jtag_tdi valid after input clock jtag_tck high | 13.8 | | ns |
| JA9 | $t_{su}(tmsV-tckH)$ | Setup time, jtag_tms valid before jtag_tck high | 13.8 | | ns |
| JA10 | $t_h(tmsV-tckH)$ | Hold time, jtag_tms valid after jtag_tck high | 13.8 | | ns |

(1) Related to the input maximum frequency supported by the JTAG module.

(2) P = jtag_tck period in ns

(3) Maximum cycle jitter supported by jtag_tck input clock.

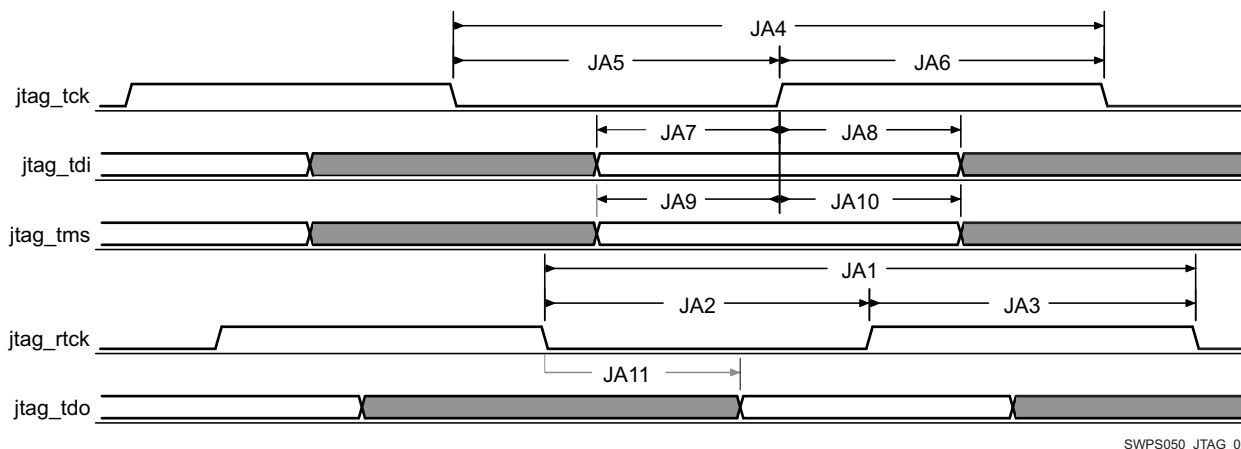
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(5) See Section 4.3 for CORE OPP voltages.

Table 6-144. JTAG Switching Characteristics—Adaptive Clock Mode - SD Card Interface (MIPI NIDnT)⁽⁴⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|-------------------|--|-----------------------|--------|------|
| | | | MIN | MAX | |
| JA1 | $1 / t_c(rtck)$ | Frequency ⁽¹⁾ , output clock jtag_rtck | | 15 | MHz |
| JA2 | $t_w(rtckL)$ | Pulse duration, output clock jtag_rtck low | $0.5 \times PO^{(2)}$ | | ns |
| JA3 | $t_w(rtckH)$ | Pulse duration, output clock jtag_rtck high | $0.5 \times PO^{(2)}$ | | ns |
| | $t_{dc}(rtck)$ | Duty cycle error, output clock jtag_rtck | -3333.0 | 3333.0 | ps |
| | $t_j(rtck)$ | Jitter standard deviation ⁽³⁾ , output clock jtag_rtck | | 33.3 | ps |
| | $t_R(rtck)$ | Rise time, output clock jtag_rtck | | 4.0 | ns |
| | $t_F(rtck)$ | Fall time, output clock jtag_rtck | | 4.0 | ns |
| JA11 | $t_d(rtckL-tdoV)$ | Delay time, output clock jtag_rtck low to output data jtag_tdo valid | -14.6 | 14.6 | ns |
| | $t_R(tdo)$ | Rise time, output data jtag_tdo | | 4.0 | ns |
| | $t_F(tdo)$ | Fall time, output data jtag_tdo | | 4.0 | ns |

- (1) Related to the jtag_rtk maximum frequency.
- (2) PO = jtag_rtk period in ns
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) See Section 4.3 for CORE OPP voltages.



SWPS050_JTAG_02

Figure 6-105. JTAG Interface Timing—Adaptive Clock Mode - SD Card Interface (MIPI NIDnT)

6.8.2 cJTAG Interface (cJTAG)

The cJTAG module is a component which can run a 2-pin communication protocol on top of an IEEE 1149.1 JTAG Test Access Port (TAP). The cJTAG logic serializes the IEEE 1149.1 transactions, using a variety of compression formats, to reduce the number of pins needed to implement a JTAG debug and boundary scan port. The Device platform implements only a basic 3-pin scan configuration.

Table 6-146 and Table 6-147 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-106).

Table 6-145. cJTAG Timing Conditions—Normal Mode

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|----------------------------|------------------------|-------|-----|------|
| | | MIN | MAX | |
| Input Conditions | | | | |
| t _R | Input signal rise time | | 2 | ns |
| t _F | Input signal fall time | | 2 | ns |
| PCB Conditions | | | | |
| | Far end load | | 30 | pF |

(1) In this table the rise and fall times are calculated for the V_{IL} / V_{IH} described in Table 4-24, Other Balls DC Electrical Characteristics.

Table 6-146. cJTAG Timing Requirements—Normal Mode⁽⁴⁾⁽⁵⁾

| NO. | PARAMETER | OPP_NOM | | UNIT |
|---------------------|-----------------------------|---|--|------|
| | | MIN | MAX | |
| For MMC PADS | | | | |
| CJ1 | 1 / t _{c(tck)} | Frequency ⁽¹⁾ , input clock jtag_tck | | MHz |
| CJ2 | t _{w(tckL)} | Pulse duration, input clock jtag_tck low | | ns |
| CJ3 | t _{w(tckH)} | Pulse duration, input clock jtag_tck high | | ns |
| | t _{dc(tck)} | | Duty cycle error, input clock jtag_tck | ps |
| | t _{j(tck)} | | Cycle jitter ⁽³⁾ , input clock jtag_tck | ps |
| CJ4 | t _{su(tmscV-tckL)} | 3.8 | Setup time, input mode select jtag_tms_tmisc valid before input clock jtag_tck low | ns |

Table 6-146. cJTAG Timing Requirements—Normal Mode⁽⁴⁾⁽⁵⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|----------------------|------------------------------------|--|----------------------|--------|------|
| | | | MIN | MAX | |
| CJ5 | $t_{h(\text{tm}scV\text{-tckL})}$ | Hold time, input mode select jtag_tms_tmisc valid after input clock jtag_tck low | 1.4 | | ns |
| For JTAG PADS | | | | | |
| CJ1 | $t_{c(\text{tck})}$ | Frequency ⁽¹⁾ , input clock jtag_tck | | 27 | MHz |
| CJ2 | $t_{w(\text{tckL})}$ | Pulse duration, input clock jtag_tck low | $0.5 \times P^{(2)}$ | | ns |
| CJ3 | $t_{w(\text{tckH})}$ | Pulse duration, input clock jtag_tck high | $0.5 \times P^{(2)}$ | | ns |
| | $t_{dc(\text{tck})}$ | Duty cycle error, input clock jtag_tck | -2222.2 | 2222.2 | ps |
| | $t_{j(\text{tck})}$ | Cycle jitter ⁽³⁾ , input clock jtag_tck | -2222.2 | 2222.2 | ps |
| CJ4 | $t_{su(\text{tm}scV\text{-tckL})}$ | Setup time, input mode select jtag_tms_tmisc valid before input clock jtag_tck low | 3.8 | | ns |
| CJ5 | $t_{h(\text{tm}scV\text{-tckL})}$ | Hold time, input mode select jtag_tms_tmisc valid after input clock jtag_tck low | 1.4 | | ns |

(1) Related to the input maximum frequency supported by the JTAG module.

(2) P = jtag_tck period in ns

(3) Maximum cycle jitter supported by jtag_tck input clock.

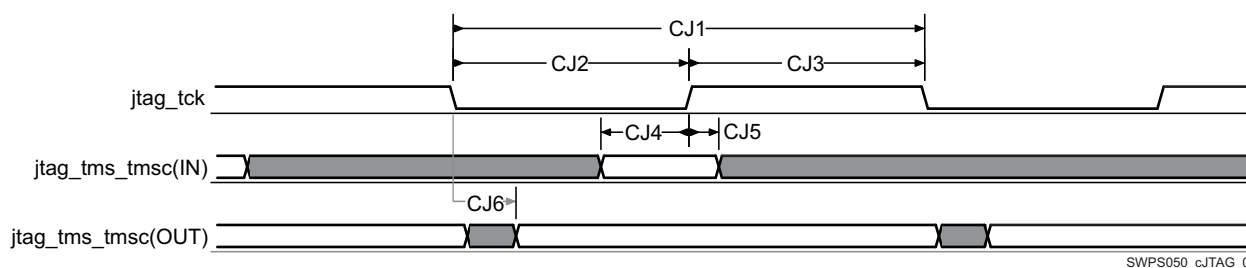
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(5) See [Section 4.3](#) for CORE OPP voltages.

Table 6-147. cJTAG Switching Characteristics—Normal Mode⁽¹⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-----|-----------------------------------|---|---------|-----|------|
| | | | MIN | MAX | |
| CJ6 | $t_{d(\text{tckL}\text{-tm}scV)}$ | Delay time, input clock jtag_tck low to output mode select jtag_tms_tmisc valid | 1.2 | 6.2 | ns |
| | $t_{R(\text{tm}sc)}$ | Rise time, output mode select jtag_tms_tmisc | | 4.0 | ns |
| | $t_{F(\text{tm}sc)}$ | Fall time, output mode select jtag_tms_tmisc | | 4.0 | ns |

(1) See [Section 4.3](#) for CORE OPP voltages.



SWPS050_cJTAG_01

Figure 6-106. cJTAG Interface Timing—Normal Mode

6.8.3 Trace Port Interface Unit (TPIU)

The TPIU PTM (Trace Port Interface Unit PTM) specific to MPU trace is available on the DRM interface (Debug Resource Manager).

6.8.3.1 TPIU PTM, DDR, 180 MHz, 16-bit data, for Lauterbach LA-7992 emulator

[Table 6-148](#) assumes testing over the recommended operating conditions and electrical characteristic conditions below .

Table 6-148. TPIU PTM Switching Characteristics⁽⁴⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|---------------------------|---|----------------------|-------|------|
| | | | MIN | MAX | |
| TPIU1 | $1 / t_{c(\text{clk})}$ | Frequency ⁽¹⁾ , output clock atpiu_clk | | 180 | MHz |
| TPIU2 | $t_{w(\text{clkH})}$ | Pulse duration, output clock atpiu_clk high | $0.5 \times P^{(2)}$ | | ns |
| TPIU3 | $t_{w(\text{clkL})}$ | Pulse duration, output clock atpiu_clk low | $0.5 \times P^{(2)}$ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output clock atpiu_clk | | 278 | ps |
| | $t_{j(\text{clk})}$ | Jitter standard deviation ⁽³⁾ , output clock atpiu_clk | | 36 | ps |
| | $t_{R(\text{clk})}$ | Rise time, output clock atpiu_clk | | 1.03 | ns |
| | $t_{F(\text{clk})}$ | Fall time, output clock atpiu_clk | | 1.03 | ns |
| TPIU4 | $t_{d(\text{clk-ctlV})}$ | Delay time, output clock atpiu_clk low/high to output control atpiu_cntl transition | | 0.957 | ns |
| TPIU5 | $t_{d(\text{clk-dataV})}$ | Delay time, output clock atpiu_clk low/high to output data atpiu_d[n:0] transition | | 0.957 | ns |
| | $t_{R(\text{DO})}$ | Rise time, output data atpiu_d[n:0] and output control atpiu_cntl | | 1.03 | ns |
| | $t_{F(\text{DO})}$ | Fall time, output data atpiu_d[n:0] and output control atpiu_cntl | | 1.03 | ns |

- (1) Related to the atpiu_clk maximum frequency.
- (2) $P = \text{atpiu_clk period in ns}$
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) See Section 4.3 for CORE OPP voltages.

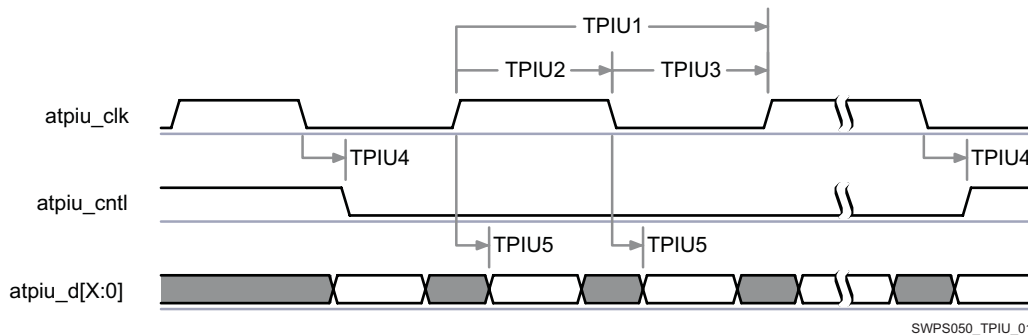


Figure 6-107. TPIU PTM DDR Transmit Mode

6.8.3.2 TPIU PTM, DDR, 180 MHz, 16-bit data, for XDS560v2 emulator

Table 6-149 assumes testing over the recommended operating conditions and electrical characteristic conditions below .

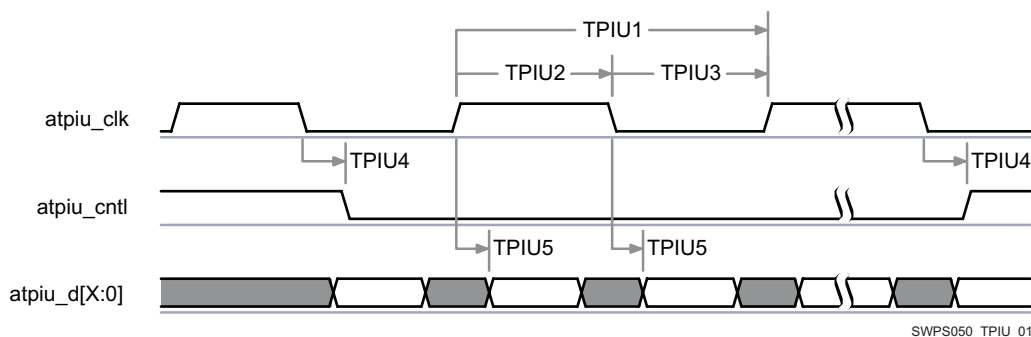
Table 6-149. TPIU PTM Switching Characteristics⁽⁴⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|--------------------------|---|----------------------|-------|------|
| | | | MIN | MAX | |
| TPIU1 | $1 / t_{c(\text{clk})}$ | Frequency ⁽¹⁾ , output clock atpiu_clk | | 180 | MHz |
| TPIU2 | $t_{w(\text{clkH})}$ | Pulse duration, output clock atpiu_clk high | $0.5 \times P^{(2)}$ | | ns |
| TPIU3 | $t_{w(\text{clkL})}$ | Pulse duration, output clock atpiu_clk low | $0.5 \times P^{(2)}$ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output clock atpiu_clk | | 278 | ps |
| | $t_{j(\text{clk})}$ | Jitter standard deviation ⁽³⁾ , output clock atpiu_clk | | 36 | ps |
| | $t_{R(\text{clk})}$ | Rise time, output clock atpiu_clk | | 1.01 | ns |
| | $t_{F(\text{clk})}$ | Fall time, output clock atpiu_clk | | 1.01 | ns |
| TPIU4 | $t_{d(\text{clk-ctlV})}$ | Delay time, output clock atpiu_clk low/high to output control atpiu_cntl transition | | 0.984 | ns |

Table 6-149. TPIU PTM Switching Characteristics⁽⁴⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|-------|---------------------------|--|---------|-------|------|
| | | | MIN | MAX | |
| TPIU5 | $t_{d(\text{clk-dataV})}$ | Delay time, output clock atpiu_clk low/high to output data atpiu_d[n:0] transition | | 0.984 | ns |
| | $t_{R(\text{DO})}$ | Rise time, output data atpiu_d[n:0] and output control atpiu_cntl | | 1.01 | ns |
| | $t_{F(\text{DO})}$ | Fall time, output data atpiu_d[n:0] and output control atpiu_cntl | | 1.01 | ns |

- (1) Related to the atpiu_clk maximum frequency.
(2) P = atpiu_clk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) See [Section 4.3](#) for CORE OPP voltages.



SWPS050_TPIU_01

Figure 6-108. TPIU PTM DDR Transmit Mode

6.8.4 System Trace Module Interface (STM)

The STM (System trace module) for hardware and software system events is available on the DRM interface (Debug Resource Manager) and SD Card Interface (MIPI NIDnT).

6.8.4.1 MIPI STMv1

[Table 6-150](#) presents STMv1 - 72 MHz SD Card Interface parameters for XDS560v2 and assumes testing over the recommended operating and electrical characteristic conditions.

Table 6-150. STMv1 Switching Characteristics – 72 MHz SD Card Interface⁽⁴⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|---------------------------|--|----------------------|-------|------|
| | | | MIN | MAX | |
| STM1 | $1 / t_{c(\text{clk})}$ | Frequency ⁽¹⁾ , output clock astm_clk | | 100 | MHz |
| STM2 | $t_{w(\text{clkH})}$ | Pulse duration, output clock astm_clk high | $0.5 \times P^{(2)}$ | | ns |
| STM3 | $t_{w(\text{clkL})}$ | Pulse duration, output clock astm_clk low | $0.5 \times P^{(2)}$ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output clock astm_clk | | 694 | ps |
| | $t_{j(\text{clk})}$ | Jitter standard deviation ⁽³⁾ , output clock astm_clk | | 90 | ps |
| | $t_{R(\text{clk})}$ | Rise time, output clock astm_clk | | 1.85 | ns |
| | $t_{F(\text{clk})}$ | Fall time, output clock astm_clk | | 1.85 | ns |
| STM4 | $t_{d(\text{clk-dataV})}$ | Delay time, output clock astm_clk low/high to output control astm_d[3:0] valid | 1.88 | 3.977 | ns |
| | $t_{R(\text{DO})}$ | Rise time, output data astm_d[3:0] | | 1.85 | ns |
| | $t_{F(\text{DO})}$ | Fall time, output data astm_d[3:0] | | 1.85 | ns |

- (1) Related to the astm_clk maximum frequency.
- (2) P = astm_clk period in ns
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) See [Section 4.3](#) for CORE OPP voltages.

Table 6-151 presents STMv1 - 80 MHz SD Card Interface parameters for XDS560v2 and assumes testing over the recommended operating and electrical characteristic conditions.

Table 6-151. STMv1 Switching Characteristics – 80 MHz SD Card Interface ⁽⁴⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|---------------------------|--|------------------------|-------|------|
| | | | MIN | MAX | |
| STM1 | $1 / t_{c(\text{clk})}$ | Frequency ⁽¹⁾ , output clock astm_clk | | 80 | MHz |
| STM2 | $t_{w(\text{clkH})}$ | Pulse duration, output clock astm_clk high | 0.5 × P ⁽²⁾ | | ns |
| STM3 | $t_{w(\text{clkL})}$ | Pulse duration, output clock astm_clk low | 0.5 × P ⁽²⁾ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output clock astm_clk | | 625 | ps |
| | $t_{j(\text{clk})}$ | Jitter standard deviation ⁽³⁾ , output clock astm_clk | | 81 | ps |
| | $t_{R(\text{clk})}$ | Rise time, output clock astm_clk | | 1.85 | ns |
| | $t_{F(\text{clk})}$ | Fall time, output clock astm_clk | | 1.85 | ns |
| STM4 | $t_{d(\text{clk-dataV})}$ | Delay time, output clock astm_clk low/high to output control astm_d[3:0] valid | 1.852 | 3.419 | ns |
| | $t_{R(\text{DO})}$ | Rise time, output data astm_d[3:0] | | 1.85 | ns |
| | $t_{F(\text{DO})}$ | Fall time, output data astm_d[3:0] | | 1.85 | ns |

- (1) Related to the astm_clk maximum frequency.
- (2) P = astm_clk period in ns
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) See [Section 4.3](#) for CORE OPP voltages.

Table 6-152 presents STMv1 - 72 MHz DRM Interface parameters for XDS560v2 and assumes testing over the recommended operating and electrical characteristic conditions.

Table 6-152. STMv1 Switching Characteristics – DRM Interface ⁽⁴⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|---------------------------|--|------------------------|-------|------|
| | | | MIN | MAX | |
| STM1 | $1 / t_{c(\text{clk})}$ | Frequency ⁽¹⁾ , output clock astm_clk | | 80 | MHz |
| STM2 | $t_{w(\text{clkH})}$ | Pulse duration, output clock astm_clk high | 0.5 × P ⁽²⁾ | | ns |
| STM3 | $t_{w(\text{clkL})}$ | Pulse duration, output clock astm_clk low | 0.5 × P ⁽²⁾ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output clock astm_clk | | 625 | ps |
| | $t_{j(\text{clk})}$ | Jitter standard deviation ⁽³⁾ , output clock astm_clk | | 81 | ps |
| | $t_{R(\text{clk})}$ | Rise time, output clock astm_clk | | 1.73 | ns |
| | $t_{F(\text{clk})}$ | Fall time, output clock astm_clk | | 1.73 | ns |
| STM4 | $t_{d(\text{clk-dataV})}$ | Delay time, output clock astm_clk low/high to output control astm_d[3:0] valid | 1.859 | 3.413 | ns |
| | $t_{R(\text{DO})}$ | Rise time, output data astm_d[3:0] | | 1.73 | ns |
| | $t_{F(\text{DO})}$ | Fall time, output data astm_d[3:0] | | 1.73 | ns |

- (1) Related to the astm_clk maximum frequency.
- (2) P = astm_clk period in ns
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) See [Section 4.3](#) for CORE OPP voltages.

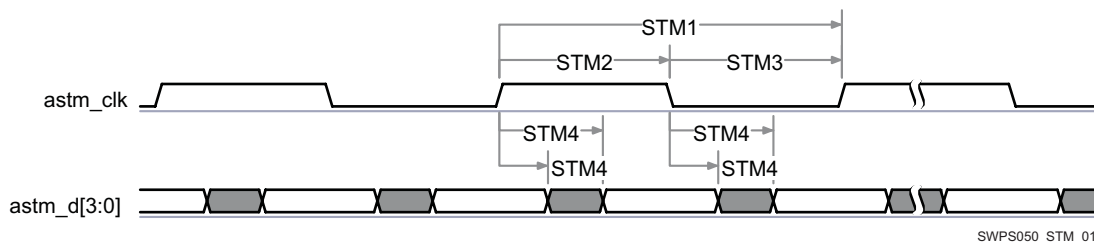


Figure 6-109. STMv1 - Transmit Mode

6.8.4.2 MIPI STMv2

[Table 6-153](#) presents STMv2 – 180MHz DRM Interface parameters for XDS560v2 and assumes testing over the recommended operating and electrical characteristic conditions.

Table 6-153. STMv2 Switching Characteristics – DRM Interface for XDS560v2 ⁽⁴⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|---------------------------|--|----------------------|------|------|
| | | | MIN | MAX | |
| STM1 | $1 / t_{c(\text{clk})}$ | Frequency ⁽¹⁾ , output clock astm_clk | | 180 | MHz |
| STM2 | $t_{w(\text{clkH})}$ | Pulse duration, output clock astm_clk high | $0.5 \times P^{(2)}$ | | ns |
| STM3 | $t_{w(\text{clkL})}$ | Pulse duration, output clock astm_clk low | $0.5 \times P^{(2)}$ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output clock astm_clk | | 278 | ps |
| | $t_{j(\text{clk})}$ | Jitter standard deviation ⁽³⁾ , output clock astm_clk | | 36 | ps |
| | $t_{R(\text{clk})}$ | Rise time, output clock astm_clk | | 1.03 | ns |
| | $t_{F(\text{clk})}$ | Fall time, output clock astm_clk | | 1.03 | ns |
| STM4 | $t_{d(\text{clk-dataV})}$ | Delay time, output clock astm_clk low/high to output control astm_d[3:0] valid | 0.623 | 1.72 | ns |
| | $t_{R(\text{DO})}$ | Rise time, output data astm_d[3:0] | | 1.03 | ns |
| | $t_{F(\text{DO})}$ | Fall time, output data astm_d[3:0] | | 1.03 | ns |

- (1) Related to astm_clk maximum frequency.
- (2) P = astm_clk period in ns
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) See [Section 4.3](#) for CORE OPP voltages.

[Table 6-154](#) presents STMv2 – 150MHz SD Card Interface parameters for XDS560v2 and assumes testing over the recommended operating and electrical characteristic conditions.

Table 6-154. Switching Characteristics –SD Card Interface for XDS560v2 ⁽⁴⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|-------------------------|--|----------------------|------|------|
| | | | MIN | MAX | |
| STM1 | $1 / t_{c(\text{clk})}$ | Frequency ⁽¹⁾ , output clock astm_clk | | 150 | MHz |
| STM2 | $t_{w(\text{clkH})}$ | Pulse duration, output clock astm_clk high | $0.5 \times P^{(2)}$ | | ns |
| STM3 | $t_{w(\text{clkL})}$ | Pulse duration, output clock astm_clk low | $0.5 \times P^{(2)}$ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output clock astm_clk | | 333 | ps |
| | $t_{j(\text{clk})}$ | Jitter standard deviation ⁽³⁾ , output clock astm_clk | | 43 | ps |
| | $t_{R(\text{clk})}$ | Rise time, output clock astm_clk | | 1.83 | ns |
| | $t_{F(\text{clk})}$ | Fall time, output clock astm_clk | | 1.83 | ns |

Table 6-154. Switching Characteristics –SD Card Interface for XDS560v2 ⁽⁴⁾ (continued)

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|---------------------------|--|---------|-------|------|
| | | | MIN | MAX | |
| STM4 | $t_{d(\text{clk-dataV})}$ | Delay time, output clock astm_clk low/high to output control astm_d[3:0] valid | 1.059 | 1.819 | ns |
| | $t_{R(\text{DO})}$ | Rise time, output data astm_d[3:0] | | 1.83 | ns |
| | $t_{F(\text{DO})}$ | Fall time, output data astm_d[3:0] | | 1.83 | ns |

- (1) Related to astm_clk maximum frequency.
 (2) P = astm_clk period in ns
 (3) The jitter probability density can be approximated by a Gaussian function.
 (4) See [Section 4.3](#) for CORE OPP voltages.

[Table 6-155](#) presents STMv2 – 180MHz DRM Interface parameters for Lauterbach LA-7992 and assumes testing over the recommended operating and electrical characteristic conditions.

Table 6-155. STMv2 Switching Characteristics – DRM Interface for Lauterbach LA-7992 ⁽⁴⁾

| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|---------------------------|--|----------------------|-------|------|
| | | | MIN | MAX | |
| STM1 | $1 / t_{c(\text{clk})}$ | Frequency ⁽¹⁾ , output clock astm_clk | | 180 | MHz |
| STM2 | $t_{w(\text{clkH})}$ | Pulse duration, output clock astm_clk high | $0.5 \times P^{(2)}$ | | ns |
| STM3 | $t_{w(\text{clkL})}$ | Pulse duration, output clock astm_clk low | $0.5 \times P^{(2)}$ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output clock astm_clk | | 278 | ps |
| | $t_{j(\text{clk})}$ | Jitter standard deviation ⁽³⁾ , output clock astm_clk | | 36 | ps |
| | $t_{R(\text{clk})}$ | Rise time, output clock astm_clk | | 1.03 | ns |
| | $t_{F(\text{clk})}$ | Fall time, output clock astm_clk | | 1.03 | ns |
| STM4 | $t_{d(\text{clk-dataV})}$ | Delay time, output clock astm_clk low/high to output control astm_d[3:0] valid | 1.059 | 1.384 | ns |
| | $t_{R(\text{DO})}$ | Rise time, output data astm_d[3:0] | | 1.03 | ns |
| | $t_{F(\text{DO})}$ | Fall time, output data astm_d[3:0] | | 1.03 | ns |

- (1) Related to astm_clk maximum frequency.
 (2) P = astm_clk period in ns
 (3) The jitter probability density can be approximated by a Gaussian function.
 (4) See [Section 4.3](#) for CORE OPP voltages.

[Table 6-156](#) presents STMv2 – 150MHz SD Card Interface parameters for Lauterbach LA-7992 and assumes testing over the recommended operating and electrical characteristic conditions.

Table 6-156. STMv2 Switching Characteristics – SD Card Interface for Lauterbach LA-7992 ⁽⁴⁾

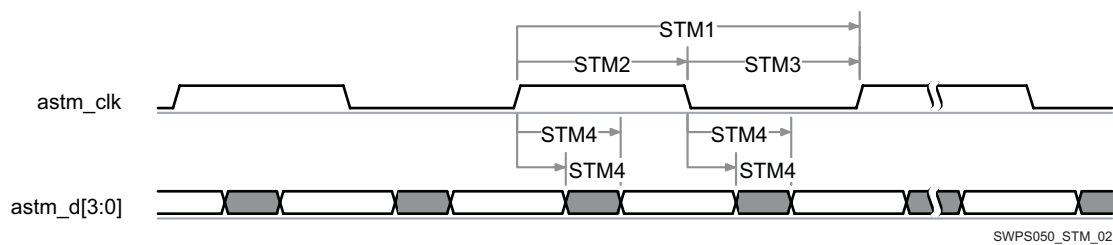
| NO. | PARAMETER | | OPP_NOM | | UNIT |
|------|---------------------------|--|----------------------|------|------|
| | | | MIN | MAX | |
| STM1 | $1 / t_{c(\text{clk})}$ | Frequency ⁽¹⁾ , output clock astm_clk | | 150 | MHz |
| STM2 | $t_{w(\text{clkH})}$ | Pulse duration, output clock astm_clk high | $0.5 \times P^{(2)}$ | | ns |
| STM3 | $t_{w(\text{clkL})}$ | Pulse duration, output clock astm_clk low | $0.5 \times P^{(2)}$ | | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output clock astm_clk | | 278 | ps |
| | $t_{j(\text{clk})}$ | Jitter standard deviation ⁽³⁾ , output clock astm_clk | | 36 | ps |
| | $t_{R(\text{clk})}$ | Rise time, output clock astm_clk | | 1.85 | ns |
| | $t_{F(\text{clk})}$ | Fall time, output clock astm_clk | | 1.85 | ns |
| STM4 | $t_{d(\text{clk-dataV})}$ | Delay time, output clock astm_clk low/high to output control astm_d[3:0] valid | 1.053 | 1.39 | ns |
| | $t_{R(\text{DO})}$ | Rise time, output data astm_d[3:0] | | 1.85 | ns |
| | $t_{F(\text{DO})}$ | Fall time, output data astm_d[3:0] | | 1.85 | ns |

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- (1) Related to astm_clk maximum frequency.
- (2) P = astm_clk period in ns
- (3) The jitter probability density can be approximated by a Gaussian function.
- (4) See [Section 4.3](#) for CORE OPP voltages.

**Figure 6-110. STMv2 - Transmit Mode**

7 Applications, Implementation, and Layout

7.1 Introduction

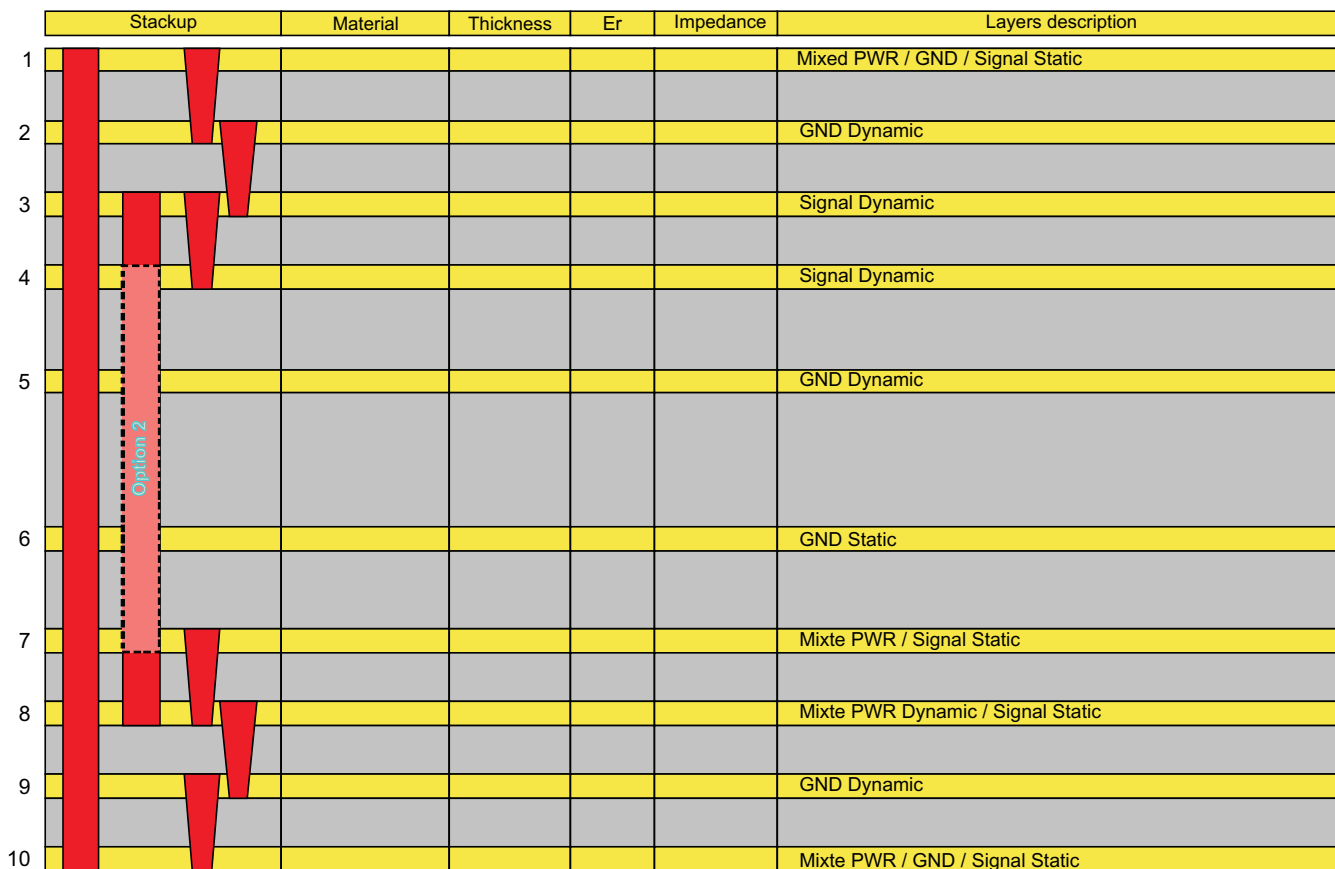
This chapter provides:

- Guidelines for the design of the PCB focusing first on power delivery network (PDN) implementation which is essential to achieve the desired level of performance on the OMAP5430 device.
- General principles and step-by-step approach for good PDN implementation and specific requirements for the different power supplies of the OMAP5 device.
- Methodology and requirements to meet the PCB routing of the Device differential interfaces (MIPI CSI-2 and DSI-1 D-PHY, MIPI HDMI PHY, USB PHY, and SATA PHY).
- PCB requirements for the general-purpose interface using a CMOS driver to meet timing requirements and minimize overshoot and undershoot at the far-end peripheral and minimize overshoot and undershoot at the far-end.
- The trace lengths given in this chapter are aligned with the FR-4 standard specification for PCB ($\epsilon_r = 4.0$). To provide a rough idea of the corresponding trace length: 67 ps per cm is considered.

7.1.1 Initial Requirements and Guidelines

The recommendation for Device board stackup is a 10-layer design with two options:

- Option 1: 3+4+3 with core via from layer 3 to layer 8
- Option 2: 3+4+3 with core via from layer 4 to layer 7 when routing is congested.



SWPS043-006

Figure 7-1. PCB Stackup

- The PDN must be optimized for low trace resistance and low trace inductance between the power management IC (PMIC) and OMAP5 device especially for vdd_mpu, vdd_mm, and vdd_core power supplies (ranked by order of criticality per their respective peak currents).
- Optimize routing power routing between vdd_mpu and the PMIC.
- It is highly recommended to run board frequency domain analysis on the vdd_mpu, vdd_mm, and vdd_core power supplies to check if proper board decoupling is implemented and confirm that the respective target impedances are met. For more information on target impedance, see , *External Capacitors*.
- Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 30 Ω and 65 Ω to minimize overshoot and undershoot on far-end loads. For more information see [Section 7.4, Single-Ended Interfaces](#).
- Characteristic impedance for differential interfaces must be routed as differential traces on the same layer. The trace width and spacing must be chosen to yield the recommended differential impedance. For more information see [Section 7.5, Differential Interfaces](#).
- An external interface using a connector must be protected following the IEC61000-4-2 level 4 system ESD.
- For the OMAP5432 device, the DDR3 memory is used—bottom:
 - There are two DDR3 channels. Each of these channels supports two chip selects and then two ranks. This means the DDR3 package can support two dies.

NOTE

The cutout technique is recommended each time it is needed to locally lower unexpected high capacitance (a wide PCB footprint of a discrete component on the top or bottom layer in regards to GND or supply shape, for instance). This technique prevents impedance discontinuities by locally removing the ground reference below the line (ground cutout) so that the actual electrical reference for the signal line will be located further away (on the next ground layer or on the edges of the plane cutout).

Special attention must be paid while doing such cutouts to limit coupling of unwanted noise coming from PCB traces that are present under the cutouts.

7.2 Power Optimizations

In this section you will find the necessary steps for the PCB power general routing:

- [Section 7.2.1, Step 1: Requirements and Guidelines for PCB Stack-up](#)
- [Section 7.2.2, Step 2: Physical Layout Guidelines of the PDN](#)
- [Section 7.2.3, Step 3: Static IR Drop PDN Guidelines](#), to minimize resistance, avoid neck-down, and reduce current density.

7.2.1 Step 1: Requirements and Guidelines for PCB Stack-up

The PCB stack-up (layer assignment) is an important factor in determining the optimal performance of the PDN. An optimized PCB stack-up for higher power integrity performance can be achieved by following these requirements:

- Power and ground plane pairs must be closely coupled together. The capacitance formed between the planes can decouple the power supply at high frequencies. Whenever possible, the power and ground planes must be solid to provide a continuous return path for the return current.
- Use a thin dielectric between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair. Minimizing the separation distance (the dielectric thickness) will maximize the capacitance.
- Keep the power and ground plane pair as close as possible to the top and bottom surfaces (see [Figure 7-2](#)). This will help to minimize the decoupling capacitors mounting, the via, and the power and ground plane pair spreading loop inductance.

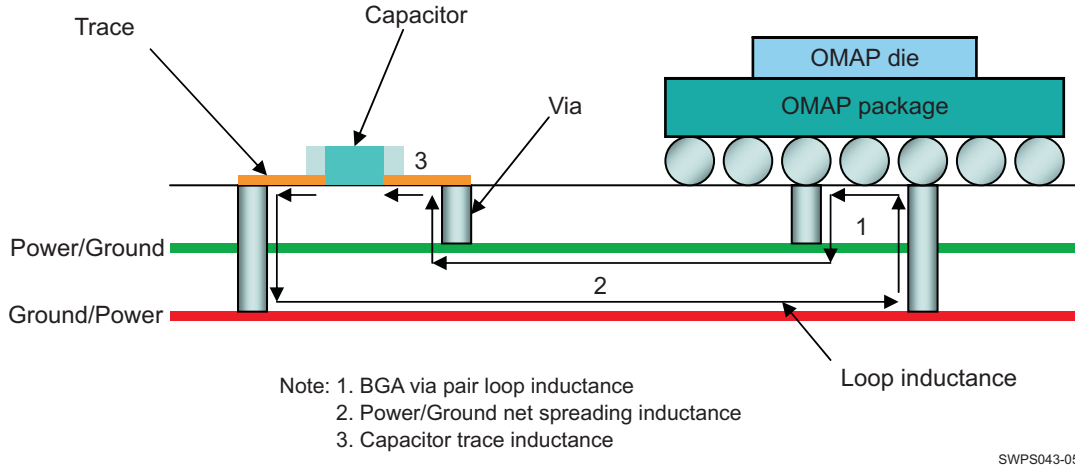


Figure 7-2. Minimize Loop Inductance With Proper Layer Assignment

The placement of power and ground planes in the PCB stackup (determined by layer assignment) has a significant impact on the parasitic inductances of the power current path as shown in Figure 7-2. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, putting high priority supplies in the top half of the stackup and low-priority supplies in the bottom half of the stackup as shown in the examples below (vias have parasitic inductances which impact the bottom layers more, so it is advised to put the sensitive and high priority power supplies on the top layers).

Figure 7-3 and Figure 7-4 show examples of typical PCB stack-up designed with power integrity in mind.

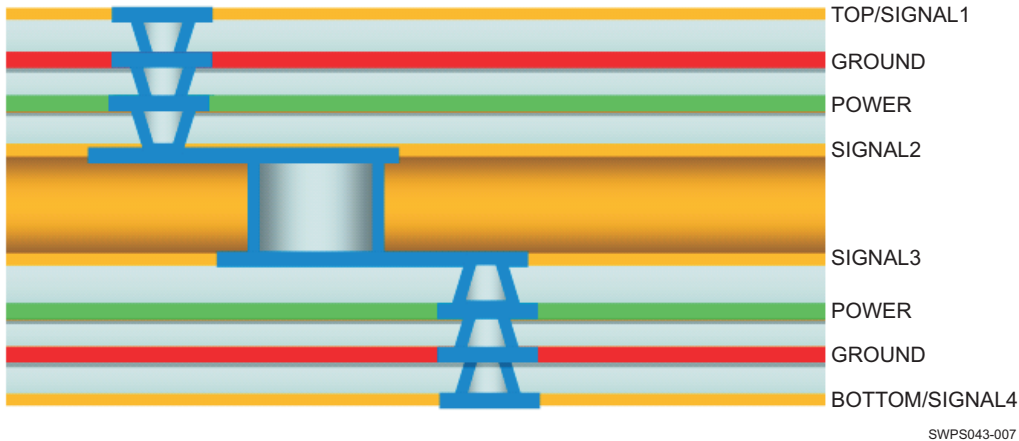


Figure 7-3. Layer PCB With High Density Interconnect (HDI) Vias

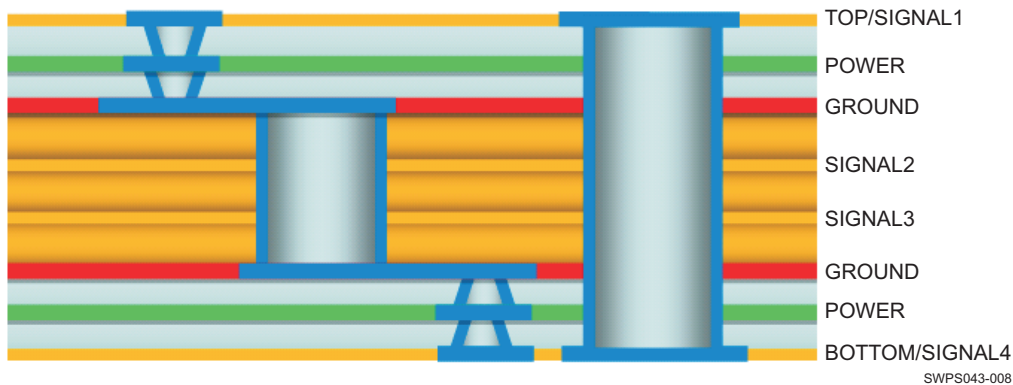


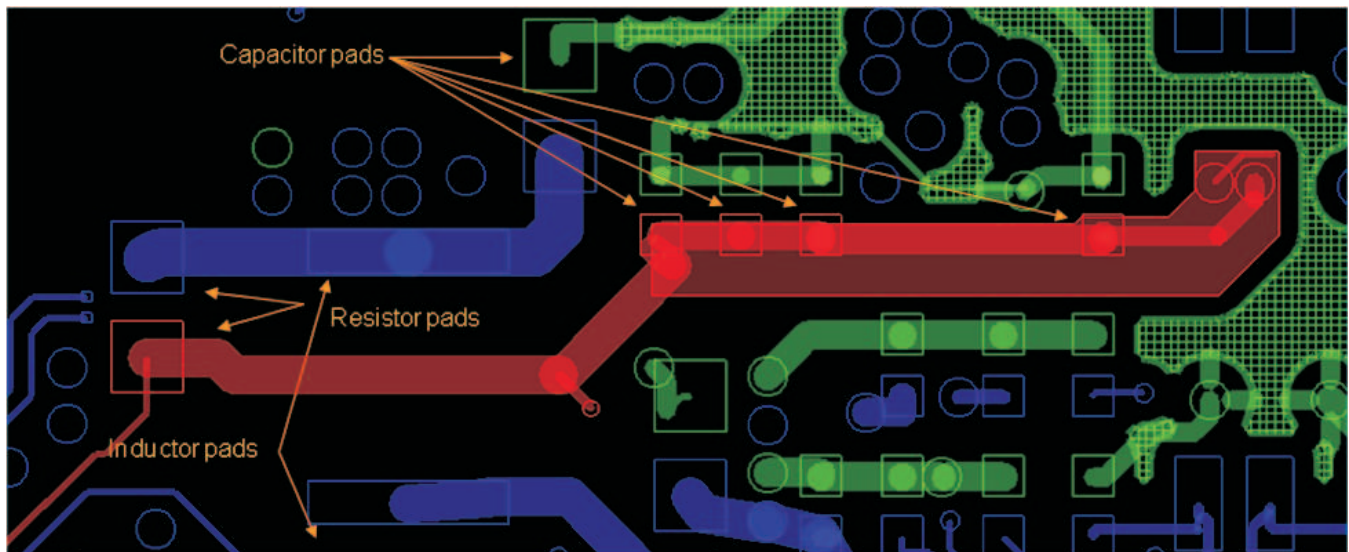
Figure 7-4. Layer PCB With Plated Through Holes (PTH) Vias

7.2.2 Step 2: Physical Layout Guidelines of the PDN

A critical step in designing an optimized PDN is that proper care must be taken to ensure that the initial layout is accomplished with good power integrity design guidelines in mind. The following points are important requirements that will need to be implemented in the PCB PDN design:

- External trace routing between components must be as wide as possible. The wider the trace, the lower the dc resistance and consequently the lower the static IR drop.
- Whenever possible, try aiming for a ratio of 1:1 or better for component (for example, capacitors and resistors) pins and vias. Do not share vias among multiple capacitors.
- Placement of the vias must be as close as possible to the solder pad.

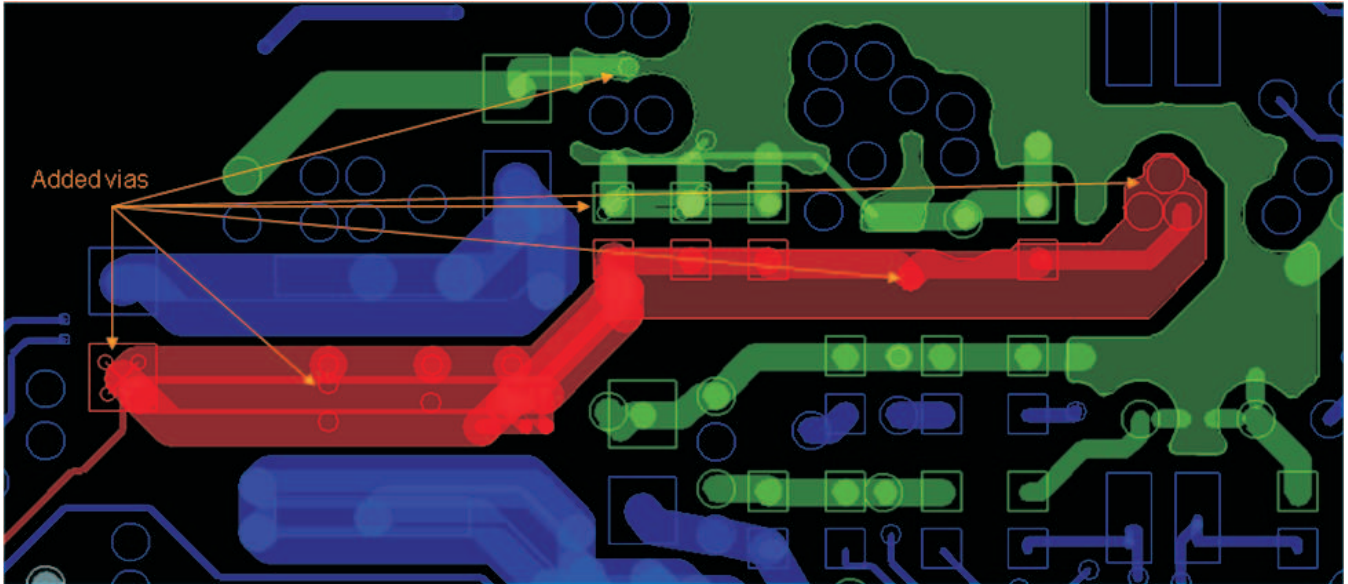
Figure 7-5 shows an example of acceptable width for power net routing but with poor via placement.



SWPS043-054

Figure 7-5. Poor Via Assignment for PDN

Figure 7-6 shows an improved power net routing with appropriate via assignment and placement, respectively.



SWPS043-055

Figure 7-6. Improved Via Assignment for PDN

To avoid any ampacity issue (this means the maximum current carrying capacity of each transitional via) an evaluation must be performed to determine the appropriate number of vias required to connect components.

Figure 7-7 and Figure 7-8 show examples of via starvation on a power net transitioning from the top routing layer to the internal layers and the improved layout, respectively.



SWPS043-056

One via for five capacitor pads is not good practice.

Figure 7-7. Via Starvation

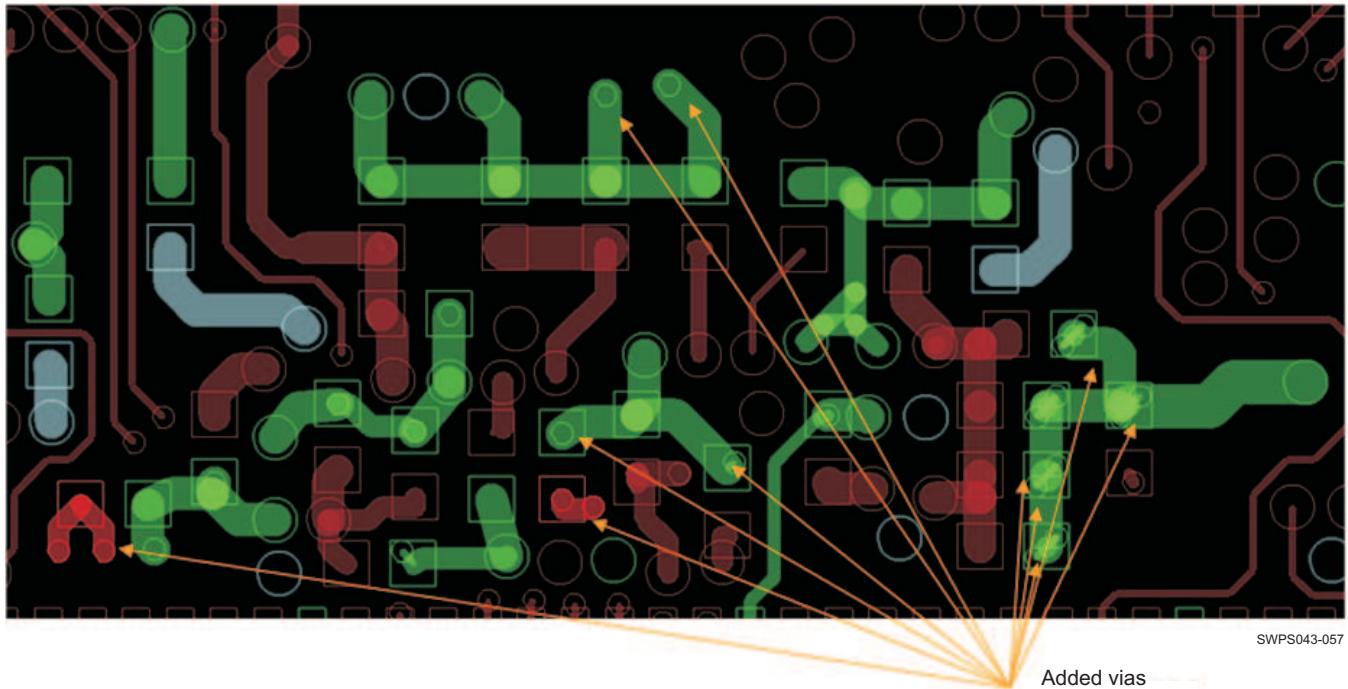


Figure 7-8. Improved Layout With More Transitional Vias

- It is also a good practice to perform a static IR drop analysis. This analysis can assess the appropriate number of vias and geometrical trace width dimensions required for the expected IR drop requirement.
- Whenever possible for the internal layers (routing and plane), wide traces and copper area fills are preferred for PDN layout. The routing power nets in plane provide for more interplane capacitance and improve high frequency performance of the PDN.
- Try to avoid different power nets (for example, VDD_MPU with VDD_CORE) coupling on the PCB by using coplanar shielding whenever appropriate.

Figure 7-9 represents an example of coplanar shielding for power nets.

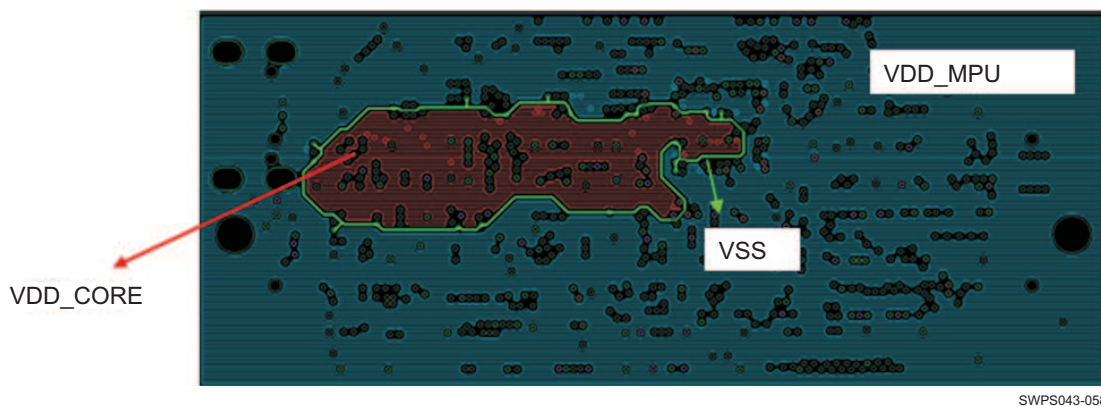


Figure 7-9. Coplanar Shielding of Power Net Using Ground Guard-band

- Decoupling capacitors must be mounted with minimum impact to inductance. A real capacitor has characteristics not only of capacitance but also inductance and resistance.

Figure 7-10 shows the parasitic model of a real capacitor. A real capacitor must be treated as an RLC circuit with effective series resistance (ESR) and effective series inductance (ESL).

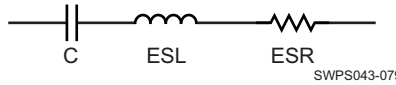


Figure 7-10. Characteristics of a Real Capacitor With ESL and ESR

The magnitude of the impedance of this series model is given as:

$$|Z| = \sqrt{ESR^2 + \left(\omega ESL - \frac{1}{\omega C}\right)^2}$$

where : $\omega = 2\pi f$

SWPS043-e001

Figure 7-11. Series Model Impedance Equation

Figure 7-12 shows the resonant frequency response of a typical capacitor with self-resonant frequency of 55 MHz. The impedance of the capacitor is a combination of its series resistance, reactive capacitance, and inductance as shown in Figure 7-11.

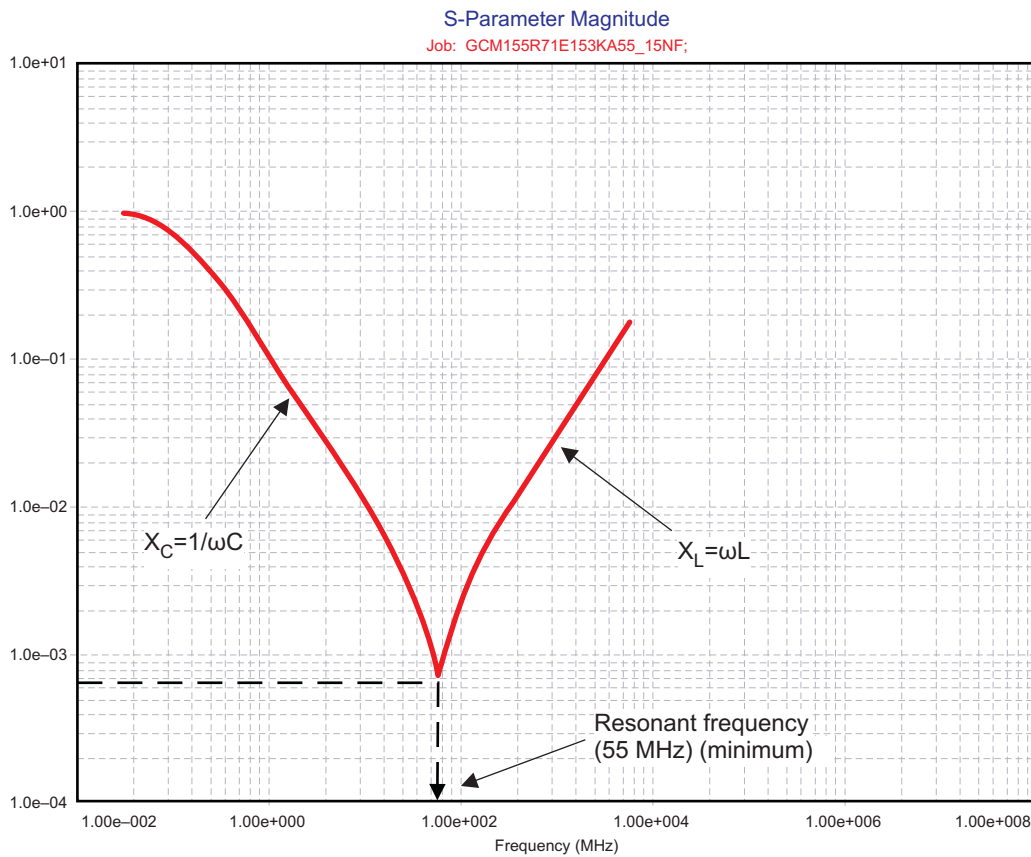


Figure 7-12. Typical Impedance Profile of a Capacitor

Since a capacitor has series inductance and resistance that will impact its effectiveness, it is important that the following recommendations are adopted in placing them on the PDN.

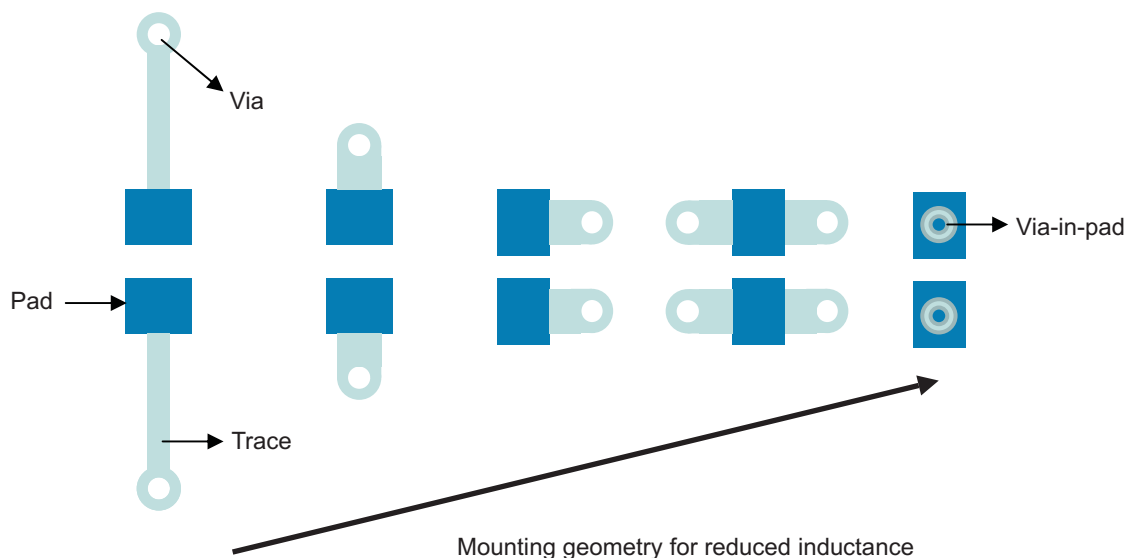
Whenever possible, please mount the capacitor with the geometry that will minimize the mounting inductance and resistance. This was shown earlier in Figure 7-2. The capacitor mounting inductance and resistance here includes the inductance and resistance of the pads, trace, and vias.

The length of a trace used to connect a capacitor has a big impact on parasitic inductance and resistance of the mounting. This trace must be as short and wide as possible. Wherever possible, minimize the trace by locating vias near the solder pad landing. Further improvements can be made to the mounting by placing vias to the side of capacitor lands or doubling the number of vias as shown in [Figure 7-13](#). If the PCB manufacturing processes allow and if cost-effective, via-in-pad (VIP) geometries are strongly recommended.

In addition to mounting inductance and resistance associated with placing a capacitor on the PCB, the effectiveness of a decoupling capacitor also depends on the spreading inductance and resistance that the capacitor sees with respect to the load. The spreading inductance and resistance is strongly dependent on the layer assignment in the PCB stack-up (as shown in [Figure 7-4](#)).

From left (highest inductance) to right (lowest inductance) the capacitor footprint types shown in [Figure 7-13](#) are known as:

- 2-via, Skinny End Exit (2vSEE)
- 2-via, Wide End Exit (2vWEE)
- 2-via, Wide Side Exit (2vWSE)
- 4-via, Wide Side Exit (4vWSE)
- 2-via, In-Pad (2vIP)



SWPS043-060

Figure 7-13. Capacitor Placement Geometry for Improved Mounting Inductance

NOTE

Evaluation of loop inductance values for decoupling capacitor footprints 2vSEE (worst case) vs 4vWSE (2nd best) has shown a 30% reduction in inductance when 4vWSE footprint was used in place of 2vSEE.

Decoupling Capacitor (Dcap) Strategy:

1. Use lowest inductance footprint and trace connection scheme possible for given PCB technology and layout area in order to minimize Dcap loop inductance to power pin as much as possible (see [Figure 7-13](#)).
2. Place Dcaps on “same-side” as component within their power plane outline to minimize “decoupling loop inductance”. Target distance to power pin should be less than ~500mils depending upon PCB layout characteristics (plane’s layer assignment and solid nature). Use PI modeling CAD tool to verify minimum inductance for top vs bottom-side placement.

3. Place Dcaps on “opposite-side” as component within their power plane outline if “same-side” is not feasible or if distance to power pin is greater than ~500mils for top-side location. Use PI modeling CAD tool to verify minimum inductance for top vs bottom-side placement.
4. Use minimum 10mil trace width for all voltage and gnd planes connections (i.e. Dcap pads, component power pins, etc.).
5. Place all voltage and gnd plane vias “as close as possible” to point of use (i.e. Dcap pads, component power pins, etc.).
6. Use a “Power/Gnd pad/pin to via” ratio of 1:1 whenever possible. Do not exceed 2:1 ratio for small number of vias within restricted PCB areas (i.e. underneath BGA components).

7.2.3 Step 3: Static IR Drop PDN Guidelines

Delivering reliable power to circuits is always of critical importance because IR drops can happen at every level in a chip, package, and board system. Components that are distant from their associated power source are particularly susceptible to an IR drop. The designs that rely on battery power must minimize the voltage drop to avoid unacceptable power loss. Early dc assessments help determine power distribution basics such as the best available entry point for power, layer stackup choices, and estimates for the amount of copper needed to carry the current.

The resistance, R_s , of a plane conductor for a unit length and unit width is called the surface resistivity (ohms per square).

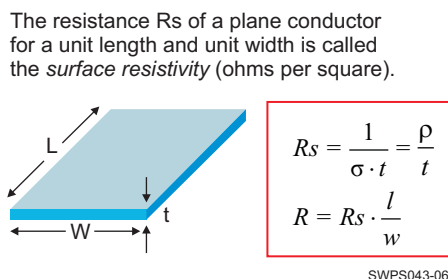
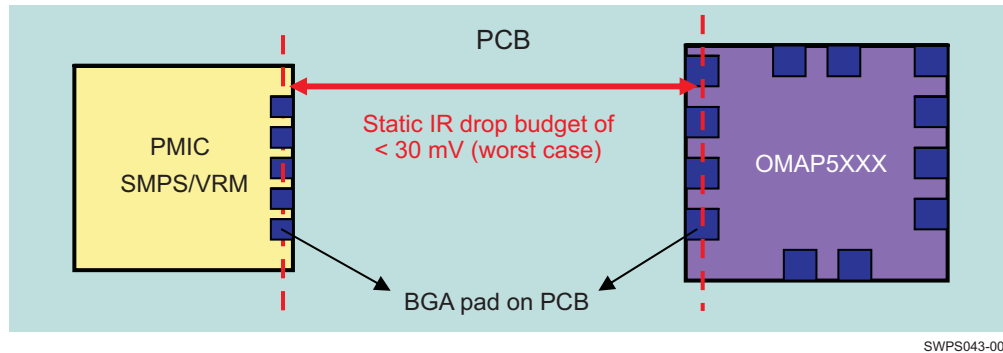


Figure 7-14. Depiction of Sheet Resistivity and Resistance

Ohm’s Law ($V = I \times R$) relates conduction current to voltage drop and at dc the relation coefficient is a constant representing the resistance of the conductor. Conductors also dissipate power due to their resistance. Both voltage drop and power dissipation are proportional to the resistance of the conductor.

System-level IR drop budget is made up of three portions: on-chip, package, and PCB board. Static IR or dc analysis and design methodology consists of designing the PDN such that the voltage drop (under dc operating conditions) across power and ground pads of the transistors of the application processor device is within a specified value of the nominal voltage for proper functioning of the device.

Figure 7-15 shows the PCB-level static IR drop budget is defined between the pins of the power management device PMIC or VRM and the BGA pads on the PCB to the application processor device to which the PMIC is supplying power.



SWPS043-009

Figure 7-15. Static IR Drop Budget for PCB Only

The total system-level margin allowed for proper device function is given, the allowable voltage variation at the BGA of the device is specified at 1.5% of the nominal voltage. For a 1.35-V supply, this must be = 20 mV. It is highly recommended to connect the VRM or the PMIC as close as physically possible on the PCB to the OMAP5430 device.

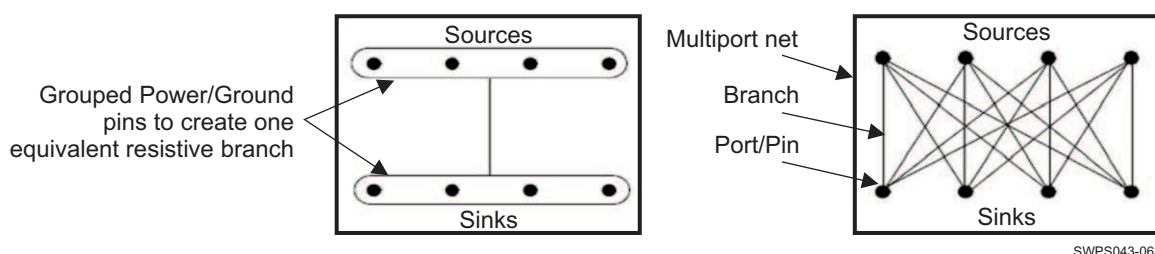
To accurately analyze the PCB static IR drop, the actual geometry of the PDN must often be properly modeled and simulated to accurately characterize long distribution paths, low weight copper, electro-migration violations of current-carrying vias, and swiss-cheese effects. It is recommended to perform the following analyses:

- Lumped resistance and IR drop analysis
- Distributed resistance and IR drop analysis

The requirements are present to perform both analyses and to show compliance. In the following sections each methodology is described in detail and examples provided of analysis flow that can be used by the PCB designer to validate compliance to the requirements on their PCB PDN design.

7.2.4 Lumped and Distributed Resistance and IR Drop Analysis Methodology

Lumped methodology consists of grouping all of the power and ground pins of the PMIC and the processor device. This is followed by extracting the lumped resistance or dc voltage drop of the equivalent path by applying a voltage source at the PMIC end and a current sink at the device end. Figure 7-16 describes the pin-grouping concept.



SWPS043-063

Figure 7-16. Pin-grouping Concept: Lumped and Distributed Methodologies

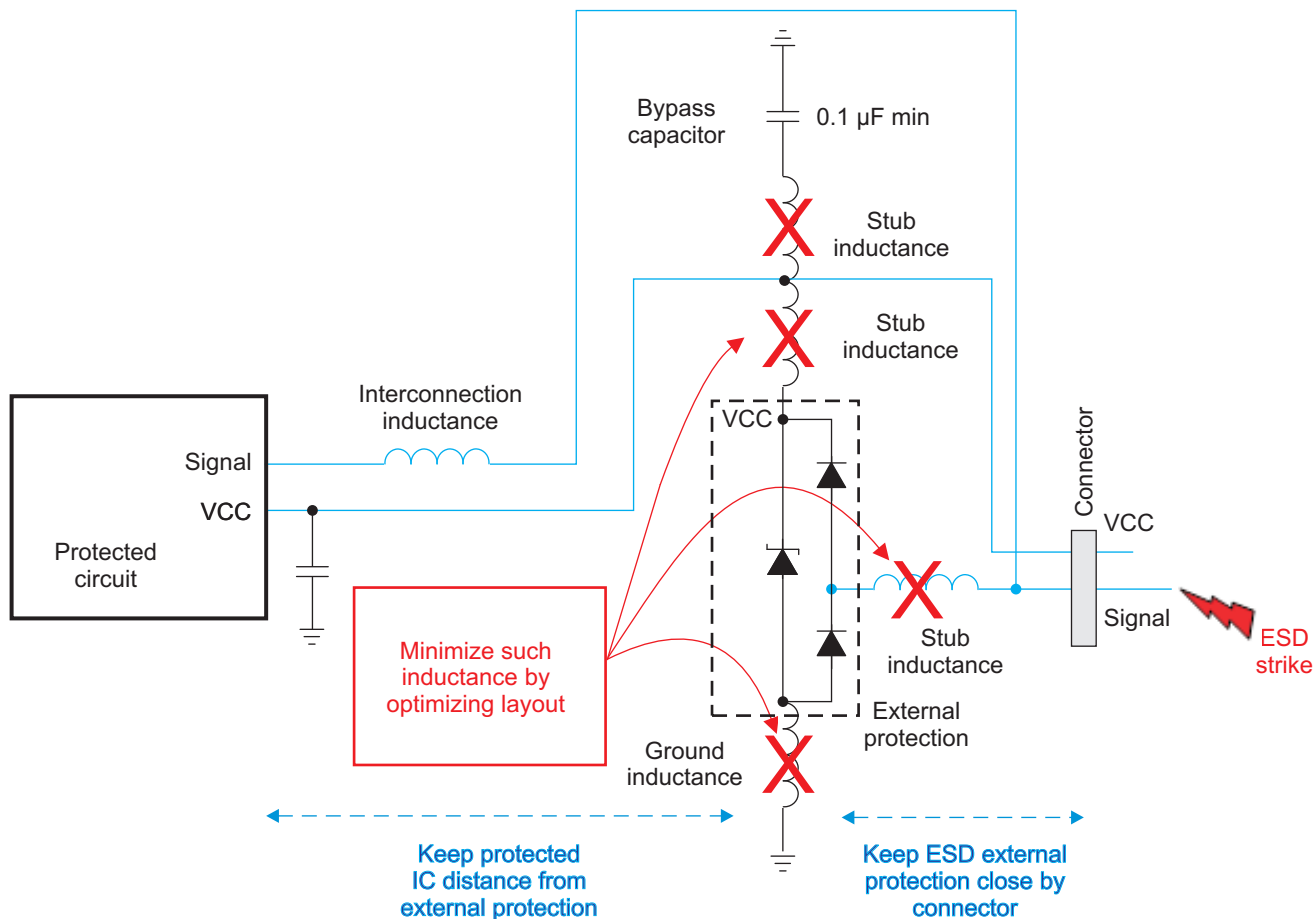
The lumped methodology consists of importing the PCB layout database (from the Cadence Allegro tool or any other layout design tool) into the static IR drop modeling and simulation tool of preference for the PCB designer. This is followed by applying the correct PCB stack-up information (thickness and material properties) of the PCB dielectric and metallization layers. The material properties of the dielectric consist of permittivity (Dk) and loss tangent (Df).

For the conductor layers, the correct conductivity needs to be programmed into the simulation tool. This is followed by pin-grouping of the power and ground nets, and applying appropriate voltage and current sources. The current and voltage information can be obtained from the power and voltage specifications of the device under different operating conditions and use-modes. After running the simulation, the lumped resistance and lumped IR drop can be examined as shown in [Figure 7-16](#).

7.2.5 System ESD Generic Guidelines

7.2.5.1 System ESD Generic PCB Guidelines

- Protection devices must be placed close to the ESD source which means close to the connector. This allows the device to subtract the energy associated with an ESD strike before it reaches the internal circuitry of the application board.
- To help minimize the residual voltage pulse that will be built-up at the protection device due to its nonzero turn-on impedance, it is mandatory to route the ESD device with minimum stub length so that the low-resistive, low-inductive path from signal to ground is established and does not increase the impedance between signal and ground.
- For an ESD protection array being railed to a power supply when no decoupling capacitor is available in close vicinity, consider using a decoupling capacitor (= 0.1 μ F) tight to the VCC pin of the ESD protection. A positive strike will be partially diverted to this capacitor resulting in a lower residual voltage pulse.
- Ensure that there is enough metallization for the supply of signals at the interconnect side (VCC and GND in [Figure 7-17](#)) from connector to external protection because the interconnect may see between 8- to 30-A current in a short period of time during the ESD event.



SWPS043-010

Figure 7-17. Recommendation for an ESD External Protection⁽¹⁾

(1) To ensure normal behavior of the ESD protection (unwanted leakage), it is better to ground the ESD protection to the board ground rather than any local ground (example isolated shield or audio ground).

7.2.5.2 Miscellaneous EMC Guidelines to Mitigate ESD Immunity

- Avoid running critical signal traces (clocks, resets, interrupts, control signals, etc.) near PCB edges.
- Add high-frequency filtering: Decoupling capacitors close to the receivers rather than close to the drivers to minimize ESD coupling.
- Put a ground (guard) ring around the entire periphery of the PCB to act as a lightning rod.
- Connect the guard ring to the PCB ground plane to provide a low-impedance path for ESD-coupled current on the ring.
- Fill unused portions of the PCB with ground plane.
- Minimize circuit loops between power and ground by using a multilayer PCB with dedicated power and ground planes.
- Shield long line lengths (strip lines) to minimize radiated ESD.
- Avoid running traces over split ground planes. It is better to use a bridge connecting the two planes in one area.

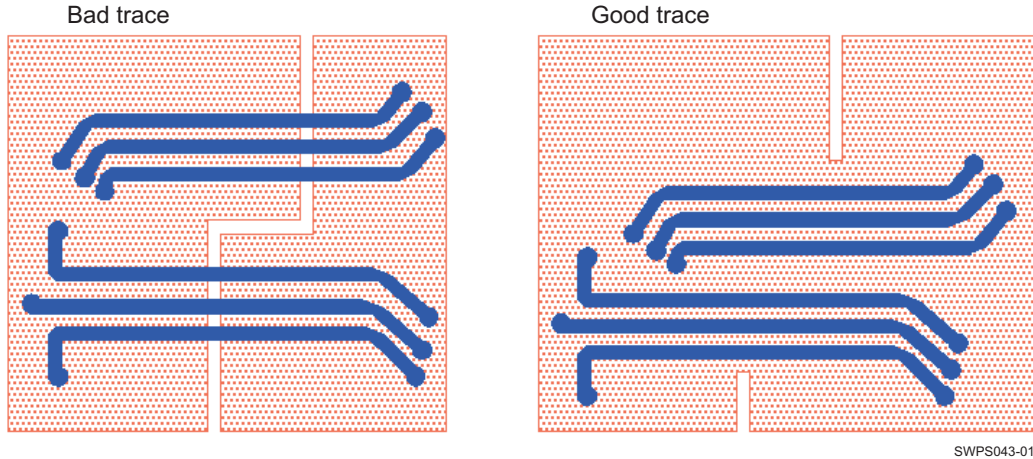


Figure 7-18. Trace Examples

- Always route signal traces and their associated ground returns as close to one another as possible to minimize the loop area enclosed by current flow:
 - At high frequencies current follows the path of least inductance.
 - At low frequencies current follows the path of least resistance.

7.2.6 EMI / EMC Issues Prevention

All high-speed digital integrated circuits can be sources of unwanted radiation, which can affect nearby sensitive circuitry and cause the final product to have radiated emission levels above the limits allowed by the EMC regulations if prevention steps are not taken. Likewise, analog and digital circuits can be susceptible to interferences from the outside world and picked up by the circuitry interconnections. To minimize the potential for EMI/EMC issues, the following guidelines are recommended to be followed.

7.2.6.1 Signal Bandwidth

To evaluate the frequency of digital signals, an estimated rule of thumb is to consider its bandwidth, f_{BW} , with respect to its rise time, t_R :

$$f_{BW} \sim 0.35 / t_R$$

This frequency actually corresponds to the break point in the signal spectrum, where the harmonics start to decay at 40 dB per decade instead of 20 dB per decade.

7.2.6.2 Signal Routing

7.2.6.2.1 Signal Routing—Sensitive Signals and Shielding

Keep radio frequency (RF) sensitive circuitry (like GPS receivers, GSM/WCDMA, *Bluetooth*/WLAN transceivers, frequency modulation (FM) radio, ...) away from high-speed ICs (such as, the OMAP device, power and audio managers, chargers, memories) and ideally on the opposite side of the PCB. For improved protection it is recommended to place these emission sources in a shield can. If the shield can have a removable lid (two-piece shield), ensure there is low contact impedance between the fence and the lid. Leave some space between the lid and the components under it to limit the high-frequency currents induced in the lid. Limit the shield size to put any potential shield resonances above the frequencies of interest; see [Figure 7-12](#), *Typical Impedance Profile of a Capacitor*.

7.2.6.2.2 Signal Routing—Outer Layer Routing

In case there is a need to use the outer layers for routing outside of shielded areas, it is recommended to route only static signals and make sure that these static signals do not carry any high-frequency components (due to parasitic coupling with other signals). In case of long traces, make provisions for a bypass capacitor near the signal source.

Routing of high-frequency clock signals on outer layers, even for a short distance, is discouraged, because their emission energy is concentrated at the discrete harmonics and can become significant even with poor radiators. Coplanar shielding of traces on outer layers (placing the ground near the sides of a track along its length) is effective only if the distance between the trace sides and the ground is smaller than the trace height above the ground reference plane. For modern multilayer PCBs this is often not possible so coplanar shielding will not be effective.

Do not route high-frequency traces near the periphery of the PCB, as the lack of a ground reference near the trace edges can increase EMI; see [Section 7.2.6.3, Ground Guidelines](#).

7.2.6.3 Ground Guidelines

7.2.6.3.1 PCB Outer Layers

Ideally the areas on the top and bottom layers of the PCB that are not enclosed by a shield must be filled with ground after the routing is completed and connected with an adequate number of vias to the ground on the inner ground planes.

7.2.6.3.2 Metallic Frames

Ensure that all metallic parts are well connected to the PCB ground (like metallic frames for LCD screens, antenna reference planes, connector cages, flex cable grounds, and so forth). If using flex PCB ribbon cables to bring high-frequency signals off the PCB then ensure they are adequately shielded (coaxial cables or flex ribbons with a solid reference ground).

7.2.6.3.3 Connectors

For high-frequency signals going to connectors choose a fully shielded connector, if possible (for example, SD card connectors). For signals going to external connectors or that are routed over long distances, it is recommended to reduce their bandwidth by using low-pass filters (RC (resistor, capacitor) combinations or lossy ferrite inductors). These filters will help to prevent emissions from the board and can also improve the immunity from external disturbances.

7.2.6.3.4 Guard Ring on PCB Edges

The major advantage of a multilayer PCB with ground planes is the ground return path below each and every signal or power trace. As shown in [Figure 7-19](#) the field lines of the signal return to the PCB ground as long as an infinite ground is available.

Traces or planes near the PCB edges do not have this infinite ground and therefore may radiate more than others. Thus, signals (like clocks) or power traces (like core power) identified as critical must not be routed in the vicinity of PCB edges, or, if not avoidable, must be accompanied by a guard ring on the PCB edge.

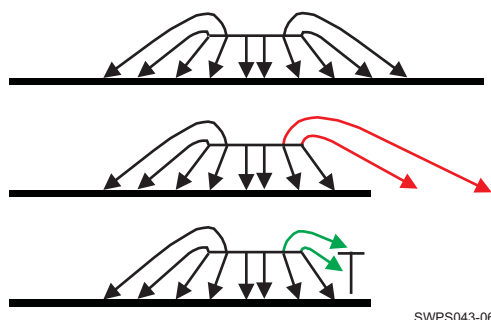


Figure 7-19. Field Lines of a Signal Above Ground



Figure 7-20. Guard Ring Routing

The intention of the guard ring is that HF energy, that otherwise would have been emitted from the PCB edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including the power layer) must be applied as shown in [Figure 7-20](#).

As these traces must have the same (HF-) potential as the ground plane, they must be connected to the ground plane at least every 10 mm.

7.2.6.3.5 Analog and Digital Grounds

For the optimum solution, the AGND and the DGND planes must be connected together at the power supply source at the same point. This ensures that both planes are at the same potential, while the transfer of noise from the digital to the analog domain is minimized.

7.3 Core Power Domains

This section provides boundary conditions and theoretical background to be applied as a guide for optimizing a PCB design. The decoupling capacitor and PDN characteristics tables shown below give recommended capacitors and PCB parameters to be followed for schematic and PCB designs. Board designs that meet the static and dynamic PDN characteristics shown in tables below will be aligned to the expected PDN performance needed to optimize SoC performance.

7.3.1 General Constraints and Theory

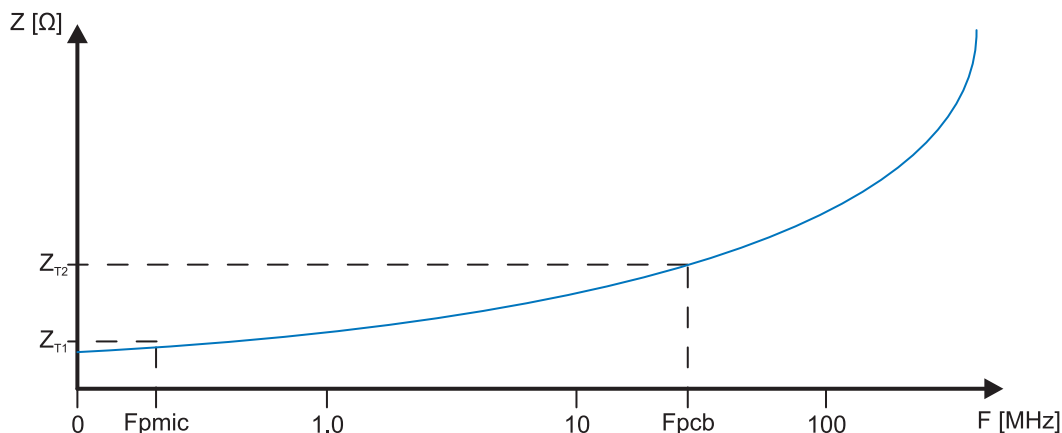
- Max PCB static/DC voltage drop (IRd) budget of **1.5% of supply voltage** when using PMICs **without remote sensing** as measured from PMIC's power inductor filter capacitor node to Processor input including any ground return losses.
- Max PCB static/DC voltage drop (IRd) budget can be relaxed to 5% of supply voltage when using PMICs with remote sensing at the load as measured from PMIC's power inductor and filter capacitor node to Device's supply input including any ground return losses.
- PMIC component DM and guidelines should be referenced for the following:
 - Routing remote feedback sensing to optimize per each SMPS's implementation
 - Selecting power filtering capacitor values and PCB placement.
- Max Effective Resistance (R_{eff}) budget can range from **4 – 50mΩ** for key Device power rails not including ground returns depending upon maximum load currents and maximum DC voltage drop budget (as discussed above).
- Max Device supply input voltage difference budget of **5mV** under max current loading shall be maintained across all balls connected to a common power rail. This represents any voltage difference that may exist between a remote sense point to any power input.
- Max PCB Loop Inductance (LL) budget between Device's power inputs and local bulk and high frequency decoupling capacitors including ground returns should range from **0.4 – 2.5nH depending upon maximum transient load currents**.
- Max PCB dynamic/AC peak-to-peak transient noise voltage budgets between PMIC and Device including ground returns are as follows:
 - **+/-3% of nominal supply voltage** for frequencies below the PMIC bandwidth (typ F_{pmic} ~ 200kHz)
 - **+/-5% of nominal supply voltage** for frequencies between F_{pmic} to F_{pcb} (typ 20 – 100MHz)

- Max PCB Impedance (Z) vs Frequency (F) budget between Device's power inputs and PMIC's output power filter node including ground return is determined by applying the Frequency Domain Target Impedance Method to determine the PCB's maximum frequency of interest (Fpcb). Ideally a properly designed and decoupled PDN will exhibit smoothly increasing Z vs. F curve. There are 2 general regions of interest as can be seen in [Figure 7-21](#).
 - 1st area is from DC (0Hz) up to Fpmic (typ a few 100 kHz) where a PMIC's transient response characteristic (i.e. Switching Freq, Compensation Loop BW) dominate. A PDN's Z is typically very low due to power filtering & bulk capacitor values when PDN has very low trace resistance (i.e. good Reff performance). The goal is to maintain a smoothly increasing Z that is less than Zt1 over this low frequency range. This will ensure that a max transient current event will not cause a voltage drop more than the PMIC's current step response can support (typ 3%).
 - 2nd area is from Fpmic up to Fpcb (typ 20-100MHz) where a PCB's inherent characteristics (i.e. parasitic capacitance, planar spreading inductances) dominate. A PDN's Z will naturally increase with frequency. At frequencies between Fpmic up to Fpcb, the goal is to maintain a smoothly increasing Z to be less than Zt2. This will ensure that the high frequency content of a max transient current event will not cause a voltage drop to be more than 5% of the min supply voltage.

$$Z_T = \frac{\text{Max Voltage Rail Drop}^{\text{Note1}}}{\text{Max Transient Current}^{\text{Note2}}}$$

$$Z_{T1} = \frac{(\text{Min Voltage}) \times (\text{PMIC's Step Response})}{(\sim 50\% \text{ of Max DC Current})} = \frac{V_{\text{min}} \times 3\%(\text{typ})}{I_{\text{max}} \times \sim 50\%}$$

$$Z_{T2} = \frac{(\text{Min Voltage}) \times (\text{High-Freq Transient Noise})}{(\sim 50\% \text{ of Max DC Current})} = \frac{V_{\text{min}} \times 5\%(\text{typ})}{I_{\text{max}} \times \sim 50\%}$$



PCB_CPD_8

Figure 7-21. PDN's Target impedance

1.Voltage Rail Drop includes regulation accuracy, voltage distribution drops, and all dynamic events such as transient noise, AC ripple, voltage dips etc.

2. Typical max transient current is defined as 50% of max current draw possible.

7.3.2 Voltage Decoupling

Recommended power supply decoupling capacitors main characteristics for commercial products whose ambient temperature is not to exceed +85C are shown in table below:

Table 7-1. Decoupling Bypass Capacitors Main Characteristics⁽¹⁾⁽²⁾

| CAPACITOR | PACKAGE | VERSION | TOLERANCE | VOLTAGE | REFERENCE |
|-------------|---------|---------|-----------|---------|-------------------|
| 22 μ F | 0603 | X5R | \pm 20% | 6.3 V | GRM188R60J226MEA |
| 4.7 μ F | 0402 | X5R | \pm 20% | 6.3 V | GRM155R60J475ME87 |
| 2.2 μ F | 0402 | X5R | \pm 20% | 6.3 V | GRM155R60J225ME95 |
| 1 μ F | 0201 | X5R | \pm 20% | 6.3 V | GRM033R60J105MEA2 |
| 470 nF | 0201 | X5R | \pm 20% | 6.3 V | GRM033R60J474ME90 |
| 220 nF | 0201 | X5R | \pm 20% | 4.0 V | GRM033R60G224ME15 |
| 100 nF | 0201 | X5R | \pm 20% | 6.3 V | GRM033R60J104ME19 |

(1) Minimum value for each PCB capacitor: 100 nF.

(2) Among the different capacitors, 470 nF is recommended (not required) to filter at 5-MHz to 10-MHz frequency range.

7.3.3 Static PDN Analysis

One power net parameter derived from a PCB's PDN static analysis is the Effective Resistance (Reff). This is the total PCB power net routing resistance that is the sum of all the individual power net segments used to deliver a supply voltage to the point of load and includes any series resistive elements (i.e. current sensing resistor) that may be installed between the PMIC outputs and Processor inputs

7.3.4 Dynamic PDN Analysis

Three power net parameters derived from a PCB's PDN dynamic analysis are the Loop Inductance (LL), Impedance (Z) and PCB Frequency of Interest (Fpcb).

- LL values shown are the recommended max PCB trace inductance between a decoupling capacitor's power supply and ground reference terminals when viewed from the decoupling capacitor with a "theoretical shorted" applied across the Processor's supply inputs to ground reference.
- Z values shown are the recommended max PCB trace impedances allowed between Fpmic up to Fpcb frequency range that limits transient noise drops to no more than 5% of min supply voltage during max transient current events.
- Fpcb (Frequency of Interest) is defined to be a power rail's max frequency after which adding a reasonable number of decoupling capacitors no longer significantly reduces the power rail impedance below the desired impedance target (Zt2). This is due to the dominance of the PCB's parasitic planar spreading and internal package inductances.

Table 7-2. Core, MPU, MM Decoupling Characteristics⁽⁶⁾

| PARAMETER | PDN IMPEDANCE CHARACTERISTICS ⁽⁴⁾ | | PCB RESISTANCE BETWEEN SPMS AND OMAP (m Ω) ⁽⁵⁾ | MAXIMUM LOOP INDUCTANCE PER CAPACITOR (nH) ⁽²⁾ | DECOUPLING CAPACITOR VALUES ⁽³⁾ | | | | | | |
|-----------------------|--|-----------------------------|---|---|--|--------|--------|-----------|-------------|-------------|------------|
| | IMPEDANCE TARGET (m Ω) | FREQUENCY OF INTEREST (MHz) | | | 100 nF | 220 nF | 470 nF | 1 μ F | 2.2 μ F | 4.7 μ F | 22 μ F |
| C _{vdd_core} | 82 | 77 | 20 | 0.6 | 3 | 1 | 0 | 1 | 0 | 1 | 0 |
| C _{vdd_mpu} | 28 | 16 | 5 | 0.4 | 5 | 0 | 3 | 4 | 1 | 0 | 1 |
| C _{vdd_mm} | 41 | 30 | 10 | 0.5 | 3 | 1 | 0 | 1 | 0 | 1 | 0 |

- (1) For more information on peak-to-peak noise values, see , *Recommended Operating Conditions*.
- (2) Values do not include ESL of the capacitor, and the ESL of the capacitor should not exceed 0.5 nH.
- (3) To take into account the aging effects and voltage impact on capacitance, their values, as described in [Table 7-1](#), are specified at $\pm 50\%$.
- (4) The PDN (Power Delivery Network) impedance characteristics are defined versus the device activity (that runs at different frequency) based on , *Recommended Operating Conditions*.
- (5) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the OMAP5 power balls.
- (6) Assuming that the external SMPS (power IC) feedback sense is taken close to OMAP5432 power balls.

Table 7-3. VIO_DDR3 Decoupling Characteristics⁽¹⁾⁽²⁾

| PARAMETER | VOLTAGE (V) | PDN IMPEDANCE CHARACTERISTICS | | DECOUPLING CAPACITOR VALUES | | | |
|---|-------------|--------------------------------|-----------------------------|-----------------------------|-------|-----------|-------------|
| | | Impedance Target (m Ω) | Frequency of Interest (MHz) | 100nF | 470nF | 1 μ F | 2.2 μ F |
| $C_{vdds_ddr_ch1} / C_{vdds_ddr_ch2}$ | 1.35 | 135 | 202 | 8 | 2 | 1 | 1 |
| $C_{vddq_vref_ddrch1} / C_{vddq_vref_ddrch2}$ | | | | | | | |

- (1) The data in this table are given with an assumption of 500 mA for 1.35- and 1.5-V voltages. This current value can vary depending on the memory vendor.
- (2) The worst case is at 1.35 V. The 1.5 V case is covered by the worst case.

NOTE

For power IC which can support more than 10 μ F close to processor, a bulk capacitor of at least 22 μ F is strongly recommended for VDD_MPU power domains.

NOTE

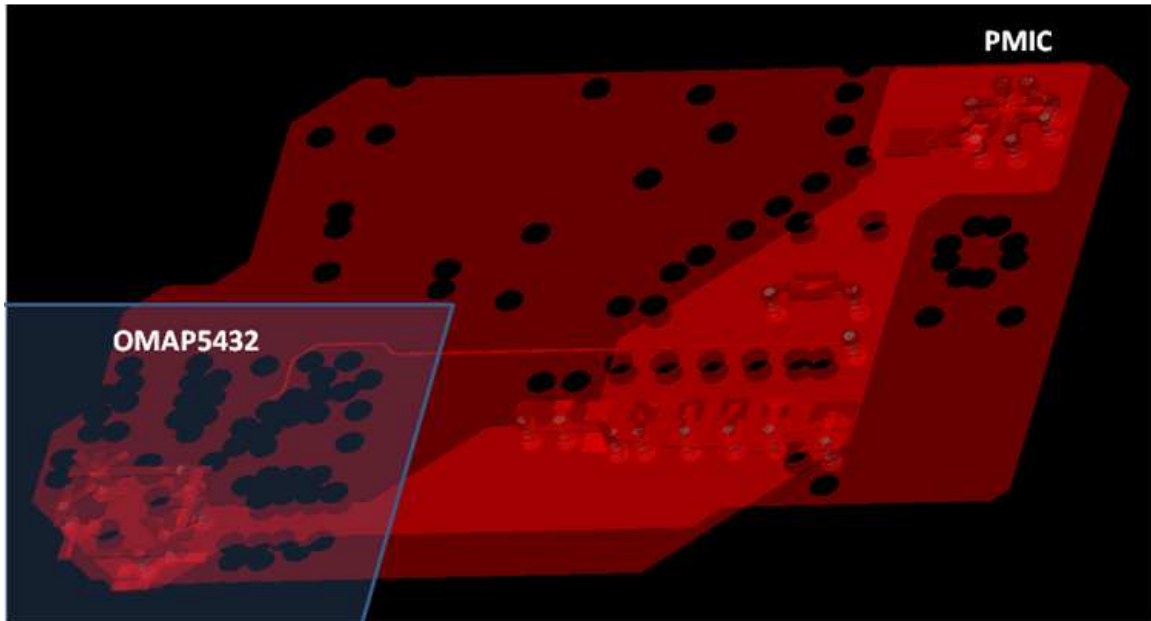
The loop inductance from SOC pin and ground of internal LDO to external capacitor (1 μ F) is 6 nH maximum. (Example: signal name "cap_vdda_ldo_sram_core_array" on ball T25)

7.3.5 Example PCB Design**7.3.5.1 MPU Voltage Decoupling PCB Examples**

[Figure 7-22](#) and [Figure 7-23](#) show an example of PCB layout of vdd_mpu with the PMIC that meets the IR drop requirements and the PCB inductance loop.

NOTE

[Figure 7-22](#) and [Figure 7-23](#) describe a working board. They do not show an optimized board.

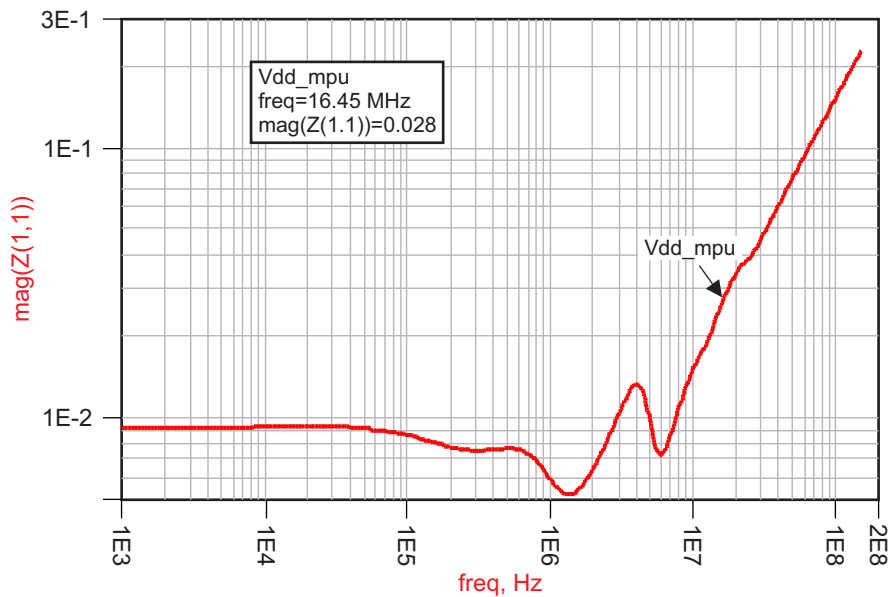


SWPS044-028

Figure 7-22. vdd_mpu PCB Requirements⁽¹⁾

(1) Figure 7-22 shows an example of vdd_mpu PCB layout that meets the IR drop and capacitance-inductance loop requirements.

Figure 7-23 describes the vdd_mpu PDN analysis versus frequency.



SWPS043-022

Figure 7-23. vdd_mpu PDN Analysis

7.3.5.2 MM Voltage Decoupling PCB Examples

Figure 7-24 and Figure 7-25 show an example of PCB layout of vdd_mm with the PMIC that meets the IR drop requirements and the PCB inductance loop.

NOTE

Figure 7-24 and Figure 7-25 describe a working board. They do not show an optimized board.

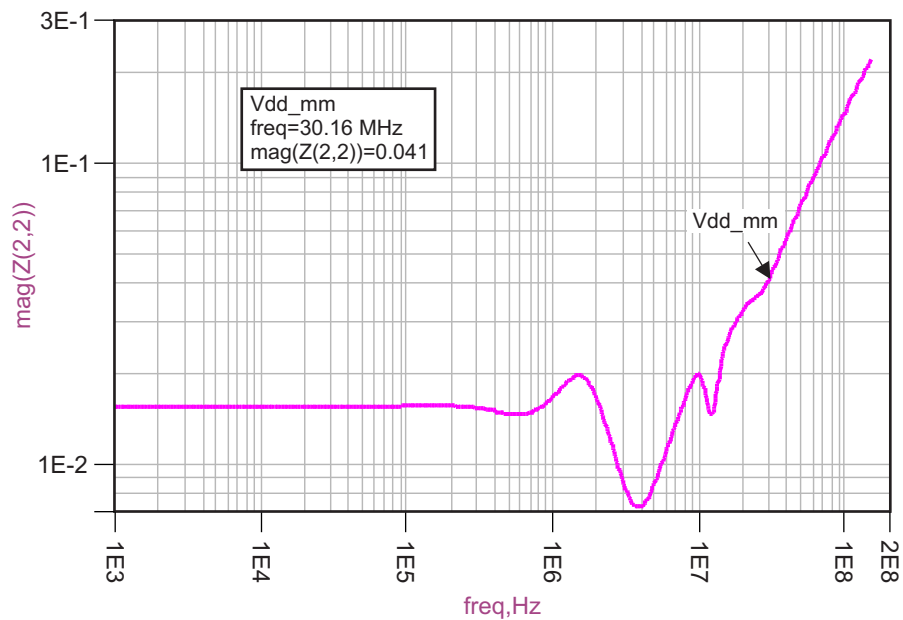


SWPS044-030

Figure 7-24. vdd_mm PCB Routing⁽¹⁾

(1) Figure 7-24 shows an example of vdd_mpu PCB layout that meets the IR drop and capacitance-inductance loop requirements.

Figure 7-25 shows the vdd_mm PDN analysis versus frequency:



SWPS043-020

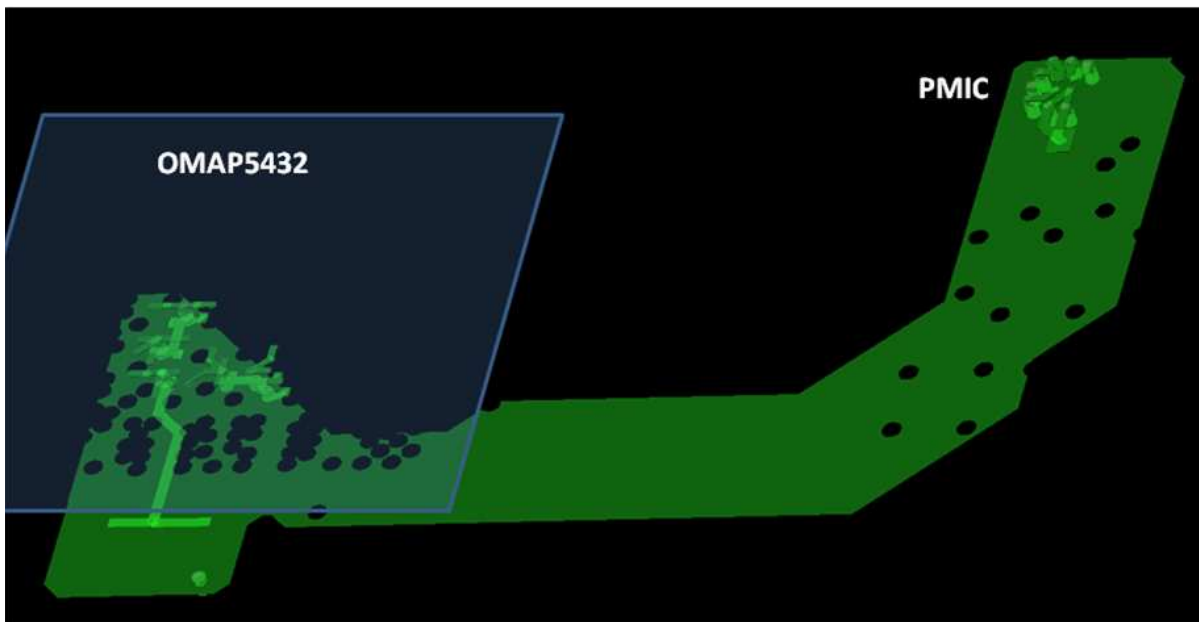
Figure 7-25. vdd_mm PDN Analysis

7.3.5.3 Core Voltage Decoupling PCB Examples

Figure 7-26 and Figure 7-27 show an example of PCB layout of vdd_core with the PMIC that meets the IR drop requirements and the PCB inductance loop.

NOTE

Figure 7-26 and Figure 7-27 show describe a working board. They do not show an optimized board.



SWPS044-032

Figure 7-26. vdd_core PCB Routing⁽¹⁾

(1) Figure 7-26 describes an example of vdd_core PCB layout that meets the IR drop and capacitance-inductance loop requirements.

Figure 7-27 shows the vdd_core PDN analysis versus frequency:

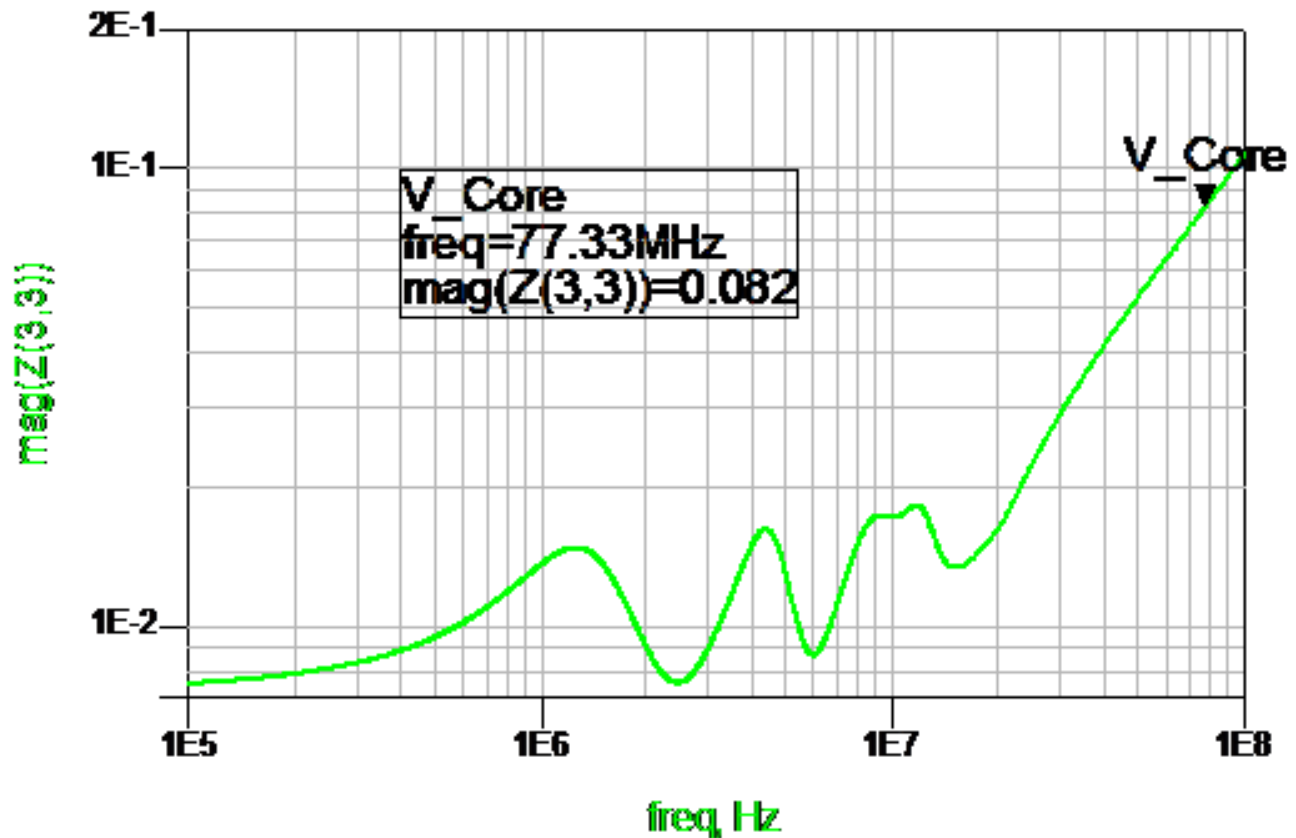


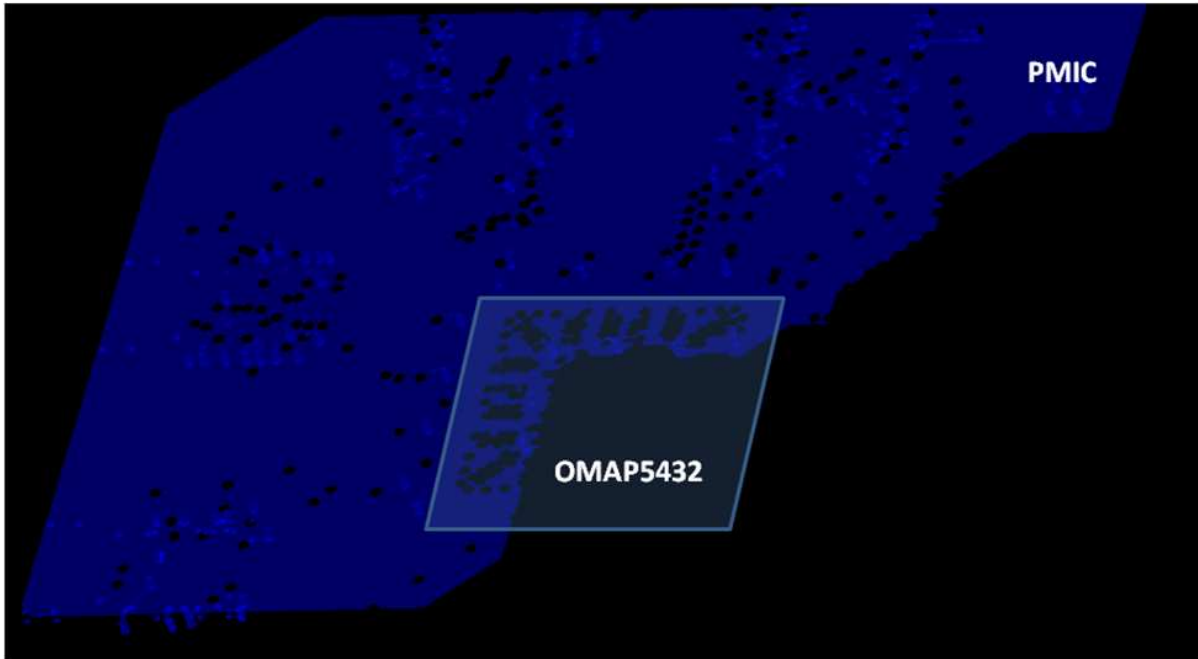
Figure 7-27. vdd_core PDN Analysis

7.3.5.4 VIO_DDR3 Decoupling PCB Examples

Figure 7-28 and Figure 7-29 show an example of PCB layout of VIO_1V5 with the PMIC that meets the IR drop requirements and the PCB inductance loop.

NOTE

Figure 7-28 and Figure 7-29 describe a working board. They do not show an optimized board.



SWPS044-034

Figure 7-28. vdd_core PCB Routing⁽¹⁾

(1) [Figure 7-28](#) describes an example of VIO_1V5 PCB layout that meets the IR drop and capacitance-inductance loop requirements.

[Figure 7-29](#) shows the VIO_1V5 PDN analysis versus frequency:

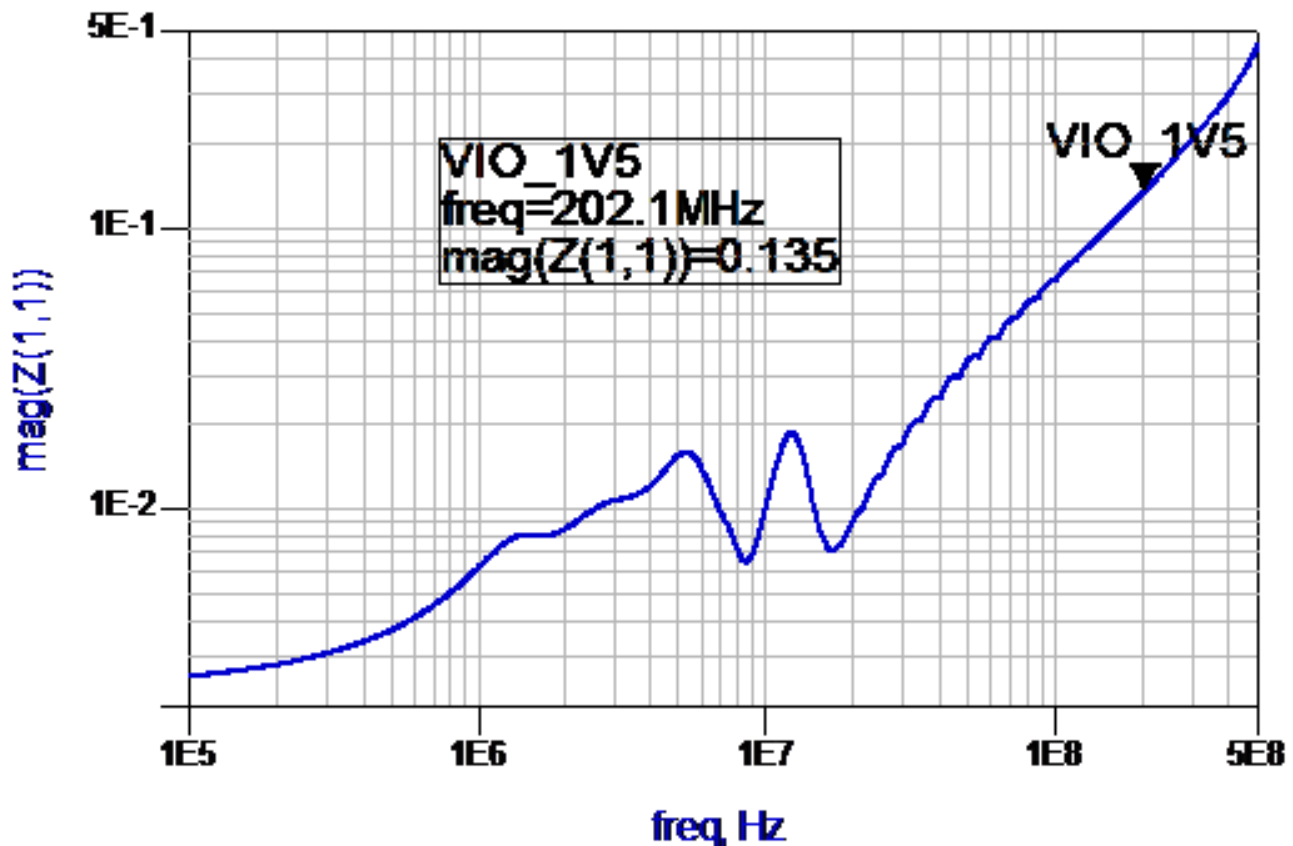


Figure 7-29. VIO_DDR3 PDN Analysis

7.4 Single-Ended Interfaces

7.4.1 General Routing Guidelines

The following paragraphs detail the routing guidelines that must be observed when routing the various functional LVCMOS interfaces:

- Line spacing:
 - For a line width equal to W , the spacing between two lines must be $2 \times W$, at least. This minimizes the crosstalk between switching signals between the different lines. On the PCB, this is not achievable everywhere (for example, when breaking signals out from the Device package), but it is recommended to follow this rule as much as possible. When violating this guideline, minimize the length of the traces running parallel to each other (see [Figure 7-30](#)).

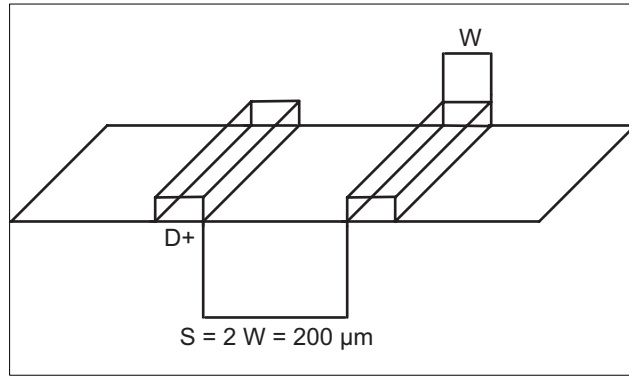


Figure 7-30. Guard Illustration

- Length matching (unless otherwise specified):
 - For bus or traces at frequencies less than 10 MHz: the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 25 mm.
 - For bus or traces at frequencies greater than 10 MHz: the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 2.5 mm.
- Characteristic impedance:
 - Unless otherwise specified, characteristic impedance for single-ended interfaces is recommended to be between 30 and 65 Ω.
- Multiple peripheral support:
 - For interfaces where multiple peripherals have to be supported in a star topology, the length of each branch has to be balanced. Before closing the PCB design, it is highly recommended to verify signal integrity based on simulations including actual PCB extraction.

NOTE

The PCB recommendations described in the next sections make references to the default multiplexing mode signals. Different multiplexing modes other than the default one (usually mode 0) are available and configurable by software programming. For more information, see , *Multiplexing Characteristics*.

7.4.2 Single-Ended PCB Guidelines

The following interfaces follow the general guidelines of single-ended interfaces.

7.4.2.1 GPMC PCB Guidelines

The GPMC interface is used to interface with external memory and in particular supports various flash types [NOR or NAND] and can be set up to support different synchronous and asynchronous protocols.

It can support up to 88.6 MHz in read mode (NOR read synchronous mode) and write mode (NOR write synchronous mode).

Table 7-4 describes the GPMC PCB requirements for NOR and NAND applications.

Table 7-4. GPMC PCB Requirements and IO Programming

| GPMC APPLICATIONS | MAXIMUM NUMBER OF PERIPHERALS | MAXIMUM FREQ. (MHz) | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|--|-------------------------------|---------------------|-------------------|-----|-------------------|-----|------------------------------|-----|----------------------------|----------------------------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| NOR flash read synchronous, write asynchronous | 1 | 88.6 | 4 | 10 | 2 | 10 | 30 | 50 | 0b10 | 0b10 |
| | | | | | | | 51 | 65 | 0b10 | 0b01 |

Table 7-4. GPMC PCB Requirements and IO Programming (continued)

| GPMC APPLICATIONS | MAXIMUM NUMBER OF PERIPHERALS | MAXIMUM FREQ. (MHz) | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|---------------------------------|-------------------------------|---------------------|-------------------------|-------------------------|-------------------|-----|---------------------------------------|-----|----------------------------|----------------------------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| PSRAM read or write synchronous | 1 | 88.6 | 3 | 8 | 2 | 10 | 30 | 50 | 0b10 | 0b10 |
| | | | | | | | 51 | 65 | 0b10 | 0b10 |
| NAND read or write synchronous | Up to 5 | 66.5 | Clock = 12 Data = 16 | Clock = 22 Data = 25 | 2 | 6 | 30 | 50 | 0b10 | 0b01 |
| | | | | | | | 51 | 65 | 0b10 | 0b10 |

7.4.2.2 HSI PCB Guidelines

The HSI interface is a high-speed serial interface that is typically used for communication with a modem. It supports maximum data rates of:

- In receive mode, 225 Mbps @OPP_NOM.
- In transmit mode, 192 Mbps @OPP_NOM.

NOTE

The 1.2-V mode is not supported in the device.

The HSI PCB recommendations are listed in [Table 7-5](#):

Table 7-5. HSI PCB Requirements and IO Programming

| FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | EXTERNAL RESISTANCE ⁽¹⁾ (Ω) | IO REGISTER PROGRAMMING | |
|-------------------|-----|-------------------|-----|---------------------------------------|-----|---|----------------------------|----------------------------|
| MIN | MAX | MIN | MAX | MIN | MAX | | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| 1.5 | | 3 | 5 | 42 | 58 | 50 ⁽²⁾⁽³⁾⁽⁵⁾ | 0b10 | 0b01 |
| | | 5 | 7 | 42 | 58 | 27 ⁽²⁾⁽⁴⁾⁽⁵⁾ | | |
| 2 | 5 | 3 | 5 | 42 | 50 | 10 ⁽⁶⁾ | | |
| | | | | 51 | 58 | 20 ⁽⁶⁾ | | |
| | | 5 | 7 | 42 | 50 | NA | | |
| | | | | 51 | 58 | 10 ⁽⁶⁾ | | |

(1) External serial resistances have to be placed on the adata and aflag PCB traces, close to the OMAP543x device.

(2) External resistance has been characterized with 50- Ω PCB trace.

(3) 50 Ω is the recommended value for a 3-cm PCB trace.

(4) 27 Ω is the recommended value for a 9-cm PCB trace.

(5) For all other PCB trace lengths, external resistance must be tuned between 27 Ω and 50 Ω .

(6) Recommendation for approximate value of external resistances. Values need to be fine tuned based on exact PCB characteristics and timing requirements.

7.4.2.3 SDMMC PCB Guidelines

The Device device supports five SD / MMC Card interfaces.

7.4.2.3.1 SD Card PCB Guidelines

The OMAP5 can support external SD cards according to the SD standard:

- DS—Default speed at 24 MHz, 3-V signaling
- HS—High speed at 48 MHz, 3-V signaling
- SDR12—SDR mode at 24 MHz, 1.8-V signaling
- SDR25—SDR mode at 48 MHz, 1.8-V signaling
- SDR50—SDR mode at 96 MHz, 1.8-V signaling
- SDR104—SDR mode at 192 MHz, 1.8-V signaling
- DDR50—DDR mode at 48 MHz, 1.8-V signaling

7.4.2.3.1.1 SD Card Interface Pin Description

[Table 7-6](#) provides for each SD Card signal the corresponding bottom ball and the IO set name.

Table 7-6. SD Card Interface Signals

| SIGNAL NAME | BOTTOM BALL | IO SET NAME |
|--------------|-------------|-------------------------|
| sdcard_clk | E3 | SDIO Set (1.8 V, 3.0 V) |
| sdcard_cmd | E2 | |
| sdcard_data0 | G3 | |
| sdcard_data1 | G2 | |
| sdcard_data2 | F2 | |
| sdcard_data3 | F3 | |

7.4.2.3.1.2 SD Card PCB Requirements With External SD Card

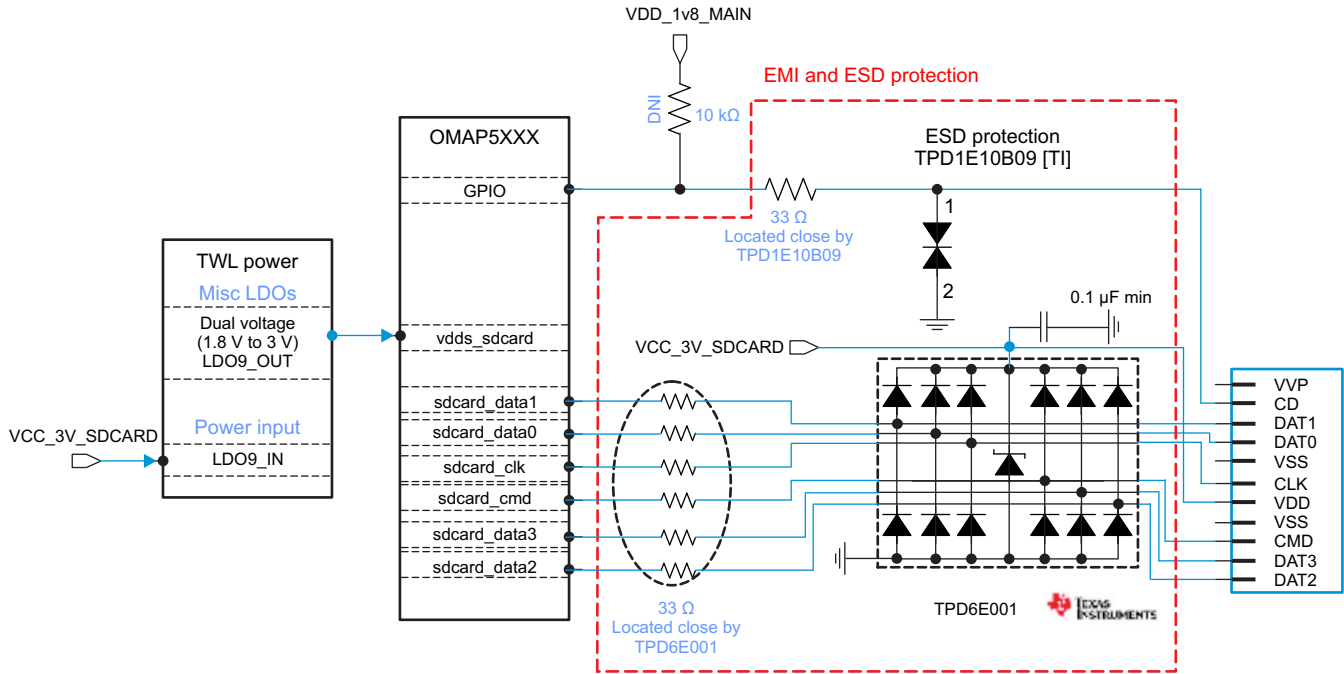
The SD Card PCB recommendations are listed in [Table 7-7](#):

Table 7-7. SD Card PCB Requirements and IO Programming

| SD CARD APPLICATIONS | PERIPHERAL NUMBER | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER PROGRAMMING |
|---|-------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|-------------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | IMPEDANCE ic[1:0] |
| DS—Default speed at 24 MHz, 3-V signaling, SDR, half-cycle mode | 1 | 7 | 10 | 2 | 10 | 30 | 40 | 0b01 (Type A) |
| | | | | | | 41 | 50 | 0b10 (Type C) |
| | | | | | | 51 | 65 | 0b10 (Type C) |
| HS—High speed at 48 MHz, 3-V signaling, SDR, half-cycle mode | 1 | 7 | 10 | 2 | 10 | 30 | 40 | 0b01 (Type A) |
| | | | | | | 41 | 50 | 0b10 (Type C) |
| | | | | | | 51 | 65 | 0b10 (Type C) |
| SDR12 at 24 MHz, 1.8-V signaling, SDR, half-cycle mode | 1 | 7 | 10 | 2 | 10 | 30 | 40 | 0b01 (Type A) |
| | | | | | | 41 | 50 | 0b00 (Type B) |
| | | | | | | 51 | 65 | 0b10 (Type C) |
| SDR25 at 48 MHz, 1.8-V signaling, SDR, half-cycle mode | 1 | 7 | 10 | 2 | 10 | 30 | 40 | 0b01 (Type A) |
| | | | | | | 41 | 50 | 0b00 (Type B) |
| | | | | | | 51 | 65 | 0b10 (Type C) |
| SDR50 at 96 MHz, 1.8-V signaling, SDR, half-cycle mode | 1 | 7 | 10 | 2 | 10 | 30 | 40 | 0b01 (Type A) |
| | | | | | | 41 | 50 | 0b00 (Type B) |
| | | | | | | 51 | 65 | 0b10 (Type C) |
| DDR50 at 48 MHz, 1.8-V signaling DDR | 1 | 7 | 10 | 2 | 10 | 30 | 40 | 0b01 (Type A) |
| | | | | | | 41 | 50 | 0b00 (Type B) |
| | | | | | | 51 | 65 | 0b10 (Type C) |
| SDR104 at 192 MHz, 1.8-V signaling, SDR, half-cycle mode | 1 | 7 | 10 | 2 | 10 | 30 | 40 | 0b01 (Type A) |
| | | | | | | 41 | 50 | 0b00 (Type B) |
| | | | | | | 51 | 65 | 0b10 (Type C) |

7.4.2.3.1.3 SD Card System ESD With External SD Card Configuration**NOTE**

For more information on system ESD or EMI / EMC, see [Section 7.2.5, System ESD Generic Guidelines](#) and [Section 7.2.6, EMI / EMC Issues Prevention](#).



SWPS049-001

Figure 7-31. SD Card Implementation Proposal With External SD Card

Table 7-8. SD Card Component Reference

| INTERFACE | DEVICE | SUPPLIER | PART NUMBER |
|-----------|--------|----------|---|
| SD Card | TVS | TI | TPD6E001RSE |
| | TVS | TI | TPD1E10B09 |
| | CFB | Murata | [600R / 100M / 0402] BLM15AG601SN1 |
| | C | Murata | [0.1 μF / 10 V / 0402] GRM155R71A104KA0 |
| | R | - | 33 Ω |

Some guidelines regarding SD Card system ESD:

- SD connector may have card detect and write protect pins, consider using an ESD external protection device with low turn-on resistance ($R_{dyn} = 1 \Omega$).
- TPD1E10B09 being asymmetrical, it is recommended to respect the mounting configuration (1: signal, 2: ground).

CAUTION

System level ESD results are dependent on the components being connected to the product.

Part numbers that are different than the reference board specification (see [Table 7-8, SD Card Component Reference](#)) are not assured to meet system level ESD requirements.

7.4.2.3.2 WLSPIO (SDIO3) PCB Guidelines

The OMAP5 can support on-board peripherals compliant with the SD standard:

- SDR12—SDR mode at 24 MHz
- SDR25—SDR mode at 48 MHz

The WLSPIO (SDIO3) PCB recommendations are listed in [Table 7-9](#):

Table 7-9. WLSADIO PCB Requirements and IO Programming

| WLSADIO APPLICATION | PERIPHERAL NUMBER | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER PROGRAMMING | |
|---|-------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|-------------------------|-------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE SC[1:0] | IMPEDANCE DS[1:0] |
| SDR12—SDR mode at 24 MHz, half-cycle mode | 1 | 2.5 | 5 | 2 | 10 | 30 | 40 | 0b10 | 0b10 |
| | | | | | | 41 | 50 | 0b10 | 0b01 |
| | | | | | | 51 | 65 | 0b10 | 0b01 |
| SDR25—SDR mode at 48 MHz, half-cycle mode | 1 | 2.5 | 5 | 2 | 10 | 30 | 40 | 0b10 | 0b10 |
| | | | | | | 41 | 50 | 0b10 | 0b01 |
| | | | | | | 51 | 65 | 0b10 | 0b01 |

7.4.2.3.3 SDIO4 PCB Guidelines

The device can support on-board peripherals compliant with the SD standard:

- SDR12—SDR mode at 24 MHz
- SDR25—SDR mode at 48 MHz

The SDIO4 PCB recommendations are listed in [Table 7-10](#):

Table 7-10. SDIO4 PCB Requirements and IO Programming

| SDIO4 APPLICATION | PERIPHERAL NUMBER | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER PROGRAMMING | |
|---|-------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|-------------------------|-------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE SC[1:0] | IMPEDANCE DS[1:0] |
| SDR12—SDR mode at 24 MHz, half-cycle mode | 1 | 2.5 | 5 | 2 | 10 | 30 | 40 | 0b10 | 0b10 |
| | | | | | | 41 | 50 | 0b10 | 0b01 |
| | | | | | | 51 | 65 | 0b10 | 0b01 |
| SDR25—SDR mode at 48 MHz, half-cycle mode | 1 | 2.5 | 5 | 2 | 10 | 30 | 40 | 0b10 | 0b10 |
| | | | | | | 41 | 50 | 0b10 | 0b01 |
| | | | | | | 51 | 65 | 0b10 | 0b01 |

7.4.2.3.4 eMMC PCB Guidelines

The eMMC interface supports 1.2-V and 1.8-V operations.

7.4.2.3.4.1 eMMC Interface

The eMMC interface is used to interface with external memory. It can support the eMMC JC64 standard:

- Standard JC64 SDR at 24 MHz
- High-speed JC64 SDR at 48 MHz
- High-speed JC64 DDR at 48 MHz
- High-speed HS200 JC64 SDR at 192 MHz

7.4.2.3.4.2 eMMC PCB Requirements

The eMMC PCB recommendations are listed in [Table 7-11](#):

Table 7-11. eMMC PCB Requirements and IO Programming

| eMMC APPLICATION | PERIPHERAL NUMBER | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER PROGRAMMING | |
|---|-------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|-------------------------|-------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE SC[1:0] | IMPEDANCE DS[1:0] |
| Standard JC64 SDR at 24 MHz, half-cycle mode | 1 | 2.5 | 5 | 2 | 10 | 30 | 40 | 0b10 | 0b10 |
| | | | | | | 41 | 50 | 0b10 | 0b01 |
| | | | | | | 51 | 65 | 0b10 | 0b01 |
| High-speed JC64 SDR at 48 MHz, half-cycle mode | 1 | 2.5 | 5 | 2 | 10 | 30 | 40 | 0b10 | 0b10 |
| | | | | | | 41 | 50 | 0b10 | 0b01 |
| | | | | | | 51 | 65 | 0b10 | 0b01 |
| High-speed JC64 DDR at 48 MHz | 1 | 2.5 | 5 | 2 | 10 | 30 | 40 | 0b10 | 0b10 |
| | | | | | | 41 | 50 | 0b10 | 0b01 |
| | | | | | | 51 | 65 | 0b10 | 0b01 |
| High-speed HS200 JC64 SDR at 192 MHz, half-cycle mode | 1 | 2.5 | 5 | 2 | 10 | 30 | 35 | 0b11 | 0b11 |
| | | | | | | 36 | 45 | 0b11 | 0b10 |
| | | | | | | 46 | 65 | 0b11 | 0b01 |

7.4.2.4 SPI PCB Guidelines

The OMAP5 processor provides four SPI interfaces:

- SPI1 and SPI2 are used in master mode only.
- SPI3 and SPI4 can be used in master or slave mode.

See the following sections for a complete description of the different SPI configurations supported by the device.

7.4.2.4.1 SPI1 Interface

The maximum speed of the SPI1 interface in master mode is 48 MHz, 24 MHz, or 12 MHz depending on the number of external peripherals.

The SPI interface 1 PCB recommendations are listed in [Table 7-12](#):

Table 7-12. SPI1 PCB Requirements and IO Programming⁽¹⁾⁽²⁾

| SPI1 APPLICATION | PERIPHERAL NUMBER | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER PROGRAMMING | |
|--|-------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|-------------------------|-------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE SC[1:0] | IMPEDANCE DS[1:0] |
| 12-MHz master mode | 2 | 7 | 10 | 4 | 10 | 30 | 65 | 0b01 | 0b00 |
| 24-MHz master mode | 2 | 7 | 10 | 2 | 10 | 30 | 65 | 0b01 | 0b00 |
| 48-MHz master mode | 1 | 2.5 | 5 | 2 | 10 | 30 | 65 | 0b10 | 0b01 |
| 12-MHz master mode—bidirectional simo signal (somi unused) | 1 | 2.5 | 5 | 1 | 10 | 30 | 65 | 0b10 | 0b00 |

(1) Bussed signals (mcspi1_clk, mcspi1_simo, and mcspi1_somi) must be T-routed or star routed.

(2) Chip selects (mcspi1_cs[3:0]) are point-to-point routed.

7.4.2.4.2 SPI2 Interface

The maximum speed of the SPI2 interface in master mode is 48 MHz, 24 MHz, or 12 MHz depending on the number of external peripherals.

The SPI interface 2 PCB recommendations are listed in [Table 7-13](#):

Table 7-13. SPI2 PCB Requirements and IO Programming⁽¹⁾⁽²⁾

| SPI2 APPLICATION | PERIPHERAL NUMBER | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER PROGRAMMING | |
|--|-------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|-------------------------|-------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE SC[1:0] | IMPEDANCE DS[1:0] |
| 12-MHz master mode | 2 | 7 | 10 | 4 | 10 | 30 | 65 | 0b01 | 0b00 |
| 24-MHz master mode | 2 | 7 | 10 | 2 | 10 | 30 | 65 | 0b01 | 0b00 |
| 48-MHz master mode | 1 | 2.5 | 5 | 2 | 10 | 30 | 65 | 0b10 | 0b01 |
| 12-MHz master mode—bidirectional simo signal (somi unused) | 1 | 2.5 | 5 | 1 | 10 | 30 | 65 | 0b10 | 0b00 |

(1) Bussed signals (mcspi2_clk, mcspi2_simo, and mcspi2_somi) must be T-routed or star routed.

(2) Chip selects (mcspi2_cs[1:0]) are point-to-point routed.

7.4.2.4.3 SPI3 Interface

The maximum speed of the SPI3 interface is 48 MHz in master mode and 24 MHz in slave mode. Only 1 external peripheral is supported.

The SPI interface 3 PCB recommendations are listed in [Table 7-14](#):

Table 7-14. SPI3 PCB Requirements and IO Programming

| SPI3 APPLICATION | PERIPHERAL NUMBER | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER PROGRAMMING | |
|--------------------|-------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|-------------------------|-------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE SC[1:0] | IMPEDANCE DS[1:0] |
| 16-MHz slave mode | 1 | 2.5 | 5 | 2 | 10 | 30 | 65 | 0b10 | 0b00 |
| 48-MHz master mode | 1 | 2.5 | 5 | 2 | 10 | 30 | 65 | 0b10 | 0b01 |

7.4.2.4.4 SPI4 Interface

The maximum speed of the SPI4 interface is 48 MHz in master mode and 24 MHz in slave mode. Only 1 external peripheral is supported.

The SPI interface 4 PCB recommendations are listed in [Table 7-15](#):

Table 7-15. SPI4 PCB Requirements and IO Programming

| SPI4 APPLICATION | PERIPHERAL NUMBER | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER PROGRAMMING | |
|--------------------|-------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|-------------------------|-------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE SC[1:0] | IMPEDANCE DS[1:0] |
| 16-MHz slave mode | 1 | 2.5 | 5 | 2 | 10 | 30 | 65 | 0b10 | 0b00 |
| 48-MHz master mode | 1 | 2.5 | 5 | | 10 | 30 | 65 | 0b10 | 0b01 |

7.4.2.5 USB PCB Guidelines

The device features two USB controllers which support the following configurations:

- The first controller (USB0, USB SS DRD controller) supports the following protocols:
 - High-speed [480 Mbits] DRD with OMAP5 embedded PHY.

NOTE

For more information on USB0 PHY in HS, see [Section 7.5.3.1, USB High-Speed PHY Interface \(480 Mbps\)](#).

- Super-speed [5 Gbits] DRD with OMAP5 embedded PHY.

NOTE

For more information on USB0 PHY in super speed, see [, USB Super-Speed PHY Interface \(5 Gbps\)](#).

- High-speed [480 Mbits] DRD ULPI PHY implementation.

NOTE

For more information on USB0 ULPI PHY PCB recommendations, see [Section 7.4.2.5.1, USB0 \(USB SS DRD Controller\) ULPI PHY Interface](#).

- The second controller (USB1, host controller) supports, on three different ports, B1, B2, and B3, the following protocols:

- Port B1:
 - High-speed [480 Mbits] HS IC interchip 2-pin configuration
 - High-speed [480 Mbits] ULPI PHY implementation

NOTE

For more information on USB1 HSIC or ULPI PHY PCB recommendations, see [Section 7.4.2.5.2, USB1 \(Host Controller\) Interface](#).

- Port B2:
 - High-speed [480 Mbits] HS IC interchip 2-pin configuration
 - High-speed [480 Mbits] ULPI TLL PHY implementation
 - Low-speed and Full-speed [12 Mbits] multimode implementations in 2-, 3-, 4-, or 6-pin configuration

NOTE

For more information on USB1 HSIC or ULPI PHY PCB recommendations, see [Section 7.4.2.5.3, USB2 \(Host Controller\) Interface](#).

- Port B3:
 - High-speed [480 Mbits] HS IC interchip 2-pin configuration

NOTE

For more information on USB1 HSIC or ULPI PHY PCB recommendations, see [Section 7.4.2.5.4, USB3 \(Host Controller\) Interface](#).

7.4.2.5.1 USB0 (USB SS DRD Controller) ULPI PHY Interface

[Table 7-16](#) describes the USB0 ULPI PHY PCB requirements.

Table 7-16. USB0 ULPI PHY PCB Requirements and IO Programming

| USB0 ULPI PHY APPLICATION | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|---|-------------------|-----|-------------------|-----|---------------------------------------|-----|----------------------------|----------------------------|
| | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| 60 MHz ULPI Slave mode SDR—8 data bits | 2.5 | 5 | 1 | 10 | 30 | 40 | 0b10 | 0b10 |
| | | | | | 41 | 50 | 0b10 | 0b10 |
| | | | | | 51 | 65 | 0b10 | 0b01 |

7.4.2.5.2 USB1 (Host Controller) Interface**7.4.2.5.2.1 USB1 (Host Controller) High-Speed Interchip (HSIC)—2 Pins**

This implementation supports HS (480 Mbps) in 2-pin configuration at 1.2 V.

Table 7-17 describes the USB1 HSIC PCB requirements.

Table 7-17. USB1 HSIC PCB Requirements and IO Programming

| USB1 HSIC APPLICATION ⁽¹⁾ | TRACE LENGTH (cm) | | FAR-END LOAD (pF) | | NEAR END EXTERNAL RESISTOR REQUIRED ⁽²⁾ (O) | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | | |
|--|-------------------|-------------------|-------------------|--------------|--|---------------------------------------|-----|----------------------------|---------------------------|---------------------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | SLEW RATE REGISTER SR[1:0] | IMPEDANCE REGISTER I[1:0] | |
| USB1 HOST HSIC 480 Mbps 2-pin asynchronous | 0 | 2 | 3 | | 39 | 45 | 55 | 0b10 | 0b00 | |
| | | | 4 | | 39 | 45 | 55 | 0b10 | 0b01 ⁽³⁾ | |
| | | | 5 | | 33 | 45 | 55 | 0b10 | 0b01 | |
| | | | 6 | | 22 | 45 | 55 | 0b10 | 0b01 | |
| | | | 7 | | 10 | 45 | 55 | 0b10 | 0b01 | |
| | | | 8 | 9 | not required | | 45 | 55 | 0b10 | 0b01 |
| | | | 10 | | not required | | 45 | 55 | 0b10 | 0b10 |
| | >2 | 6 | 3 | | 22 | 45 | 55 | 0b10 | 0b01 ⁽³⁾ | |
| | | | 4 | | 18 | 45 | 55 | 0b10 | 0b01 ⁽³⁾ | |
| | | | 5 | | 15 | 45 | 55 | 0b10 | 0b01 | |
| | | | 6 | 10 | not required | | 45 | 55 | 0b10 | 0b01 ⁽³⁾ |
| | >6 | 10 ⁽⁴⁾ | 3 | 4 | not required | | 45 | 55 | 0b10 | 0b00 ⁽³⁾ |
| | | | 5 | | 10 | | 45 | 55 | 0b10 | 0b01 |
| | | | 6 | 8 | not required | | 45 | 55 | 0b10 | 0b01 |
| 9 | | | 10 | not required | | 45 | 55 | 0b10 | 0b10 | |
| PARAMETER | | | | | | VALUE | | UNIT | | |
| Skew due to crosstalk between data and strobe signals, including board skew ⁽⁵⁾ | | | | | | MIN | MAX | | | |
| | | | | | | | 50 | ps | | |

(1) Recommendations of the table are valid for a skew between the strobe and data signals of 50 ps. This skew value includes the crosstalk between signals and the trace length uncertainty.

(2) For some specific cases, external resistors have to be added for the data and strobe PCB traces to fulfill the slew rate defined by the High-Speed Inter-Chip USB (v1.0) specification. Resistors have to be located as close as possible to the device.

(3) For some specific cases, the High-Speed Inter-Chip USB (v1.0) specification is not fully verified from a slew rate perspective, the rise and fall times can be faster. No functional issue is expected, but a bit higher than in the specification.

(4) To ensure performances with interconnect length up to 10 cm, the coupling between lines has to be minimized. Spacing between the strobe and data lines must be $> 3 \times W$ ($5 \times W$ recommended).

(5) This skew budget includes the effect of the crosstalk between the traces and the PCB trace length uncertainty.

7.4.2.5.2.2 USB1 (Host Controller)—ULPI PHY

This interface operates at 480 Mbps in high-speed mode with external PHY transceiver.

Table 7-18 describes the USB1 ULPI PHY PCB requirements.

Table 7-18. USBB1 ULPI PHY PCB Requirements and IO Programming

| USBB2 ULPI PHY APPLICATION | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|--|-------------------|-----|-------------------|-----|---------------------------------------|-----|----------------------------|----------------------------|
| | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| USBB1 (HOST controller) 60 MHz ULPI slave mode SDR—8 data bits | 2.5 | 5 | 1 | 10 | 30 | 40 | 0b10 | 0b10 |
| | | | | | 41 | 50 | 0b10 | 0b10 |
| | | | | | 51 | 65 | 0b10 | 0b01 |

7.4.2.5.3 USBB2 (Host Controller) Interface

7.4.2.5.3.1 USBB2 (Host Controller) HSIC—2 Pins

This implementation supports high-speed (480 Mbits) in 2-pin configuration at 1.2 V.

Table 7-19 describes the USBB2 HSIC PCB requirements.

Table 7-19. USBB2 HSIC PCB Requirements and IO Programming

| USBB2 HSIC APPLICATION ⁽¹⁾ | TRACE LENGTH (cm) | | FAR-END LOAD (pF) | | NEAR END EXTERNAL RESISTOR REQUIRED ⁽²⁾ (O) | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|--|-------------------|-------------------|-------------------|-----|--|---------------------------------------|-----|----------------------------|---------------------------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | SLEW RATE REGISTER SR[1:0] | IMPEDANCE REGISTER I[1:0] |
| USBB1 HOST HSIC 480 Mbits 2-pin asynchronous | 0 | 2 | 3 | | 39 | 45 | 55 | 0b10 | 0b00 |
| | | | 4 | | 39 | 45 | 55 | 0b10 | 0b01 ⁽³⁾ |
| | | | 5 | | 33 | 45 | 55 | 0b10 | 0b01 |
| | | | 6 | | 22 | 45 | 55 | 0b10 | 0b01 |
| | | | 7 | | 10 | 45 | 55 | 0b10 | 0b01 |
| | | | 8 | 9 | not required | 45 | 55 | 0b10 | 0b01 |
| | | | 10 | | not required | 45 | 55 | 0b10 | 0b10 |
| | >2 | 6 | 3 | | 22 | 45 | 55 | 0b10 | 0b01 ⁽³⁾ |
| | | | 4 | | 18 | 45 | 55 | 0b10 | 0b01 ⁽³⁾ |
| | | | 5 | | 15 | 45 | 55 | 0b10 | 0b01 |
| | | | 6 | 10 | not required | 45 | 55 | 0b10 | 0b01 ⁽³⁾ |
| | >6 | 10 ⁽⁴⁾ | 3 | 4 | not required | 45 | 55 | 0b10 | 0b00 ⁽³⁾ |
| | | | 5 | | 10 | 45 | 55 | 0b10 | 0b01 |
| | | | 6 | 8 | not required | 45 | 55 | 0b10 | 0b01 |
| | | | 9 | 10 | not required | 45 | 55 | 0b10 | 0b10 |
| PARAMETER | | | | | | VALUE | | UNIT | |
| | | | | | | MIN | MAX | | |
| Skew due to crosstalk between data and strobe signals, including board skew ⁽⁵⁾ | | | | | | | 50 | ps | |

(1) Recommendations of the table are valid for a skew between the strobe and data signals of 50 ps. This skew value includes the crosstalk between signals and the trace length uncertainty.

(2) For some specific cases, external resistors have to be added for the data and strobe PCB traces to fulfill the slew rate defined by the High-Speed Inter-Chip USB (v1.0) specification. Resistors have to be located as close as possible to the device.

(3) For some specific cases, the High-Speed Inter-Chip USB (v1.0) specification is not fully verified from slew rate perspective, the rise and fall times can be faster. No functional issue expected but a bit higher than in the specification.

(4) To ensure performances with interconnect length up to 10 cm, the coupling between lines has to be minimized. Spacing between the strobe and data lines must be $> 3 \times W$ ($5 \times W$ recommended).

(5) This skew budget includes the effect of the crosstalk between the traces and the PCB trace length uncertainty.

7.4.2.5.3.2 USB2 (Host Controller)—ULPI TLL PHY

This USB2 TLL PHY interface operates at 480 Mbits in HS without an external PHY transceiver (transceiverless link).

Table 7-20 describes the USB2 ULPI PHY PCB requirements.

Table 7-20. USB2 ULPI TLL PHY PCB Requirements and IO Programming

| USB2 ULPI PHY TLL APPLICATION | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|---|-------------------|-----|-------------------|-----|--|-----|----------------------------------|----------------------------------|
| | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| USB2 (HOST controller) 60 MHz ULPI Slave mode SDR —8 data bits | 2.5 | 5 | 1 | 10 | 30 | 40 | 0b10 | 0b10 |
| | | | | | 41 | 50 | 0b10 | 0b10 |
| | | | | | 51 | 65 | 0b10 | 0b01 |

7.4.2.5.3.3 USB2 (Host Controller)—Low-Speed / Full-Speed Multimode Interface

This interface supports low- / full-speed multimode implementations in 2-, 3-, 4-, or 6-pin configuration and is multiplexed twice on the OMAP5 device.

Table 7-21 describes the USB2 low-speed / full-speed multimode PCB requirements.

Table 7-21. USB2 Low-Speed / Full-Speed Multimode PCB Requirements and IO Programming

| USB2 LOW-/ FULL-SPEED MULTIMODE APPLICATION | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|---|-------------------|-----|-------------------|-----|--|-----|----------------------------------|----------------------------------|
| | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| USB2 (HOST controller) Up to 12 MHz low- / full-speed multimode | 2.5 | 5 | 1 | 10 | 30 | 40 | 0b01 | 0b11 |
| | | | | | 41 | 50 | 0b01 | 0b10 |
| | | | | | 51 | 65 | 0b01 | 0b01 |

7.4.2.5.4 USB3 (Host Controller) Interface

7.4.2.5.4.1 USB3 (Host Controller) HSIC—2 Pins

This implementation supports HS (480 Mbits) in 2-pin configuration at 1.2 V.

Table 7-22 describes the USB3 HSIC PCB requirements.

Table 7-22. USB3 HSIC PCB Requirements and IO Programming

| USB3 HSIC APPLICATION ⁽¹⁾ | TRACE LENGTH (cm) | | FAR-END LOAD (pF) | | NEAR END EXTERNAL RESISTOR REQUIRED ⁽²⁾ (Ω) | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | | |
|---|-------------------|-------------------|-------------------|-----|--|------------------------------|-----|----------------------------|---------------------------|---------------------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | SLEW RATE REGISTER SR[1:0] | IMPEDANCE REGISTER I[1:0] | |
| USB31 HOST HSIC 480 Mbits 2-pin asynchronous | 0 | 2 | 3 | | 39 | 45 | 55 | 0b10 | 0b00 | |
| | | | 4 | | 39 | 45 | 55 | 0b10 | 0b01 ⁽³⁾ | |
| | | | 5 | | 33 | 45 | 55 | 0b10 | 0b01 | |
| | | | 6 | | 22 | 45 | 55 | 0b10 | 0b01 | |
| | | | 7 | | 10 | 45 | 55 | 0b10 | 0b01 | |
| | | | 8 | 9 | not required | | 45 | 55 | 0b10 | 0b01 |
| | | | 10 | | not required | | 45 | 55 | 0b10 | 0b10 |
| | >2 | 6 | 3 | | 22 | 45 | 55 | 0b10 | 0b01 ⁽³⁾ | |
| | | | 4 | | 18 | 45 | 55 | 0b10 | 0b01 ⁽³⁾ | |
| | | | 5 | | 15 | 45 | 55 | 0b10 | 0b01 | |
| | | | 6 | 10 | not required | | 45 | 55 | 0b10 | 0b01 ⁽³⁾ |
| | >6 | 10 ⁽⁴⁾ | 3 | 4 | not required | | 45 | 55 | 0b10 | 0b00 ⁽³⁾ |
| | | | 5 | | 10 | 45 | 55 | 0b10 | 0b01 | |
| | | | 6 | 8 | not required | | 45 | 55 | 0b10 | 0b01 |
| | | | 9 | 10 | not required | | 45 | 55 | 0b10 | 0b10 |
| PARAMETER | | | | | | VALUE | | UNIT | | |
| | | | | | | MIN | MAX | | | |
| Skew due to cross talk between data and strobe signals, including board skew ⁽⁵⁾ | | | | | | | 50 | ps | | |

- (1) Recommendations of the table are valid for a skew between the strobe and data signals of 50 ps. This skew value includes the crosstalk between signals and the trace length uncertainty.
- (2) For some specific cases, external resistors have to be added for the data and strobe PCB traces to fulfill the slew rate defined by the High-Speed Inter-Chip USB (v1.0) specification. Resistors have to be located as close as possible to the device.
- (3) For some specific cases, the high-speed interchip USB (v1.0) specification is not fully verified from slew rate perspective, the rise and fall times can be faster. No functional issue expected but a bit higher than in the specification.
- (4) To ensure performances with interconnect length up to 10 cm, the coupling between lines has to be minimized. Spacing between the strobe and data lines must be $> 3 \times W$ ($5 \times W$ recommended).
- (5) This skew budget includes the effect of the crosstalk between the traces and the PCB trace length uncertainty.

7.4.2.6 Audio McBSP PCB Guidelines

The OMAP5 provides three McBSP interfaces. These interfaces are used for transmission of audio to or from various peripherals.

7.4.2.6.1 McBSP1 Interface

McBSP1 interface supports different modes: half- or full-cycle mode, master-slave and TDM multichannel configuration.

The McBSP1 interface PCB recommendations are listed in [Table 7-23](#):

Table 7-23. McBSP1 PCB Requirements and IO Programming

| McBSP1 APPLICATION | PERIPHERAL NUMBER | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER PROGRAMMING | |
|---|-------------------|-------------------|-----|-------------------|-----|------------------------------|-----|-------------------------|-------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE SC[1:0] | IMPEDANCE DS[1:0] |
| I2S format (non-TDM mode), master or slave mode, full- or half-cycle mode at 12.288 MHz | 1 | 2.5 | 5 | 1 | 10 | 30 | 40 | 0b10 | 0b10 |
| | | | | | | 41 | 50 | 0b10 | 0b10 |
| | | | | | | 51 | 65 | 0b10 | 0b01 |

Table 7-23. McBSP1 PCB Requirements and IO Programming (continued)

| McBSP1 APPLICATION | PERIPHERAL NUMBER | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER PROGRAMMING | |
|--|-------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|-------------------------|-------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE SC[1:0] | IMPEDANCE DS[1:0] |
| I2S format in TDM mode, multiple peripherals, master or slave mode, half-cycle mode at 6.144 MHz | up to 5 | 5 | 25 | 1 | 10 | 30 | 40 | 0b00 | 0b00 |
| | | | | | | 41 | 50 | 0b00 | 0b00 |
| | | | | | | 51 | 65 | 0b00 | 0b00 |
| I2S format in TDM mode, single peripheral, slave mode, full-cycle mode at 49.12 MHz (input only) | 1 | 2.5 | 5 | 2.5 | 5 | 30 | 40 | 0b10 | 0b10 |
| | | | | | | 41 | 50 | 0b10 | 0b10 |
| | | | | | | 51 | 65 | 0b10 | 0b01 |

7.4.2.6.2 McBSP2 Interface

McBSP2 interface supports different modes: half- or full-cycle mode, master-slave.

The McBSP2 interface PCB recommendations are listed in [Table 7-24](#):

Table 7-24. McBSP2 PCB Requirements and IO Programming

| McBSP2 APPLICATION | PERIPHERAL NUMBER | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER PROGRAMMING | |
|---|-------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|-------------------------|-------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE SC[1:0] | IMPEDANCE DS[1:0] |
| I2S format (non-TDM mode), master or slave mode, full- or half-cycle mode at 12.288 MHz | 2 | 7 | 10 | 1 | 10 | 30 | 40 | 0b01 | 0b00 |
| I2S format in TDM mode, single peripheral, master or slave mode, full- or half-cycle mode at 12.288 MHz | 1 | 2.5 | 5 | 2.5 | 5 | 30 | 40 | 0b10 | 0b10 |
| | | | | | | 41 | 50 | 0b10 | 0b10 |
| | | | | | | 51 | 65 | 0b10 | 0b01 |

7.4.2.6.3 McBSP3 Interface

McBSP3 interface is multiplexed twice on the device and supports different modes: half- or full-cycle mode, master-slave.

The McBSP3 interface PCB recommendations are listed in [Table 7-25](#):

Table 7-25. McBSP3 PCB Requirements and IO Programming

| McBSP3 APPLICATION | PERIPHERAL NUMBER | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER PROGRAMMING | |
|---|-------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|-------------------------|-------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE SC[1:0] | IMPEDANCE DS[1:0] |
| I2S format (non-TDM mode), master or slave mode, full- or half-cycle mode at 12.288 MHz | 2 | 7 | 10 | 1 | 10 | 30 | 40 | 0b01 | 0b00 |
| I2S format in TDM mode, single peripheral, master or slave mode, full- or half-cycle mode at 12.288 MHz | 1 | 2.5 | 5 | 2.5 | 5 | 30 | 40 | 0b10 | 0b10 |
| | | | | | | 41 | 50 | 0b10 | 0b10 |
| | | | | | | 51 | 65 | 0b10 | 0b01 |

7.4.2.7 Audio PCB Guidelines

This section describes the other audio interfaces of the device implemented in the audio back-end module. For more information on the overall audio scheme and implementation proposals, see the OMAP543x TRM.

7.4.2.7.1 Audio—McPDM interface

McPDM is a proprietary interface based on multichannel pulse density modulation. This interface supports 5 downlink and 2 uplink channels, and operates up to 19.2 Mbps.

[Table 7-26](#) describes the audio—McPDM PCB requirements.

Table 7-26. Audio—McPDM PCB Requirements and IO Programming

| McPDM APPLICATION | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|--------------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|----------------------------|----------------------------|
| | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| up to 19.2 Mbps McPDM | 7 | 10 | 1 | 10 | 30 | 40 | 0b01 | 0b00 |
| | | | | | 41 | 50 | 0b01 | 0b00 |
| | | | | | 51 | 65 | 0b01 | 0b00 |

7.4.2.7.2 Audio—DMIC Interface

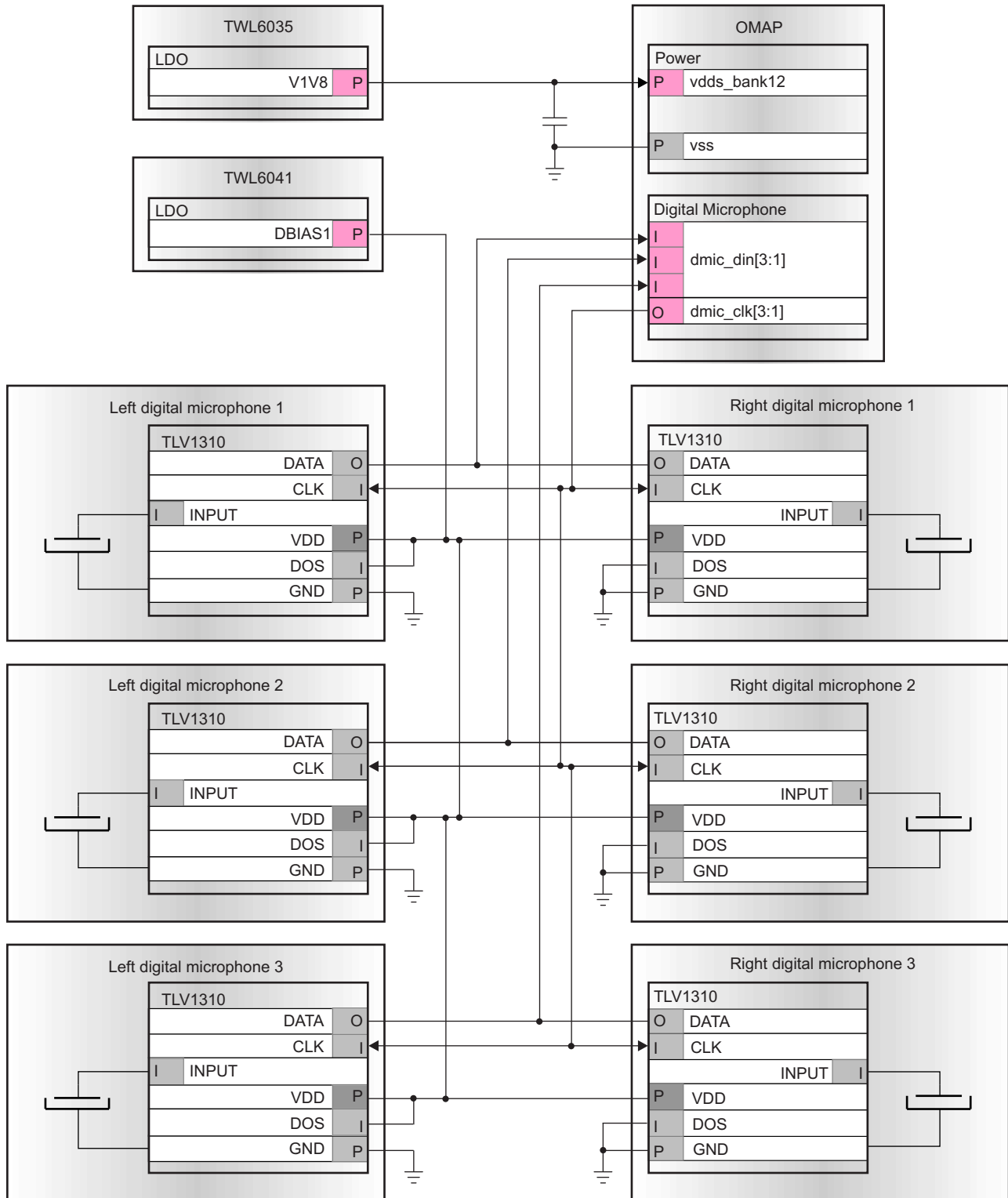
DMIC interface operates at 3.84 MHz with external digital microphones.

[Table 7-27](#) describes the audio—DMIC PCB requirements.

Table 7-27. Audio—DMIC PCB Requirements and IO Programming

| DMIC APPLICATION | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|----------------------------|----------------------------|
| | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| 3.84-MHz DMIC | 7 | 10 | | 25 | 30 | 40 | 0b00 | 0b00 |
| | | | | | 41 | 50 | 0b00 | 0b00 |
| | | | | | 51 | 65 | 0b00 | 0b00 |

Figure 7-32 describes a DMIC implementation proposal.



SWPS049-014

Figure 7-32. DMIC Implementation Proposal

(1) It is not recommended to use different PCB guideline clock outputs rather than sharing one as described in the above implementation.

In such case, each pair (pair [3:1]) of digital microphones can be connected to a dedicated data and clock signals (dmic_din[3:1], dmic_clk[3:1]). This way each microphone is turned on or off independently from the others.

7.4.2.7.3 Audio—McASP Interface

Table 7-28 describes the audio—McASP PCB requirements.

Table 7-28. Audio—McASP PCB Requirements and IO Programming

| McASP APPLICATION | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|----------------------------------|-------------------|-----|-------------------|-----|---------------------------------------|-------------------|----------------------------|----------------------------|
| | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| McASP S/PDIF mode 24.576 Mbits/s | 5 | 10 | 10 | 30 | 45 | 85 ⁽¹⁾ | 0b01 | 0b00 |

(1) PCB impedance is extended to 85 Ω to support 75- Ω coaxial cable as defined in the S/PDIF standard. For long coaxial cable (up to 10 m), a redriver has to be implemented on the PCB, close to the coaxial cable connector.

7.4.2.8 Display Parallel Interface PCB Guidelines

This section addresses the parallel display interface.

7.4.2.8.1 Display Parallel Interface (DPI) Interface

The OMAP5432 processor provides a 24-bit parallel display subsystem (DSS) interface running up to 170 MHz.

Table 7-29 describes the display parallel interface PCB requirements.

Table 7-29. Display Parallel Interface (DPI) PCB Requirements and IO Programming

| DPI APPLICATION | NUMBER OF PERIPHERALS | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|---|-----------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|----------------------------|----------------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| DPI—24-bit display extension at 170 MHz (bridge to display port or DSI) | 1 | 2.5 | 5 | 1 | 5 | 30 | 40 | 0b10 | 0b11 |
| | | | | | | 41 | 50 | 0b10 | 0b10 |
| | | | | | | 51 | 60 | 0b10 | 0b01 |

7.4.2.8.2 Remote Frame Buffer Interface (RFBI) Interface

The processor provides a 16-bit RFBI running up to 30 Mbps.

Table 7-30 describes the remote frame buffer interface PCB requirements.

Table 7-30. Remote Frame Buffer Interface PCB Requirements and IO Programming

| RFBI APPLICATION | NUMBER OF PERIPHERALS | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|------------------------------------|-----------------------|-------------------|-----|-------------------|-----|---------------------------------------|-----|----------------------------|----------------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| RFBI 16 bits at 30 Mbps (Pico DLP) | 1 | 2.5 | 5 | 1 | 10 | 30 | 65 | 0b10 | 0b01 |

7.4.2.9 I²C Interface PCB Guidelines

The Device processor provides five I²C interfaces. The I²C interface supports the high-speed mode at 3.8 MHz and fast mode at 400 kHz.

It additionally provides a fifth I²C interface (sr_pmic_scl and sr_pmic_sda) that is dedicated to controlling the SmartReflex circuitry within the power IC companion chip.

I²C rise time is specified for loads up to 80 pF in high-speed mode and 150 pF in fast mode.

LB[1:0] register can select the appropriate pullup resistor for given load range.

Table 7-31 describes the I²C interface PCB requirements.

Table 7-31. I²C Pulls and Load Description

| PARAMETER | | MIN | NOM | MAX | UNIT | |
|-----------|---|-----------------|-----------------|--|--|----|
| RINPU | Internal pullup resistance for a given load range | LB[1:0] = 00 | High-speed mode | | 1.8 (for a load in the range of 5 pF to 12 pF) | kΩ |
| | | | Fast mode | | 4.0 (for a load in the range of 5 pF to 15 pF) | |
| | LB[1:0] = 01 | High-speed mode | | 1.0 (for a load in the range of 12 pF to 25 pF) | | |
| | | Fast mode | | 2.1 (for a load in the range of 15 pF to 50 pF) | | |
| | LB[1:0] = 10 | High-speed mode | | 0.525 (for a load in the range of 25 pF to 50 pF) | | |
| | | Fast mode | | 0.840 (for a load in the range of 50 pF to 150 pF) | | |
| | LB[1:0] = 11 | High-speed mode | | 0.300 (for a load in the range of 50 pF to 80 pF) | | |
| | | Fast mode | | NA | | |

7.4.2.10 UART Interface PCB Guidelines

The OMAP5432 processor provides 4 UART interfaces.

7.4.2.10.1 UART Interface PCB Requirements

The PCB requirements that must be met for the routing of the UART signals are:

- Far-end load is less than 5 pF
- Maximum trace length = 10 cm
- The trace impedance must be between 30 Ω and 65 Ω
- Output buffer settings:
 - SR[1:0] = 0b00
 - DS[1:0] = 0b01

7.4.2.11 PWM Timer Interface PCB Guidelines

Device processor provides six PWM outputs. These outputs can have their duty cycle controlled by software to provide controls such as display backlight control or keypad backlight control.

The PCB requirements that must be met for the routing of the PWM timer signals are:

- The trace impedance must be between 35 Ω and 65 Ω
- Maximum trace length = 10 cm

7.4.2.12 KeyPad Interface PCB Guidelines

The Device processor provides a 9x9 keypad controller multiplexed twice in the device.

The PCB requirements that must be met for the routing of the KeyPad row and column signals are:

- The trace impedance must be between 30 Ω and 65 Ω
- Maximum trace length = 20 cm

7.4.2.13 Debug Interface PCB Guidelines

7.4.2.13.1 MPU Traces (PTM) and System Traces (STM) Through DRM Interface

MPU and system traces can be exported to an external trace receiver through the DRM interface.

Table 7-32 describes the DRM interface PCB requirements.

Table 7-32. DRM Interface PCB Requirements and IO Programming

| DRM APPLICATION | RE-DRIVER AT MIPI60 JTAG CONNECTOR LEVEL ⁽³⁾ | FAR-END LOAD (pF) | | TRACE LENGTH (cm) | | CHARACTERISTIC IMPEDANCE (Ω) | | IO REGISTER CONFIGURATION | |
|---|---|-------------------|-------------------|-------------------|-----|------------------------------|-------------------|----------------------------|----------------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | SLEW RATE REGISTER SC[1:0] | IMPEDANCE REGISTER DS[1:0] |
| PTM (ARM trace over TPIU)—180-MHz DDR, 16-data-bit mode ⁽¹⁾ , with Lauterbach LA-7992 | Yes | 5 ⁽⁴⁾ | 10 ⁽³⁾ | 10 | 20 | 40 | 51 ⁽⁵⁾ | 0b11 | 0b10 |
| PTM (ARM trace over TPIU)—180-MHz DDR, 16-data-bit mode ⁽¹⁾ , with XDS60v2_pro | No | 2 | 5 | 10 | 20 | 40 | 51 ⁽⁵⁾ | 0b11 | 0b10 |
| STMv2 (System Trace)—180-MHz DDR mode, 4-data-bit mode ⁽²⁾ , with Lauterbach LA-7992 or XDS560v2 | Yes | 5 ⁽⁴⁾ | 10 ⁽³⁾ | 10 | 20 | 40 | 51 ⁽⁵⁾ | 0b11 | 0b10 |
| STMv1 (System Trace)—80-MHz DDR mode, 4-data-bit mode ⁽²⁾ , with XDS560v2 | Yes | 5 ⁽⁴⁾ | 10 ⁽³⁾ | 10 | 20 | 40 | 51 ⁽⁵⁾ | 0b11 | 0b10 |

- (1) Only the 16-data-bit mode is supported (data = drm_emu[4:19], ctrl = drm_emu3, and clock = drm_emu2). The 18-data-bit mode muxing signals from core domain (drm_emu[2:19]) and wake-up domain (drm_emu[0:1]) are not supported at this frequency.
- (2) Only 4-data-bit mode using the pin signals located in the wake-up domain (data = drm_emu[0;1;4;5], ctrl = drm_emu3, and clock = drm_emu2) is supported. Muxing of wake-up domain emu[0:1] with core domain RFBI signals is not supported.
- (3) Level shifter can be implemented on the Device board close to the MIPI60 JTAG connector or plugged in the MIPI 60JTAG connector.
- (4) Far-end load values correspond to the input capacitance of the re-driver requested to support the application.
- (5) For PCB trace lengths shorter than the maximum recommendation, the maximum trace impedance value can be extended to 55 Ω. In that case, a fine-tuned electrical study has to be performed to limit the signal integrity issue.

7.4.2.13.2 System (STM) and JTAG Traces Through SD Card Interface

System trace can be exported to the external trace receiver through the SD card interface (SD card slot).

The NIDnT PCB requirements and IO settings are those described for the SD card interface, see Section 7.4.2.3.1, *Single-Ended Interfaces—SD Card PCB Guidelines*.

7.5 Differential Interfaces

7.5.1 General Routing Guidelines

The following general routing guidelines describe the routing guidelines for differential lanes and differential signals.

Specific guidelines by the OMAP5 interface are outlined in that chapter.

- As much as possible, no other high frequency signals must be routed in close proximity to the differential pair.
- Differential traces must be routed on the same layer. For each signal of the pair, the trace width and spacing must be chosen to yield the differential impedance value recommended.
- Minimize external components on differential lanes (like external ESD, probe points).
- Through-hole pins are not recommended.
- Differential lanes must not cross image planes (ground planes).
- No sharp bend on differential lanes.
- Number of vias on the differential pairs must be minimized, and identical on each line of the differential pair. In case of multiple differential lanes in the same interface, all lines must have the same number of vias.
- Shielded routing is to be promoted as much as possible (for instance, signals must be routed on internal layers that are inside power and/or ground planes).

7.5.2 MIPI D-PHY PCB Guidelines

The MIPI D-PHY signals include the CSIPORTA, CSIPORTB, CSIPORTC, DSIPORTA, and DSIPORTC interfaces to or from the OMAP5430 device.

For more information regarding the MIPI-PHY signals and corresponding balls, see , *Signal Descriptions*.

For more information, you can also see the MIPI D-PHY specification v1-01-00_r0-03 (specifically the Interconnect and Lane Configuration and Annex B Interconnect Design Guidelines chapters).

In the next section, the PCB guidelines of the following five differential interfaces are presented:

- CSIPORTA, CSIPORTB, and CSIPORTC MIPI CSI-2 at 1.5 Gbps
- DSIPORTA and DSIPORTC MIPI DSI-1 at 1.255 Gbps

7.5.2.1 CSIPORTA, CSIPORTB, and CSIPORTC MIPI CSI-2 (1.5 Gbps), and DSIPORTA and DSIPORTC MIPI DSI-1 (1.255 Gbps)

7.5.2.1.1 General Guidelines

The general guidelines for the PCB differential lines are:

- Differential trace impedance $Z_0 = 100 \Omega$ (minimum = 85Ω , maximum = 115Ω)
- Total conductor length from the OMAP5 package pins to the peripheral device package pins is 25 to 30 cm with common FR4 PCB and flex materials.

NOTE

Longer interconnect length can be supported at the expense of detailed simulations of the complete link including driver and receiver models.

The general rule of thumb for the space $S = 2 \times W$ is not designated (see [Figure 7-30, Guard Illustration](#)). It is because although the $S = 2 \times W$ rule is a good rule of thumb, it is not always the best solution. The electrical performance will be checked with the frequency-domain specification. Even though the designer does not follow the $S = 2 \times W$ rule, the differential lines are ok if the lines satisfy the frequency-domain specification.

Because the MIPI signals are used for low-power single-ended signaling in addition to their high-speed differential implementation, the pairs must be loosely coupled.

7.5.2.1.2 Length Mismatch Guidelines

7.5.2.1.2.1 CSIPORTA, CSIPORTB, and CSIPORTC MIPI CSI-2 (1.5 Gbps)

The guidelines of the length mismatch for CSI-2 are presented in [Table 7-33](#).

Table 7-33. Length Mismatch Guidelines for CSI-2 (1.5 Gbps)

| PARAMETER | TYPICAL VALUE | UNIT |
|--------------------------|---|------|
| Operating speed | 1500 | Mbps |
| UI (bit time) | 667 | ps |
| Intralane skew | Have to satisfy mode-conversion S parameters ⁽¹⁾ | |
| Interlane skew (UI / 50) | 13.34 | ps |

(1) sdc12, scd21, scd12, sdc21, scd11, sdc11, scd22, and sdc22

7.5.2.1.2.2 DSIPORTA and DSIPORTC MIPI DSI-1 (1.255 Gbps)

The guidelines of the length mismatch for DSI-1 are presented in [Table 7-34](#).

Table 7-34. Length Mismatch Guidelines for DSI-1 (1.255 Gbps)

| PARAMETER | TYPICAL VALUE | UNIT |
|---------------------------|---------------|------|
| Operating speed | 1255.5 | Mbps |
| UI (bit time) | 797 | ps |
| Intralane skew (UI / 150) | 5.31 | ps |
| Interlane skew (UI / 50) | 15.93 | ps |

7.5.2.1.3 Frequency-domain Specification Guidelines

After the PCB design is finished, the S-parameters of the PCB differential lines will be extracted with a 3D Maxwell Equation Solver such as the high-frequency structure simulator (HFSS) or equivalent, and compared to the frequency-domain specification as defined in the section 7 of the MIPI Alliance Specification for D-PHY Version v1-01-00_r0-03.

If the PCB lines satisfy the frequency-domain specification, the design is finished. Otherwise, the design needs to be improved.

7.5.3 USB PHY PCB Guidelines

7.5.3.1 USB High-Speed PHY Interface (480 Mbps)

The USB_{D0_HS} PHY signals are the positive and negative (DP and DM) signals from the USB transceiver contained within the device.

7.5.3.1.1 General Guidelines and Length Mismatch Guidelines

7.5.3.1.1.1 USB High-Speed (HS) PCB Requirements

- DP and DM lines must have $Z_0 = 90 \Omega$ differential trace impedance (minimum = 80 Ω , maximum = 100 Ω).
- Intralane delay mismatch between DP and DM is less than 5 ps.
- DP and DM trace lengths between the OMAP5 package pins and the USB HS connector < 30 cm (including ESD and CMF)
- Distance between the common mode choke (CMF) and the ESD protection device (TVS) must be as short as possible.
- Distance between the ESD protection device (TVS) and the connector must be as short as possible.
- USB standard connector must be used (micro-AB or mini-AB).
- USB grounds must be shorted to the board ground plane with minimum routing (only a via must be connected to the ground plane to avoid loop creation and so to reduce EMI).

7.5.3.1.1.2 USB High-Speed (HS) Implementation Proposal

[Figure 7-33](#) proposes an example of USB high-speed (HS) PHY implementation with a PMIC and a TPD4S012 component.

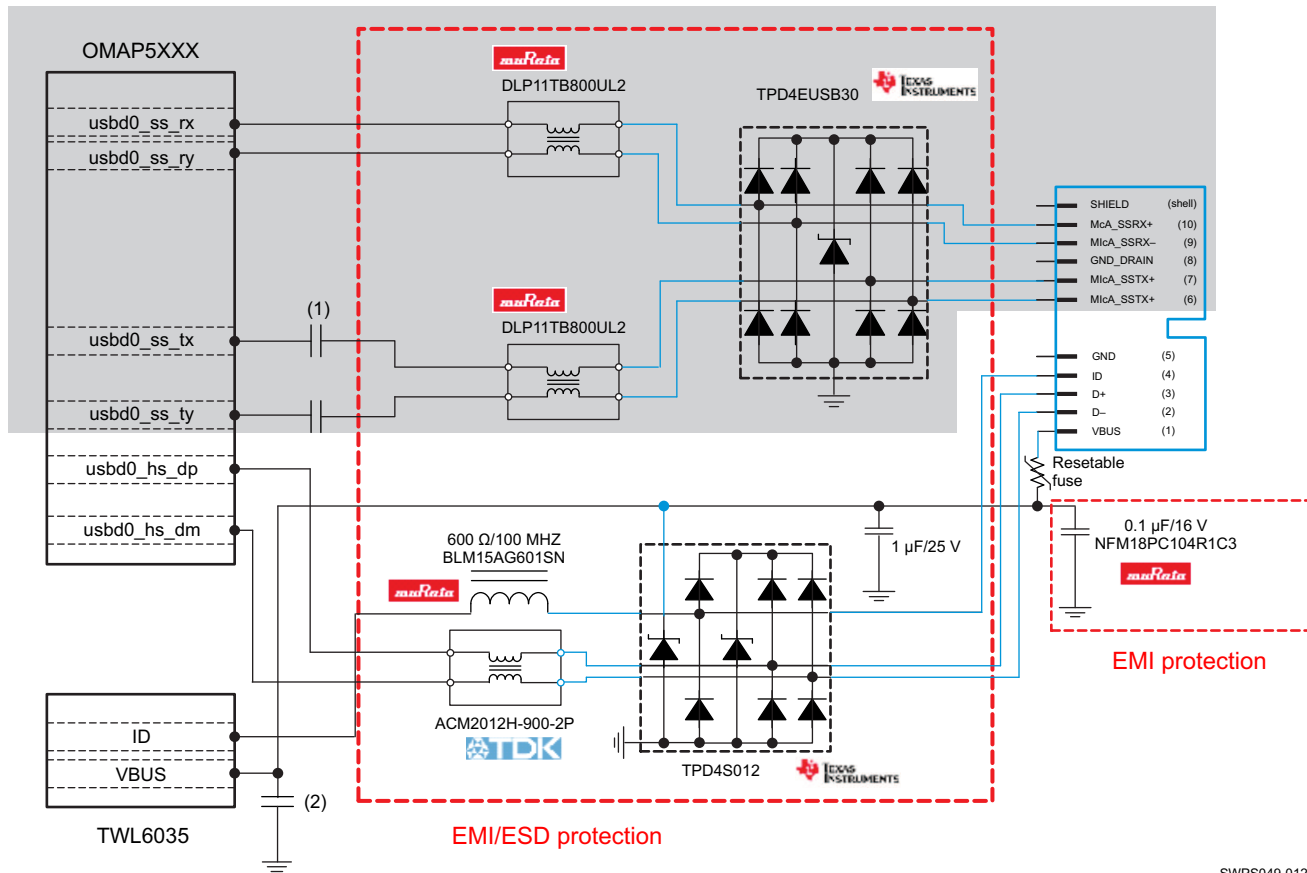


Figure 7-33. USB HS Implementation Proposal (ESD/EMI Protection)

SWPS049-012

- (1) For capacitor value, please refer to the USB3 standard specification.
- (2) For capacitor value, please refer to the TWL6035 TRM.

NOTE

System level ESD results (following IEC 61000-4-2 standard) are dependent on the components being connected to the product.

Part numbers that are different from the reference board specification described in [Table 7-35, USB HS PHY Component References](#), are not assured to meet system level ESD requirements.

For more information on USB HS PHY ESD recommendation see [Section 7.5.3.1.1.3, USB High-Speed \(HS\) ESD Implementation](#).

Table 7-35. USB HS PHY Component References

| INTERFACE | DEVICE | SUPPLIER | PART NUMBER |
|------------|--------|----------|--|
| USB HS PHY | TVS | TI | TPD4S012DRY |
| | CMF | TDK | ACM2012H-900-2P |
| | CFB | Murata | [600R / 100M / 0402] BLM15AG601SN1 |
| | C | Murata | [1 μ F / 25 V / 0603] GRM188R71E105KA12D |
| | EMICAP | Murata | [0.1 μ F / 16 V] NFM18PC104R1C3 |

7.5.3.1.1.3 USB High-Speed (HS) ESD Implementation

NOTE

For more information on system ESD or EMI/EMC, see [Section 7.2.5, System ESD Generic Guidelines](#) and [Section 7.2.6, EMI / EMC Issues Prevention](#).

ESD: USB HS has the following pins to protect: DP and DM attached to the OMAP5430 device, and ID and VBUS pins attached to the PMIC device.

For DP and DM pins:

- ESD protection device must be preferably an array with a low capacitance (= 1.0 pF typical) and a low turn-on resistance ($R_{dyn} = 1.2 \Omega$) while the VBUS pin is designed to tolerate 20 V.
- Common mode choke filter (CMF) must be placed between the ESD protection and the OMAP5430 device to minimize electromagnetic interference (EMI).
- DC series resistance of the CMF needs to be 3 Ω maximum.

For VBUS and ID pins:

- For the VBUS pin, a broadband decoupling capacitor reduces noise in the VBUS power line. In addition, a large decoupling capacitor will absorb the ESD pulse energy.
- For the ID pin, a chip ferrite bead placed between the ESD protection and the PMIC is recommended.

NOTE

System level ESD results (following IEC 61000-4-2 standard) are dependent on the components being connected to the product.

Part numbers that are different from the reference board specification described in [Table 7-35, USB HS PHY Component References](#), are not assured to meet system level ESD requirements.

7.5.3.1.2 Interconnect Simulation

After the PCB design is finished, the S-parameters of the PCB differential lines will be extracted with a 3D Maxwell Equation Solver such as the high-frequency structure simulator (HFSS) and run simulations to check that the link meets the USB HS performances at the USB2 conformance test points:

- TP2 when simulating the USB2 driver
- TP1 when simulating the USB2 receiver

If the performances are met, the design is finished. Otherwise, the design needs to be improved.

7.5.3.2 USB 3.0 Board Design and Layout Guidelines

This section provides the timing specification for the USB3.0 (USB1 in the device) interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. TI has performed the simulation and system design work to ensure the USB3.0 interface requirements are met. The design rules stated within this document are targeted at DEVICE mode electrical compliance. HOST mode and/or systems that do not include the 3m USB cable and far-end 11-inch PCB trace required by DEVICE mode compliance testing may not need the complete list of optimizations shown in this document; however, applying these optimizations to HOST mode systems will lead to optimal DEVICE mode performance.

7.5.3.2.1 USB 3.0 interface introduction

The USB 3.0 has two unidirectional differential pairs: TXp/TXn pair and RXp/RXn pair. AC coupling caps are needed on the board for TX traces.

[Figure 7-34](#) present high level schematic diagram for USB 3.0 interface.

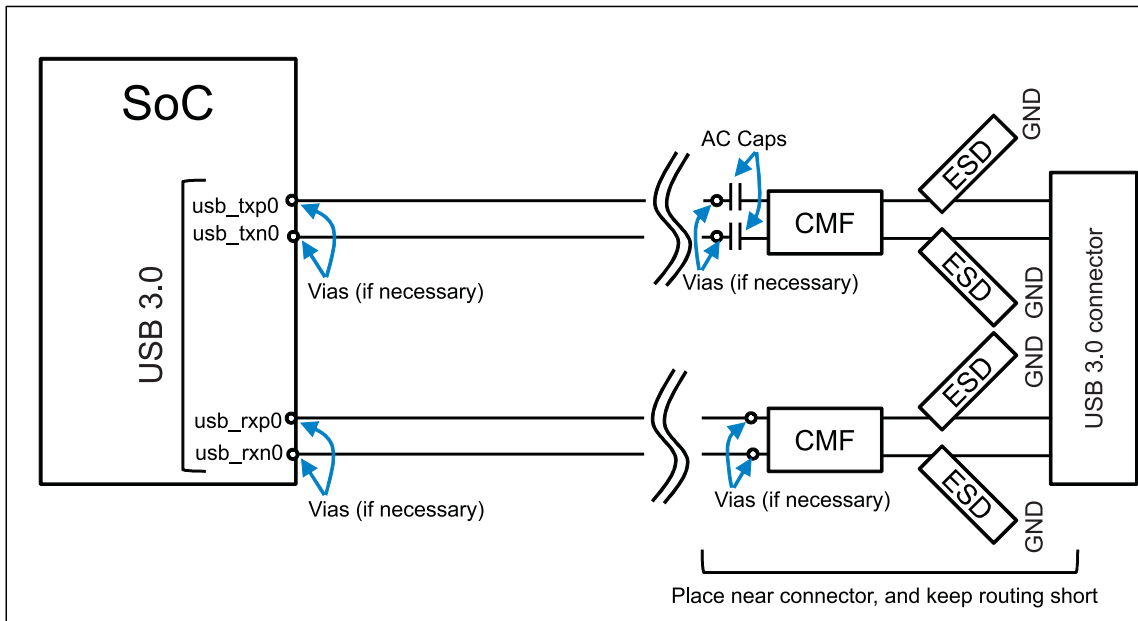


Figure 7-34. USB 3.0 Interface High Level Schematic

NOTE

ESD components should be on a PCB layer next to a system GND plane layer so the inductance of the via to GND will be minimal.

If vias are used, place the vias near the AC Caps or CMFs and under the SoC BGA, if necessary.

Figure 7-35 present placement diagram for USB 3.0 interface.

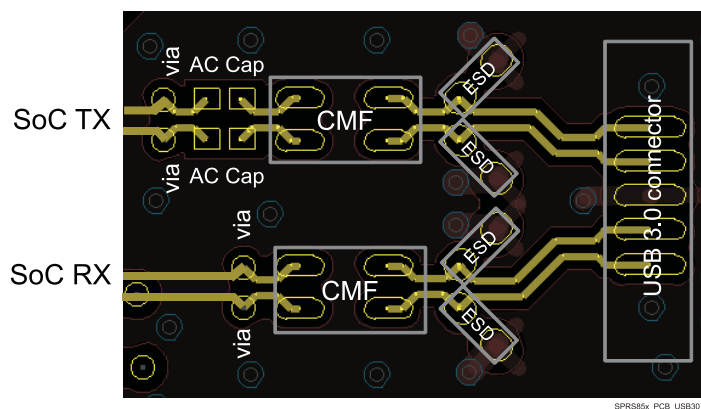


Figure 7-35. USB 3.0 placement diagram

Table 7-36. USB1 Component Reference

| INTERFACE | COMPONENT | SUPPLIER | PART NUMBER |
|-----------|-----------|----------|----------------------------|
| USB3 PHY | ESD | TI | TPD1E05U06 |
| | CMF | Murata | DLW21SN900HQ2 |
| | C | - | 100nF (typical size: 0201) |

7.5.3.2.2 USB 3.0 General routing rules

Some general routing guidelines regarding USB 3.0:

- Avoid crossing splits reference plane(s).
- Shorter trace length is preferred.
- Minimize the via usage and layer transition
- Keep large spacing between TX and RX pairs.
- Intra-lane delay mismatch between DP and DM less than 1ps. Same for RXp and RXn.
- Distance between common mode filter (CMF) and ESD protection device should be as short as possible
- Distance between ESD protection device and USB connector should be as short as possible.
- Distance between AC capacitors (TX only) and CMF should be as short as possible.
- USB 3.0 signals should always be routed over an adjacent ground plane.

Table 7-37 and Table 7-38 present routing specification and recommendations for USB1 in the device.

Table 7-37. USB1 Routing Specifications

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|------|------|------|----------|
| Device balls to USB 3.0 connector trace length | | | 3000 | Mils |
| Skew within a differential pair | | 3 | 6 | Mils |
| Number of stubs allowed on TX/RX traces | | | 0 | Stubs |
| TX/RX pair differential impedance | 83.7 | 90 | 96.3 | Ω |
| Number of vias on each TX/RX trace ⁽¹⁾ | | | 2 | Vias |
| Differential pair to any other trace spacing ⁽²⁾ ⁽³⁾ ⁽⁴⁾ | 2xDS | 3xDS | | |
| Number of ground plane cuts allowed within USB3 routing region (except for specific ground carving as explained in this document) | | | 0 | Cuts |
| Number of layers between USB3.0 routing region and reference ground plane | | | 0 | Layers |
| PCB trace width | | 6 | | Mils |
| PCB BGA escape via pad size | | 18 | | Mils |
| PCB BGA escape via hole size | | 10 | | Mils |

(1) Vias must be used in pairs and spaced equally along a signal path.

(2) DS = differential spacing of the traces.

(3) Exceptions may be necessary in the SoC package BGA area.

(4) GND guard-bands on the same layer may be closer, but should not be allowed to affect the impedance of the differential pair routing. GND guard-bands to isolate USB3.0 differential pairs from all other signals are recommended.

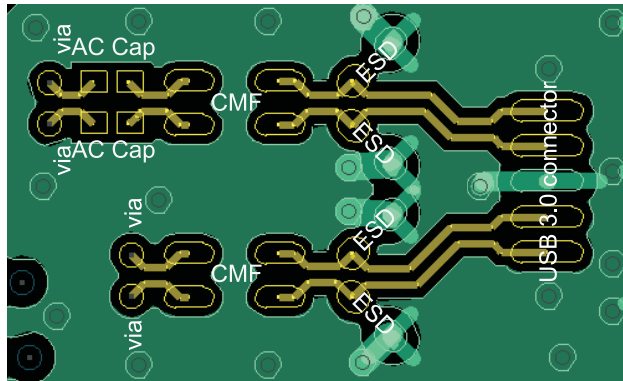
Table 7-38. USB1 Routing Recommendations

| Item | Description | Reason |
|-----------------|--|--|
| ESD location | Place ESD component on same layer as connector (no via or stub to ESD component) | Eliminate reflection loss from via & stub to ESD |
| ESD part number | TPD1E05U06 | Minimize capacitance (0.42pF) |
| CMF part number | DLW21SN900HQ2 | Manufacturer's recommended device |
| Connector | Use USB3.0 connector with supporting s-parameter model | Enable full signal chain simulation |
| Carve Ground | Carve GND underneath AC Caps, ESD, CMF, and connector | Minimize capacitance under ESD and CMF |
| Round pads | Minimize pad size and round the corners of the pads for the ESD and CMF components | Minimize capacitance |

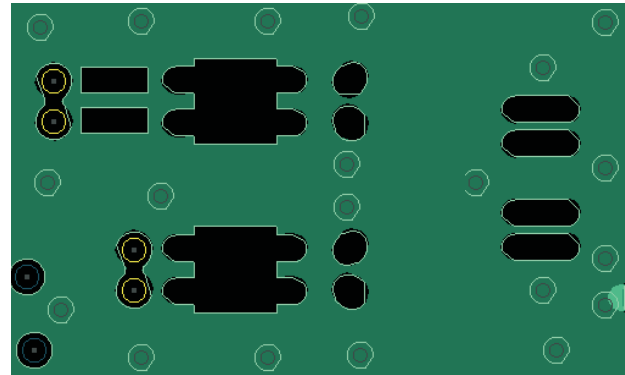
Table 7-38. USB1 Routing Recommendations (continued)

| Item | Description | Reason |
|------|---|---|
| Vias | Max 2 vias per signal trace. If vias are required, place vias close to the AC Caps and CMFs. Vias under the SoC grid array may be used if necessary to route signals away from BGA pattern. | Vias significantly degrade signal integrity at 2.5GHz |

Figure 7-36 presents an example layout, demonstrating the “carve GND” concept.



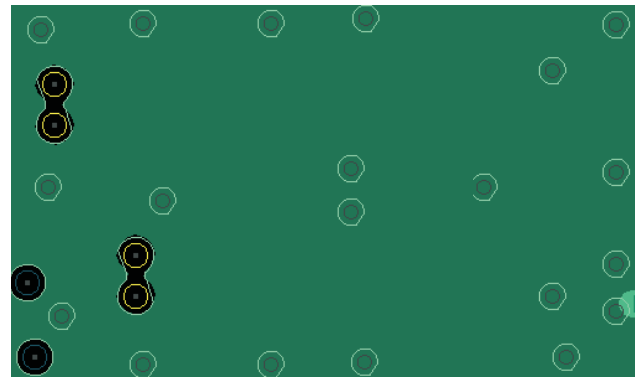
Top Layer: Routing from SoC through AC Caps, CMF, and ESD to connector.



Layer2, GND: Gaps carved in GND underneath AC Caps, CMF, ESD, and connector.



Layer3, Signal: Implement as keep-out zone underneath carved GND areas.



Layer4, GND Plane underneath AC Caps, CMF, ESD, and connector.

SPRS85x_PCB_USB30_3

Figure 7-36. USB 3.0 Example “carve GND” layout

7.5.4 HDMI Board Design and Layout Guidelines

This section provides the timing specification for the HDMI interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. TI has performed the simulation and system design work to ensure the HDMI interface requirements are met. The design rules stated within this document are targeted at resolutions less than or equal to 1080p60 with 8-bit color; deep color (10-bit) requires further signal integrity optimization.

7.5.4.1 HDMI Interface Schematic

The HDMI bus is separated into three main sections (HDMI Ethernet and the optional Audio Return Channel are not specifically supported by this Device):

1. Transition Minimized Differential Signaling (TMDS) high speed digital video interface

2. Display Data Channel (I2C bus for configuration and status exchange between two devices)
3. Consumer Electronics Control (optional) for remote control of connected devices.

The DDC and CEC are low speed interfaces, so nothing special is required for PCB layout of these signals.

The TMDS channels are high speed differential pairs and therefore require the most care in layout. Specifications for TMDS layout are below.

Figure 7-37 shows the HDMI interface schematic.

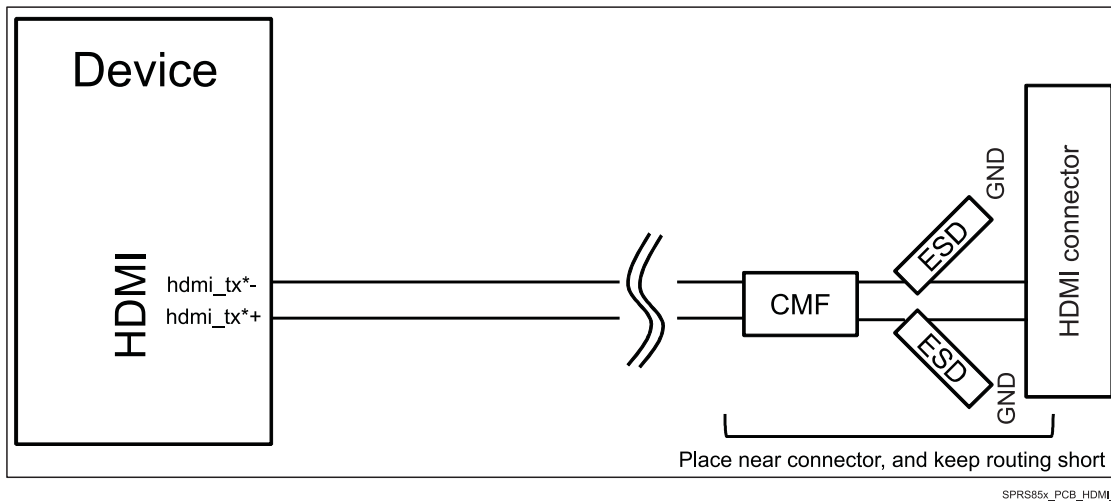


Figure 7-37. HDMI Interface High Level Schematic

Figure 7-38 presents placement diagram for HDMI interface.

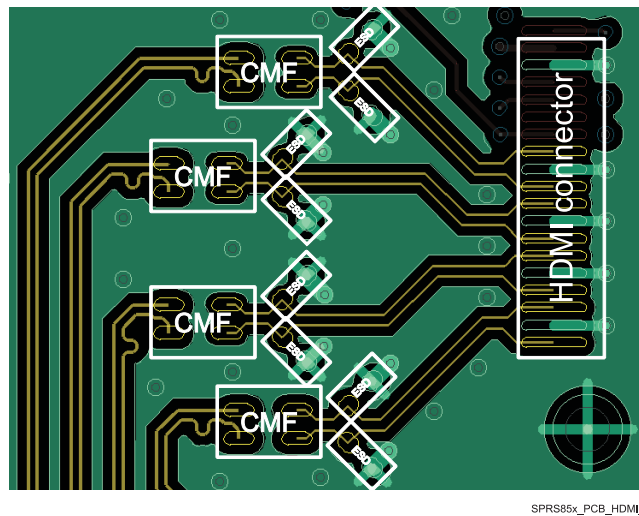


Figure 7-38. HDMI Placement Diagram

Table 7-39. HDMI Component Reference

| INTERFACE | DEVICE | SUPPLIER | PART NUMBER |
|-----------|--------|----------|---------------|
| HDMI | ESD | TI | TPD1E05U06 |
| | CMF | Murata | DLW21SN900HQ2 |

7.5.4.2 TMD5 General Routing Guidelines

The TMD5 signals are high speed differential pairs. Care must be taken in the PCB layout of these signals to ensure good signal integrity.

The TMD5 differential signal traces must be routed to achieve 100 Ohms (+/- 10%) differential impedance and 60 ohms (+/-10%) single ended impedance. Single ended impedance control is required because differential signals can't be closely coupled on PCBs and therefore single ended impedance becomes important.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 60 ohms impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier, and trace width variations don't affect impedance as much, therefore it's easier to maintain accurate impedance over the length of the signal. The wider traces also show reduced skin effect and therefore often result in better signal integrity.

Some general routing guidelines regarding TMD5:

- Avoid crossing splits reference plane(s).
- Shorter trace length is preferred.
- Distance between common mode filter (CMF) and ESD protection device should be as short as possible
- Distance between ESD protection device and HDMI connector should be as short as possible.

Table 7-40 shows the routing specifications for the TMD5 signals.

Table 7-40. TMD5 Routing Specifications

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|------|------|------|--------|
| Device balls to HDMI header trace length | | | 4000 | Mils |
| Skew within a differential pair | | 3 | 5 | Mils |
| Number of stubs allowed on TMD5 traces | | | 0 | stubs |
| TMD5 pair differential impedance | 90 | 100 | 110 | Ω |
| TMD5 single-ended impedance | 54 | 60 | 66 | Ω |
| Number of vias on each TMD5 trace | | | 0 | Vias |
| TMD5 differential pair to any other trace spacing ⁽¹⁾ ⁽²⁾ ⁽³⁾ | 2xDS | 3xDS | | Mils |
| Number of ground plane cuts allowed within HDMI routing region (except for specific ground carving as explained in this document) | | | 0 | Cuts |
| Number of layers between HDMI routing region and reference ground plane | | | 0 | Layers |
| PCB trace width | | 4.4 | | Mils |

(1) DS = differential spacing of the traces.

(2) Exceptions may be necessary in the SoC package BGA area.

(3) GND guard-bands may be closer, but should not be allowed to affect the impedance of the differential pair routing. GND guard-bands to isolate HDMI differential pairs from all other signals is recommended.

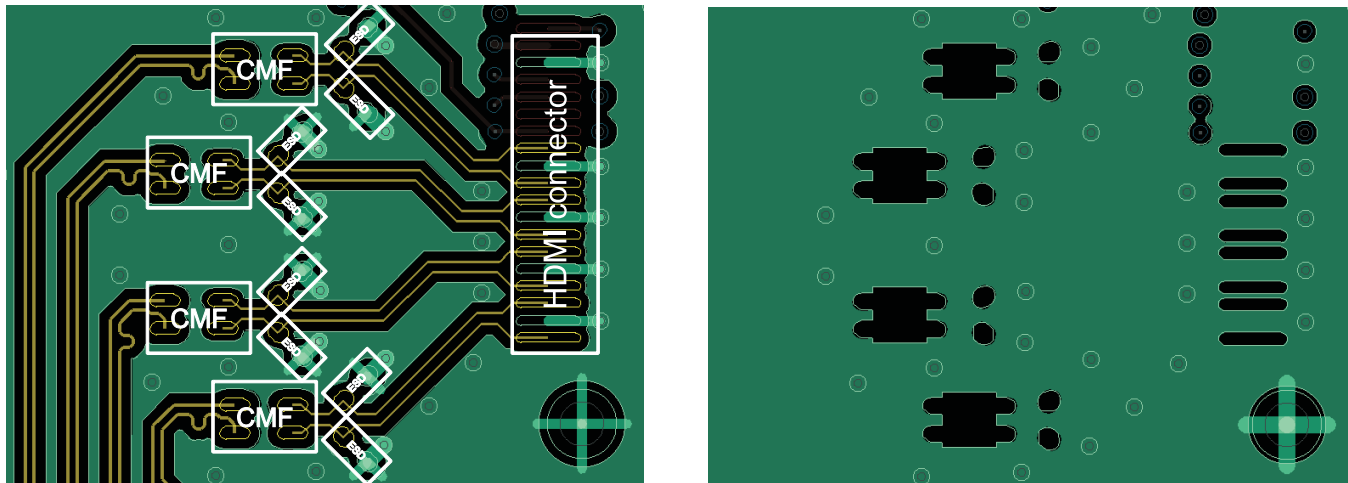
Table 7-41. TDMS Routing Recommendations

| Item | Description | Reason |
|-----------------|-------------|-------------------------------|
| ESD part number | TPD1E05U06 | Minimize capacitance (0.42pF) |

Table 7-41. TDMS Routing Recommendations (continued)

| Item | Description | Reason |
|---------------|--|--|
| Carve Ground | Carve GND underneath ESD and CMF | Minimize capacitance under ESD and CMF |
| Round pads | Reduce pad size and round the corners of the pads for the ESD and CMF components | Minimize capacitance |
| Routing layer | Route all signals only on the same layer as SoC | Minimize reflection loss |

Figure 7-39 presents an example layout, demonstrating the “carve GND” concept.



Top Layer: Routing from SoC through CMF, and ESD to connector.

Layer2, GND: Gaps carved in GND underneath, CMF, ESD, and connector.

SPRS85x_PCB_HDMI_3

Figure 7-39. HDMI Example “carve GND” layout

7.5.4.3 TPD5S115

The TPD5S115 is an integrated HDMI companion chip solution. The device provides a regulated 5 V output (5VOUT) for sourcing the HDMI power line. The TPD5S115 exceeds the IEC61000-4-2 (Level 4) ESD protection level.

7.5.4.4 HDMI ESD Protection Device (Required)

Interfaces that connect to a cable such as HDMI generally require more ESD protection than can be built into the processor’s outputs. Therefore this HDMI interface requires the use of an ESD protection chip to provide adequate ESD.

When selecting an ESD protection chip, choose the lowest capacitance ESD protection available to minimize signal degradation. In no case should be ESD protection circuit capacitance be more than 5pF.

TI manufactures these devices that provide ESD protection for HDMI signals such as the TPDxE05U06. For more information see the www.ti.com website.

7.5.4.5 PCB Stackup Specifications

Table 7-42 shows the stackup and feature sizes required for HDMI.

Table 7-42. HDMI PCB Stackup Specifications

| PARAMETER | MIN | TYP | MAX | UNIT |
|--------------------------|-----|-----|-----|--------|
| PCB Routing/Plane Layers | 4 | 6 | - | Layers |

Table 7-42. HDMI PCB Stackup Specifications (continued)

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|-----|-----|-----|--------|
| Signal Routing Layers | 2 | 3 | - | Layers |
| Number of ground plane cuts allowed within HDMI routing region | - | - | 0 | Cuts |
| Number of layers between HDMI routing region and reference ground plane | - | - | 0 | Layers |
| PCB Trace width | | 4 | | Mils |

7.5.4.6 Grounding

Each TMDS channel has its own shield pin and they should be grounded to provide a return current path for the TMDS signal.

7.5.5 SATA Board Design and Layout Guidelines

The device provides one SATA port. This section provides the timing specification for the SATA interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. TI has performed the simulation and system design work to ensure the SATA interface requirements are met.

7.5.5.1 SATA Interface Schematic

Figure 7-40 shows the data portion of the SATA interface schematic.

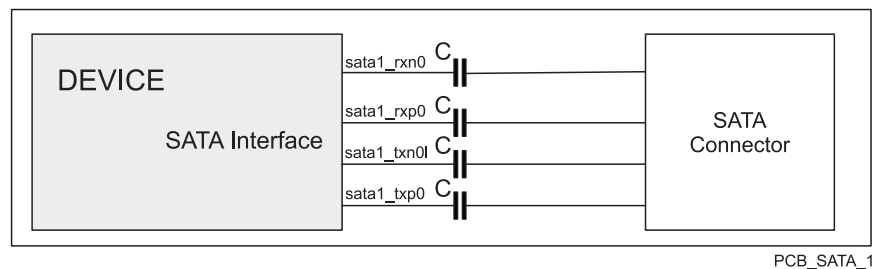


Figure 7-40. SATA Interface High Level Schematic

NOTE

AC coupling capacitors (C) are required on the receive and transmit data pairs. Table 7-43 shows the requirements for these capacitors.

Table 7-43. SATA AC Coupling Capacitors Requirements

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|-----|------|------|-----------|
| SATA AC coupling capacitor value | 0.3 | 10 | 12 | nF |
| SATA AC coupling capacitor package size | | 0402 | 0603 | EIA(1)(2) |

(1) EIA LxW units, i.e., a 0402 is a 40x20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

7.5.5.2 Compatible SATA Components and Modes

Table 7-44 shows the compatible SATA components and supported modes. Note that the only supported configuration is an internal cable from the processor host to the SATA device.

Table 7-44. Compatible SATA Components and Modes

| PARAMETER | MIN | MAX | UNIT | SUPPORTED |
|----------------|-----|-----|------|-----------|
| Transfer Rates | 1.5 | 3 | Gbps | |
| Internal Cable | - | - | - | YES |

7.5.5.3 PCB Stackup Specifications

Table 7-45 shows the stackup and feature sizes required for these types of SATA connections.

Table 7-45. SATA PCB Stackup Specifications

| PARAMETER | MIN | TYP | MAX | UNIT |
|--|-----|-----|-----|--------|
| Number of ground plane cuts allowed within SATA routing region | - | - | 0 | Cuts |
| Number of layers between SATA routing area and reference plane | - | - | 0 | Layers |
| PCB Routing clearance | | 4 | | Mils |
| PCB Trace width | | 4 | | Mils |

7.5.5.4 Routing Specifications

The SATA data signal traces must be routed to achieve 100 Ohms (+/-10%) differential impedance and 60 ohms (+/-10%) single ended impedance. The signal ended impedance is required because differential signals can't be closely coupled on PCBs and therefore single ended impedance becomes important. 60 ohms is chosen for the single ended impedance to minimize problems caused by too low an impedance.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 100 ohms differential and 60 ohms single ended impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

Table 7-46 shows the routing specifications for the SATA data signals.

Table 7-46. SATA Routing Specifications

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---------------------|-----|---------------------|-------|
| SATA signal trace length (device balls to SATA connector) | | | 3000 ⁽¹⁾ | Mils |
| Differential pair trace skew matching | | | 5 | Mils |
| Number of stubs allowed on SATA traces ⁽²⁾ | | | 0 | stubs |
| TX/RX pair differential impedance | 90 | 100 | 110 | Ω |
| TX/RX single-ended impedance | 54 | 60 | 66 | Ω |
| Number of vias on each SATA trace | | | 0 | Vias |
| SATA differential pair to any other trace spacing | 2xDS ⁽³⁾ | | | |

(1) Beyond this, signal integrity may suffer.

(2) Inline pads may be used for probing.

(3) DS = differential spacing of the SATA traces.

Table 7-47. SATA Routing Recommendations

| Item | Description | Reason |
|-----------------|-------------|--|
| ESD part number | None | ESD suppression generally not used on SATA |

7.6 Clock Routing Guidelines

7.6.1 32-kHz Oscillator Routing

When designing the printed-circuit board:

- Keep the crystal as close as possible to the crystal pins X1 and X2.
- Keep the trace lengths short and small to reduce capacitor loading and prevent unwanted noise pickup.
- Place a guard ring around the crystal and tie the ring to ground to help isolate the crystal from unwanted noise pickup.
- Keep all signals out from beneath the crystal and the X1 and X2 pins to prevent noise coupling.
- Finally, an additional local ground plane on an adjacent PCB layer can be added under the crystal to shield it from unwanted pickup from traces on other layers of the board. This plane must be isolated from the regular PCB ground plane and tied to the GND pin of the RTC. The plane must not be any larger than the perimeter of the guard ring. Make sure that this ground plane does not contribute to significant capacitance (a few pF) between the signal line and ground on the connections that run from X1 and X2 to the crystal.

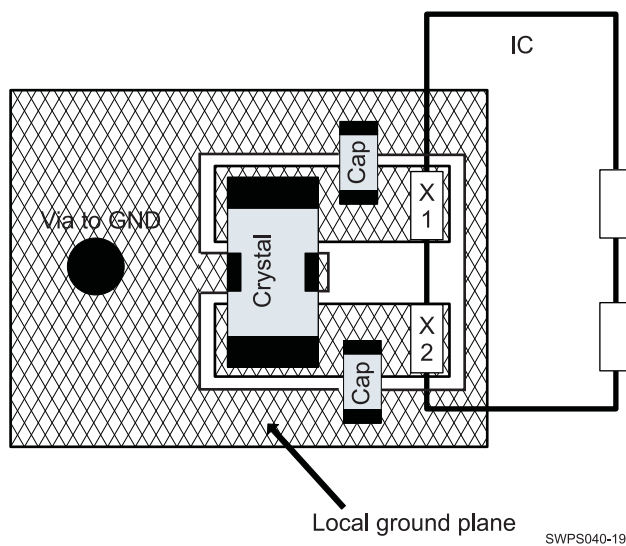


Figure 7-41. Slow Clock PCB Requirements

7.6.2 Oscillator Ground Connection

Although the impedance of a ground plane is low it is, of course, not zero. Therefore, any noise current in the ground plane causes a voltage drop in the ground. [Figure 7-42](#) shows the grounding scheme for slow (low frequency) clock generated from the internal oscillator.

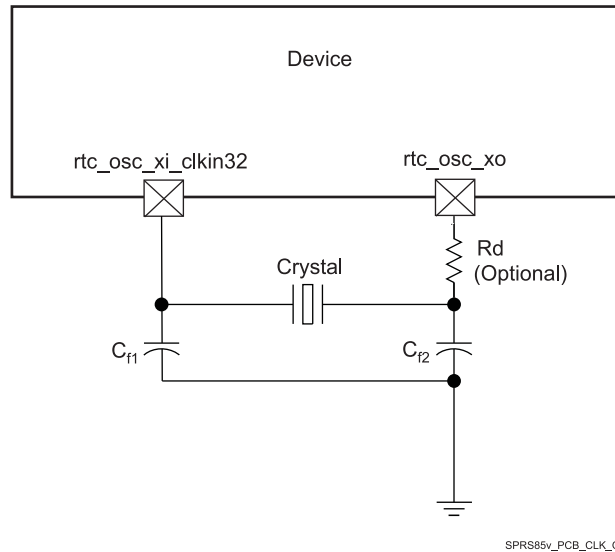
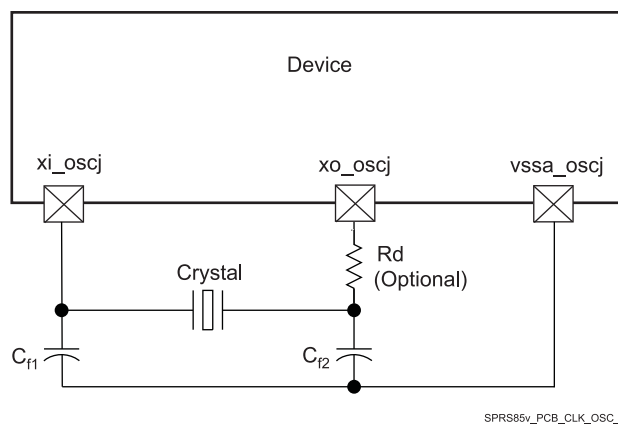


Figure 7-42. Grounding Scheme for Low-Frequency Clock

Figure 7-43 shows the grounding scheme for high-frequency clock.



(1) j in *_osc = 0 or 1

Figure 7-43. Grounding Scheme for High-Frequency Clock

7.7 DDR3 Board Design and Layout Guidelines

7.7.1 Introduction

The OMAP5432 device has two 32-bit-wide DDR3 channels. The device supports both 1.5-V (DDR3) and 1.35-V (DDR3L) voltage operation. Because the bus width is 32 bits, it is not compatible with DDR3 UB DIMM. Primarily, the OMAP5432 device is intended to use the on-board DDR3 memories.

The OMAP5432 pitch and ballout have been defined to enable platform design with HDI and PTH PCB technologies. PTH technology permits minimizing costs associated to the PCB but induces additional routing constraints.

In this section, the principle of the DDR3 memory interface and the PCB design method are described for these two different PCB types (6L PTH and 1-4-1 HDI).

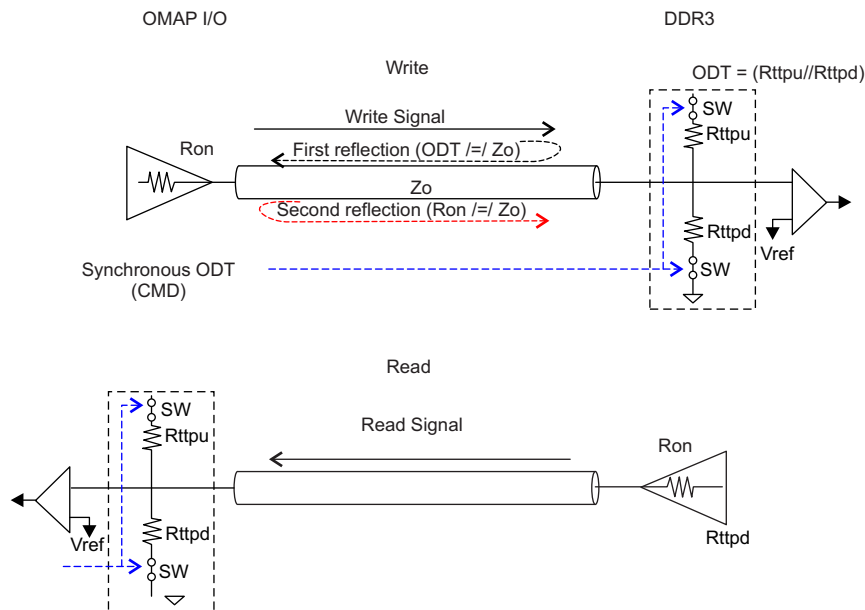
7.7.2 DDR3 Memory Configuration

According to the JEDEC Standard, DDR3 is specified as three different bus types: x4 (78-ball FBGA), x8 (78-ball FBGA), and x16 (96-ball FBGA). Because the OMAP5432 device does not support x4, either x8 or x16 are used. Different from LPDDR2, two or four DDR3 memories are used to build the 32-bit memory bus.

7.7.2.1 DDR3 IO and Termination

For high-speed data transmission, the PCB line impedance must be controlled, and the on-die termination may be applied. Usually a 50-Ω characteristic impedance (Z_0) is used.

As indicated from Figure 7-44, the drive impedance and the termination are programmable. To minimize the reflection, a termination equal to Z_0 may be used. It may be adjusted to a higher value (for example, 60 Ω) to reduce the power consumption.



| | | | |
|-----------------|---|----------------|-----|
| OMAP5432 I/O | Drive strength (R_{on}) in Ω | I[2:0] = 000 | 80 |
| | | I[2:0] = 001 | 60 |
| | | I[2:0] = 010 | 48 |
| | | I[2:0] = 011 | 40 |
| | | I[2:0] = 100 | 34 |
| ODT in Ω | odt[1:0] = 00 | OFF | |
| | odt[1:0] = 01 | 60 | |
| | odt[1:0] = 10 | 80 | |
| | odt[1:0] = 11 | 120 | |
| DDR3 memory | Drive strength (R_{on}) in Ω | bit[1:0] = 00 | 40 |
| | | bit[1:0] = 01 | 34 |
| | ODT in Ω | bit[2:0] = 001 | 60 |
| | | bit[2:0] = 010 | 120 |
| | | bit[2:0] = 011 | 40 |
| | | bit[2:0] = 100 | 20 |
| bit[2:0] = 101 | 30 | | |

$ODT = R_{ttpu} // pd$

SWPS044-009

Figure 7-44. DDR3 Data Transmission Model

7.7.2.2 Source Matching Concept

It is possible to choose the characteristic impedance equal to the drive impedance and to remove the termination. In this case, the signal is reflected at the receiver; however, the reflection signal is absorbed at the driver. It depends on the length and crosstalk of the lines; minor degradation of the signal may be acceptable, but needs to be simulated and validated.

To reduce the crosstalk and to make 34- to 40-Ω impedance, the HDI PCB may be used. Note that the drive impedance changes 15% and the PCB impedance changes 20%. It is important to verify the design at the corner conditions.

7.7.2.3 Termination Power

When ODT is enabled, the power dissipation is increased. With the ODT control signal, termination is enabled only when the data burst occurs. Therefore, the termination power is proportional to the usage of bus. That is, it is proportional to the data rate.

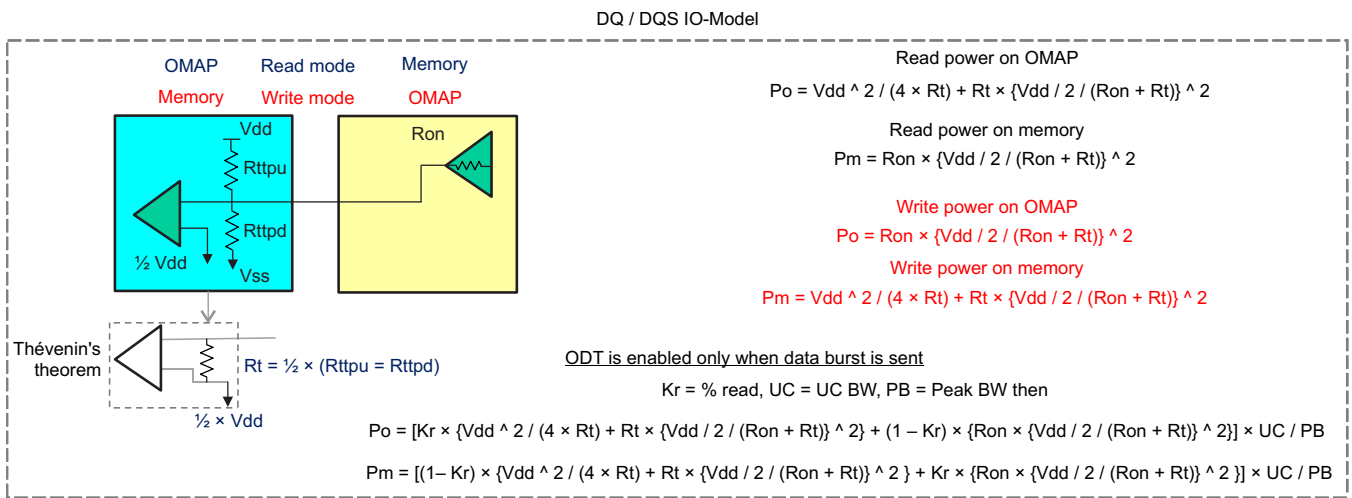


Figure 7-45. Data IO Model

Figure 7-45 shows how termination power is calculated. When OMAP writes to the memory, the termination occurs at the memory side, the direction is reversed by a read. Figure 7-45 shows power consumption per bit and it is necessary to multiply by the number of bits. One data byte consists of 11 data lanes, so the termination power of the entire 8 bytes is 88 times the value.

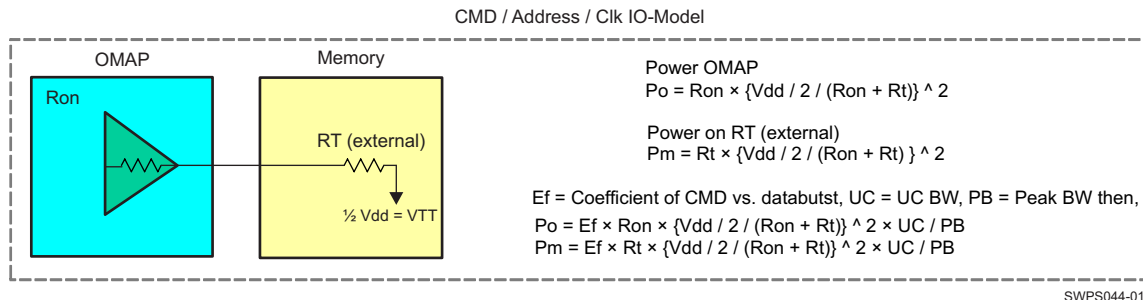


Figure 7-46. Termination Power on the Command-Address Bit

There is no ODT on the command-address (CA) bit. If a fly-by connection is selected, termination resistors are added to the PCB and the VTT (= Vref) regulator is used. If the T-branch connection is used, the CA termination could be eliminated.

7.7.2.4 T-Branch and Fly-by Topologies

Multiple DDR3 memories are connected to construct the 32-bit data bus. The CA signals are common to all memories. It is possible to use the T-branch topology with up to 2 x16 DDR3 memories. The CA termination may be eliminated.

If the x8 DDR3 is used, and more than two memories are connected to a CA bus, then the fly-by topology must be used.

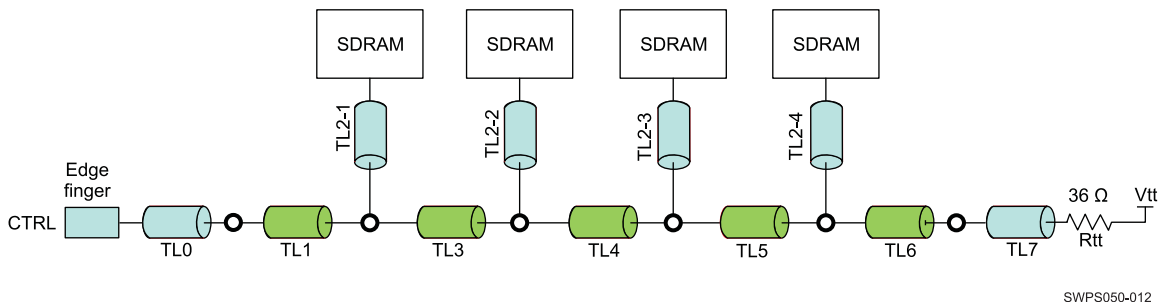


Figure 7-47. Fly-by Topology

With fly-by topology, multiple memories are connected to the single transmission line and the line is terminated at the end. Because each memory is driven by different timing, it is possible to reduce the impact of the capacitive loads.

The OMAP5432 memory controller supports write leveling, therefore we can use the fly-by topology. However, if the x16 device is used, only two memories are connected to the channel. In this case T-branch topology can be used.

The OMAP5432 CA balls are located between the data bytes. The T-branch CA bus can be placed between the two memories.

The OMAP5432 ballout is optimized for x16 DDR3 device so that the data bits are connected straight in one layer.

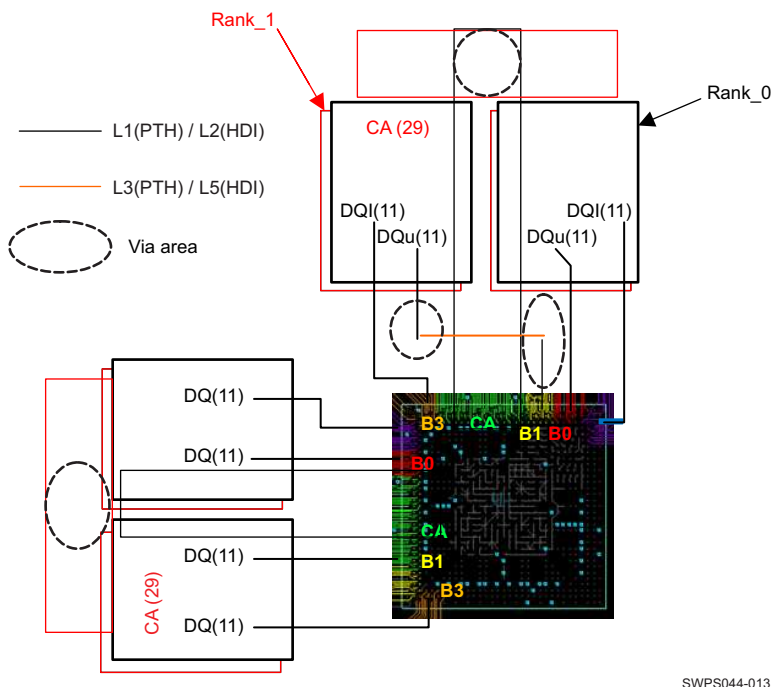


Figure 7-48. Floor Plan for the x16 DDR3 (T-Branch)

Figure 7-49 shows the floor plan for the x8 DDR3 using the fly-by topology. As the CA balls are located between the data bytes, it is necessary to cross the data lines.

Considering the footprint of the memories, the x16 with T-branch topology has been selected for the reference board.

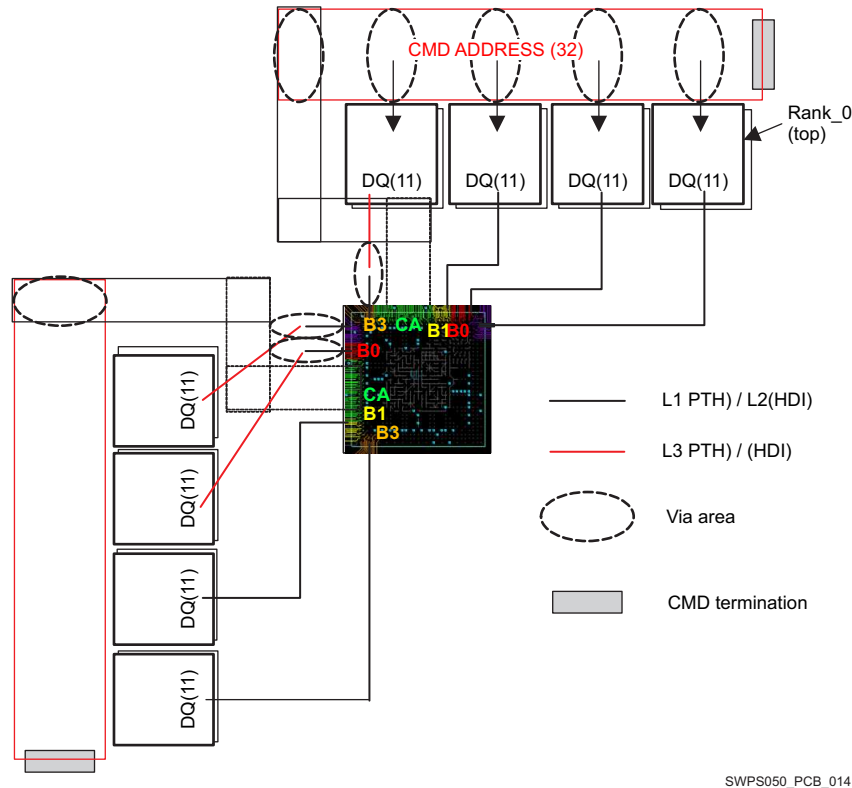


Figure 7-49. Floor Plan for x8 DDR3 (Fly-by Topology)

7.7.3 PCB Stack Up Options

The OMAP5432 ball assignment is optimized for the x16 T-branch connection. The balls in the first row are partially depopulated so that the outer three rows can be routed by the single layer. All DDR3 signals are assigned there.

The balls in rows 4, 5, 6, 7, and 8 are routed through the vias located in the via channel array (VCA). Because of the VCA, we can use a conventional 6L PTH PCB for the OMAP5432 device.

It is also possible to use 1-4-1 HDI PCB. For the HDI PCB, L1 can be the GND plane. The DDR3 signals are routed by the L2 that works as a shielded strip-line. It is possible to attain the lower characteristic impedance and therefore source matching may be applied.

It is also possible to connect the power planes to the core balls through VCA. The power plane is not disconnected by the signal vias.

7.7.3.1 PTH PCB

Figure 7-50 shows the 6L PTH stack up. Via size can be up to 0.25 mm with a 0.45-mm annular ring. To escape 0.5 BGA, trace width and space must be 75/75 μm .

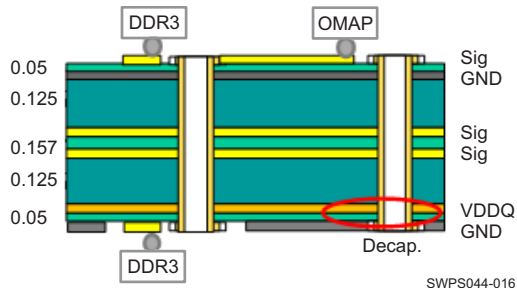


Figure 7-50. 6L PTH Stack up

If needed because of a manufacturing reason, we could use the 75/75 bottleneck and relax the rest of the design to 100/100 (see Figure 7-51).

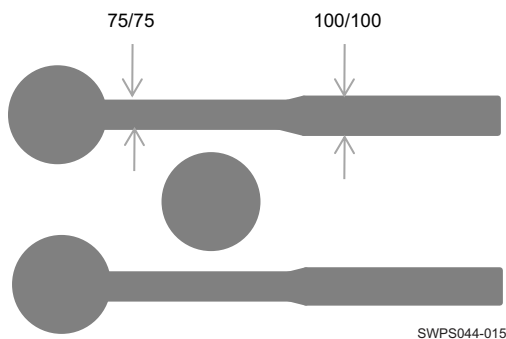


Figure 7-51. 75/75u Bottleneck

The signals are primarily in layer 1. Layer 6 is used for bit mirroring of the bottom side memories. Layer 3 or 6 is used for crossing the signals. Layer 4 is reserved for other signals.

The GND plane and the 75- μ m wide-line form a 51- Ω Microstrip line. Note that the GND plane is the return path of the signals. Therefore, the GND plane must always present under the signal line.

Layer 5 is used by the VDD plane. The line in layer 6 also works as Microstrip line. Except for the area of the L6 signal, it is recommended to cover layer 6 by GND as much as possible.

The L6 GND and the L5 VDD form a distributed decoupling capacitor.

7.7.3.2 1-4-1 HDI PCB

In the HDI PCB stack up, the DDR3 signals are primarily routed on layer 2. It is possible to use layer 4 for data crossing. Layer 3 is the VDD plane. A distributed decoupling capacitor is made between layer 3 and layer 5. Except around the IC, the components, and some critical nets, layer 1 and layer 6 must be the GND planes. It is useful to control EMC, and to reduce the cross-talk.

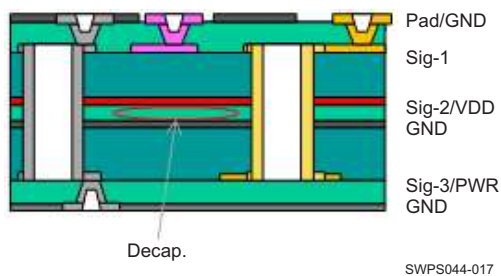


Figure 7-52. 1-4-1 HDI Stack up

7.7.4 PTH PCB Layout

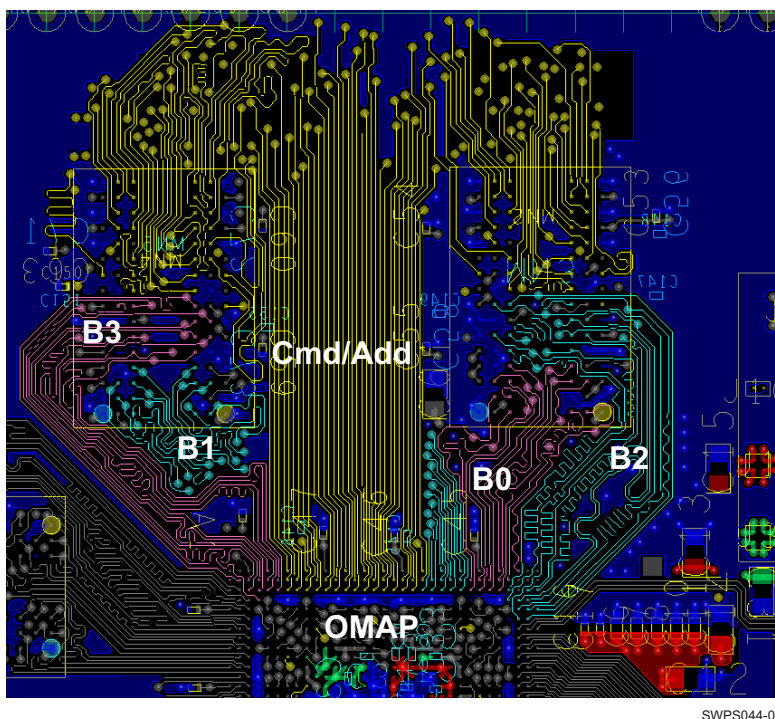
7.7.4.1 Floor Plan

A high-level floor plan based on the x16 DDR3 has been presented in [Figure 7-48](#).

The CA bus is routed between the two DDR3 memories.

4 × 1.5-V decoupling capacitors and a 2x Vref decoupling capacitor must be placed as close as possible to the OMAP device.

The channel 2 floor plan is almost identical, except for the B1 byte. Because the CA is located within the two data bytes, CA and data are connected directly.

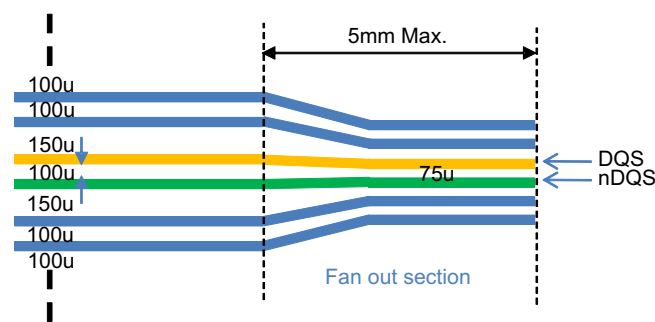
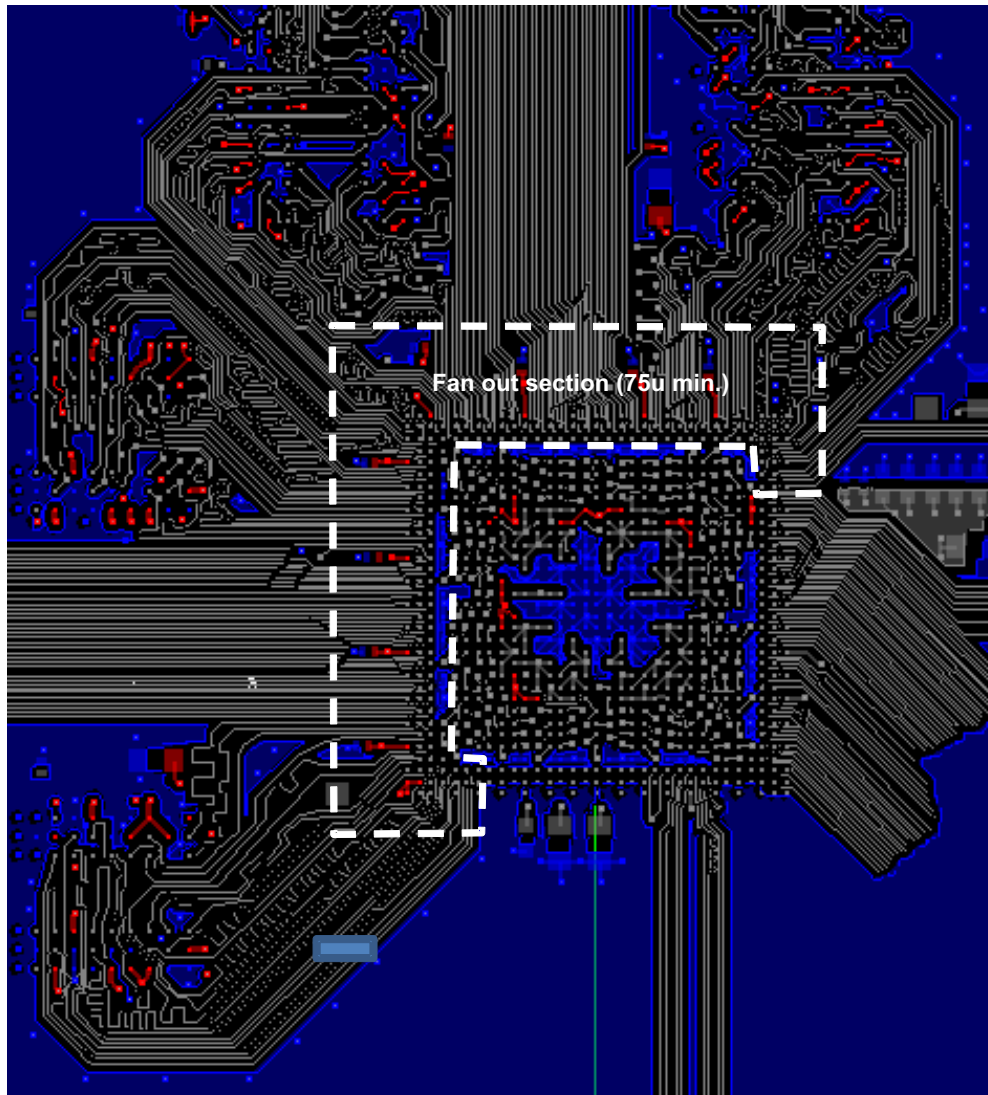


SWPS044-018

Figure 7-53. Channel 1 Test Layout (L1)

7.7.4.2 DQ Signal Routing

Minimum line spacing of 75 μm can be used for BGA escape and in the fan out area, as indicated on [Figure 7-54](#). The total sum line length of 75 μm must be limited within 5 mm. Otherwise, line to line spacing must be greater than 2x the dielectric thickness (data to data) and 3x (data to strobe). In this stack up a 50- μm dielectric thickness is used.



SWPS044-036

Figure 7-54. Line to Line Space (Edge to Edge)

Within the byte the data signal length must be matched within ± 0.5 mm. For routing to the bottom side memories, a PTH via is placed as close as possible to the DDR3 memory and routed to the bottom memories by L6. Signals are mirrored by the L6 traces.

In case the multiple layers are used within the same byte, it must be considered that the signal velocity is different from layer to layer. In this case static skew of data signals must be controlled within ± 10 ps from the strobe (DQS/nDQS).

7.7.4.3 Byte 1 (DQ08-15) Crossing

The channel 1 byte 1 signals need to cross the CA bus, if possible layer 6 should be used. Note that signal velocity of layer 1 and layer 6 is same. If other layers are used, careful skew control is needed. The vias must be located within 5 mm from the nearest decoupling capacitor. This is to connect the layer 5 plane and layer 2 plane to provide return paths. If both layers 2 and 5 are assigned to GND, the decoupling capacitor can be replaced by the vias connecting the both planes. The signal vias must be placed in distance so that the plane is connected in between the vias.

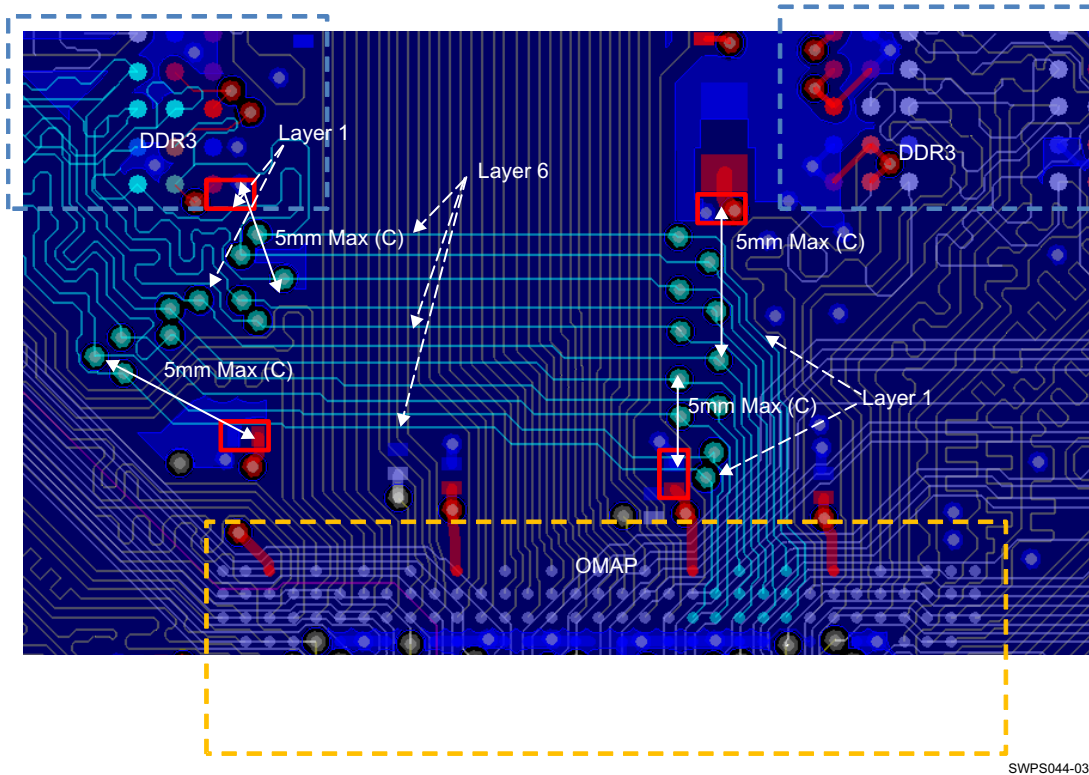


Figure 7-55. Byte 1 Crossing CA Bus

It is also important to secure the return path in the GND plane. As indicated on [Figure 7-56](#) vias must have enough distance, not to make a big hole in the GND plane.

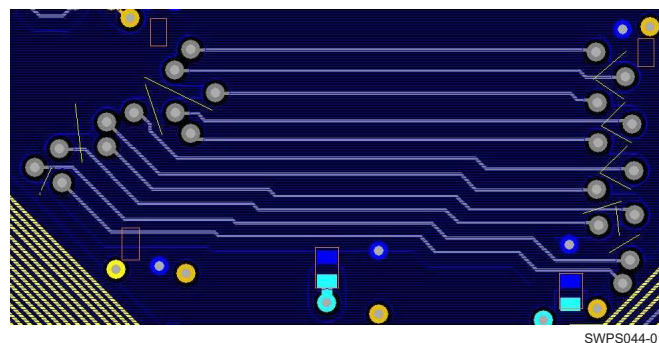


Figure 7-56. Layer2 GND Return Path (Yellow) and Decoupling Capacitors

7.7.4.4 Command Signal Routing

To obtain the best signal integrity, the T-branch CA line must be laid out as shown in Figure 7-57. The left and right arms of large-T (L1 = L2) must be balanced to within ±2 mm. It is ideal that small T (L3 = L4, L5 = L6) are also balanced to within ±2 mm, but it may be difficult.

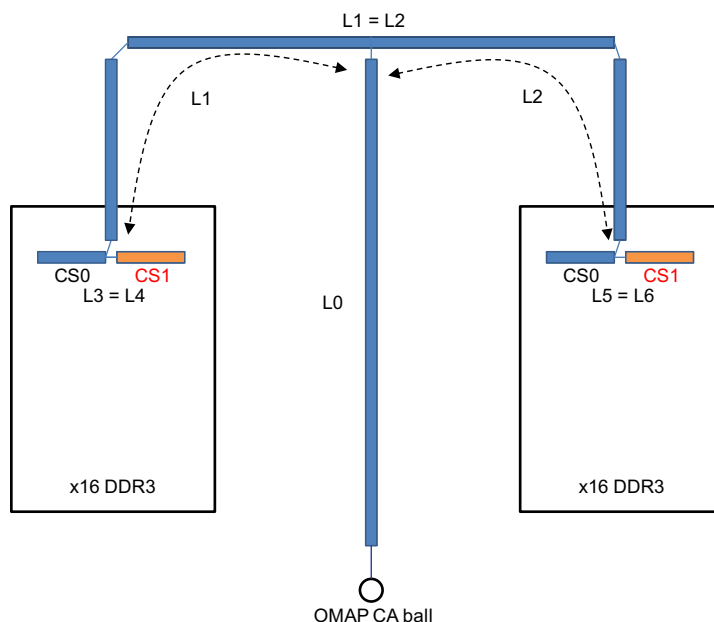
Therefore, small T must be as short as possible. The unbalanced-T causes the signal degradation.

It is possible to route this way by 1-4-1 HDI.

The vias may be placed outside of the memory BGA area, it is important to match the left and right branches to within ±2 mm.

To route the CA bus by the 6L PTH, the small T could be long; therefore, it will be necessary to balance the small T. See Figure 7-58.

For the test layout, layer 1 is used for the blue line, layer 3 for the green, and layer 6 for the orange.



SWPS044-020

Figure 7-57. Goal of CA Layout

Hints for line balancing:

- The trombone loops may be added to balance L1 and L2. For example, if A0 is located at left, L1 needs to be extended. If ODT_0 is located at right, L2 needs to be extended. It is desirable to balance them within a few mm.
- The order of the horizontal bus must align to the order of the DDR3 balls. For example, RAS and CAS must be located next to the memory, A13 and A14 must be far from the memory. Reset must be at the end (reset is asynchronous).
- clk and nclk are close to the middle of the bus.

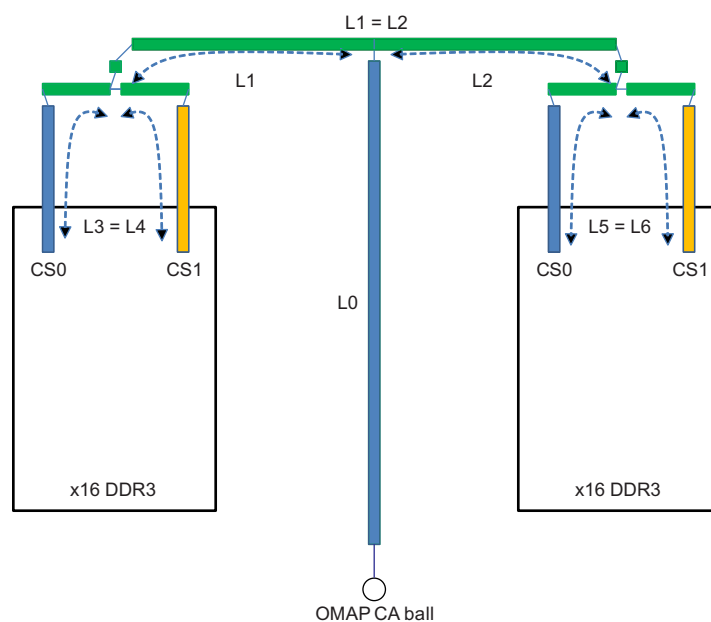


Figure 7-58. CA Topology of 6L PTH

In this way, total line length can be balanced $< \pm 10$ mm, from the clk lines. Static skew around 70 ps is acceptable.

7.7.4.5 Clock to Data Strobe Relationship

The OMAP5432 device supports write and read leveling. For the OMAP controller to work properly, the clock and the data-strobe must meet the following (DDR3-1066). The OMAP memory controller can delay the strobe to align to the clock at the memory. Therefore, the clock delay must be same or longer than the strobe.

Clock to strobe delay ($\text{clk} - \text{dqs} = D1$):

Default setting (invert clock): $-470 \text{ ps} < D1 < 470 \text{ ps}$

Approximate physical length: $-67 \text{ mm} < D1 < 67 \text{ mm}$

If D1 is not in this range, a noninvert clock can be used: $470 \text{ ps} < D1 < 1410 \text{ ps}$

Approximate physical length: $67 \text{ mm} < D1 < 201 \text{ mm}$

See the OMAP543x TRM to change invert clock setting.

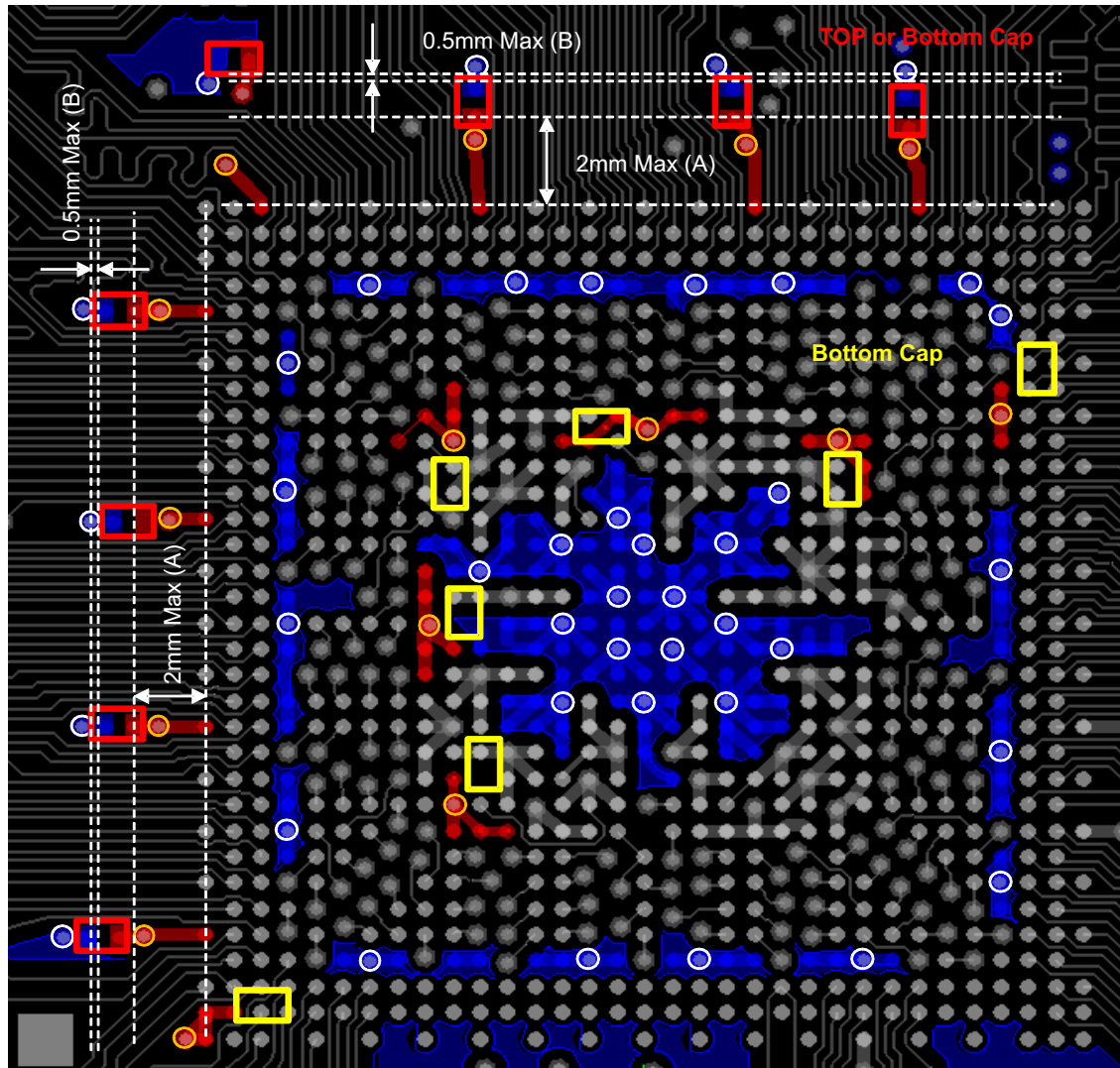
Maximum round trip delay ($\text{ckl} + \text{dqs} + 0.5 \times t_{\text{CK}} = D2$)

$D2 < 2231 \text{ ps}$

If you use the floor plan described in this chapter, these conditions will be met with good margin.

7.7.4.6 Power Plane

Layer 2 and layer 5 are planes. They are assigned to GND and VDD-IO/DDR3 supply (1.35 V). The OMAP5432 GND and VDD-IO BGA must be connected to the plane. As illustrated in [Figure 7-59](#), BGAs are depopulated so that critical via can be placed. GND/VDD-IO vias must be placed as mentioned in [Figure 7-59](#). VDD-IO BGA must be connected to the decoupling capacitor by 0.25-mm width line at maximum length of 2 mm (A). The GND/VDD-IO vias must be located next to the decoupling capacitor. The maximum pad-to-pad spacing must be less than 0.5 mm (B). The 7 bottom decoupling capacitors must be connected between VDD-IO vias and GND vias. The maximum VDD-GND loop must be less than 2.5 mm.



SWPS044-037

Figure 7-59. Critical Via and Decoupling Capacitor Connection

The layer 2 and layer 5 planes must be secured in the area as indicated in [Figure 7-60](#). Basically the layer 2 plane must be placed anywhere the layer 1 signal line is present and the layer 5 plane for layer 6 signals. No other signal line is present in the plane secure area.

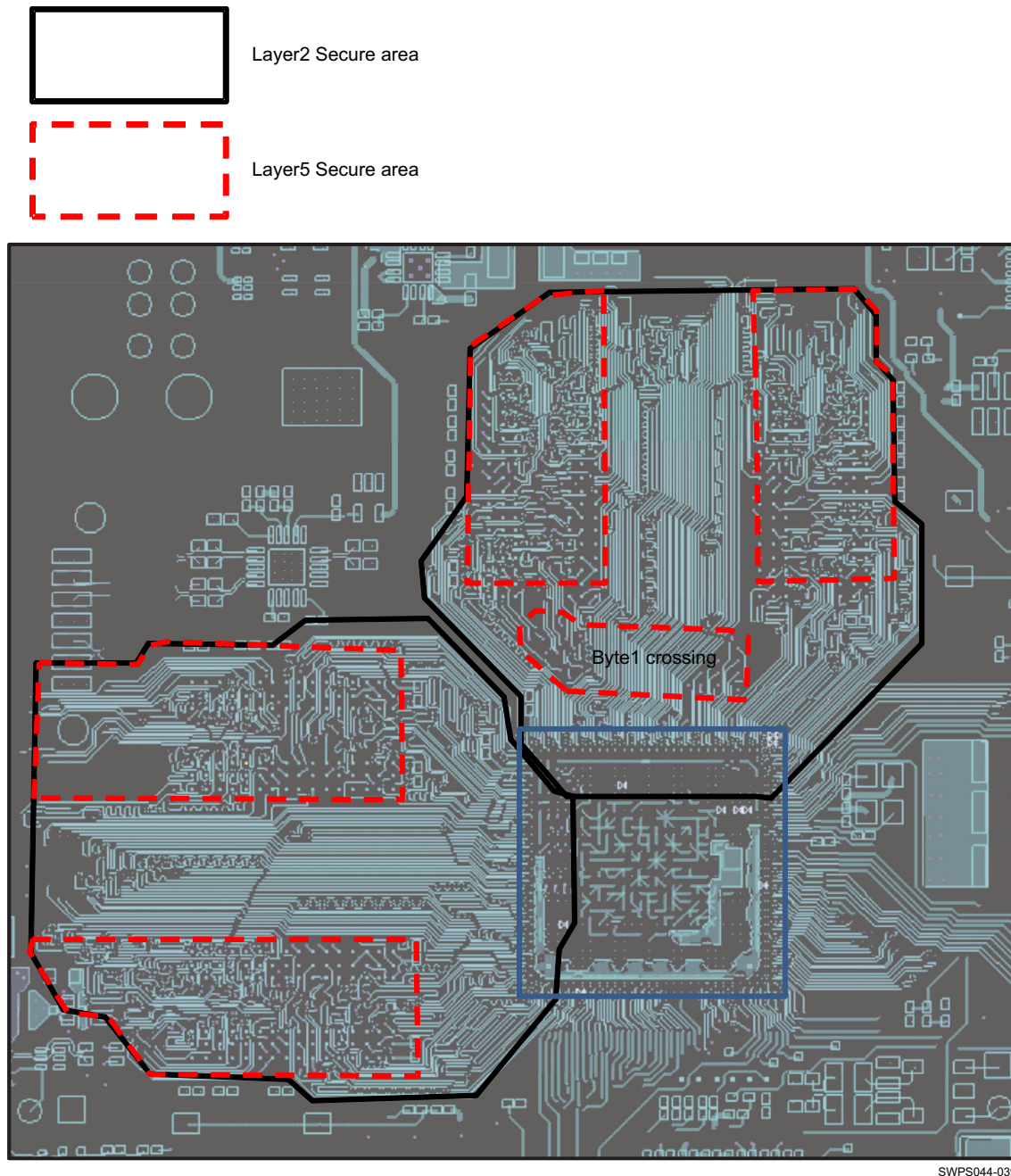


Figure 7-60. Layer 2/Layer 5 Plane Secure Area

7.7.4.7 Vref Routing

There are two Vref balls per channel. They are routed to DDR3 VREFDQ and VREFCA along with the CA bus. A greater than or equal to 500- μm wide trace must be used with a minimum 150- μm space from other signals. A 0.1- μF decoupling capacitor must be connected at both ends.

7.7.5 HDI PCB

7.7.5.1 Floor Plan

The high-level floor plan is almost identical to the PTH PCB. As already shown in [Figure 7-52](#), layer 1 is GND and the signals are routed by layer 2. Layer 3 is the VDD plane. With this sandwich structure, layer 2 works as a strip-line.

The impedance of layer 2 (75 μm) is 39 to 42 Ω and that is matched to the drive impedance of the IO ($R_{on} = 40 \Omega$). Crosstalk to or from the adjacent lines is smaller than the microstrip structure.

The DQ bit swap is applied as PTH PCB, it helps to simplify the routing (see).

As described in [Section 7.7.5.3](#), the crossing of address signals to the bottom memories can be done at the memory ball. Therefore, command routing topology shown in [Figure 7-57](#) must be used. L1 and L6 are used to cross address lines to the bottom memory.

7.7.5.2 DQ Signal Routing

[Figure 7-61](#) and [Figure 7-62](#) show the test layout by 1-4-1 HDI PCB. Layer 1 is covered by the GND plane, and layer 2 is used for connecting data signal to memory. Layer 5 is used to cross the data signals to the bottom memories.

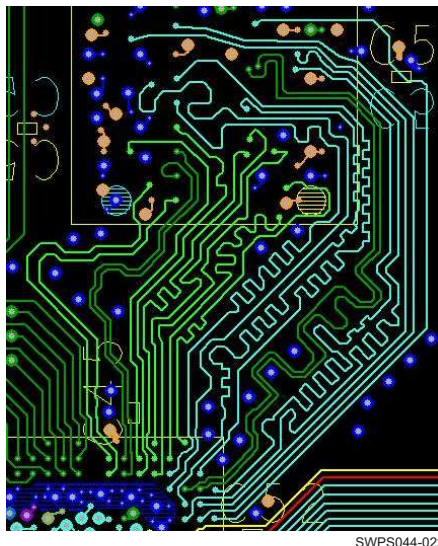


Figure 7-61. Routing DQ0/2 (L2)



Figure 7-62. Routing DQ0/2 (L1)

7.7.5.3 Command-Address Routing

Figure 7-63 and Figure 7-64 show how CA signals are routed by HDI PCB. It is possible to cross the signal for the bottom memory at the memory balls. The vias are placed at the middle of the memory to balance the small-T as much as possible. L1 is used to cross inner balls (rows 3 and 7) and L6 for outer balls (rows 2 and 8).

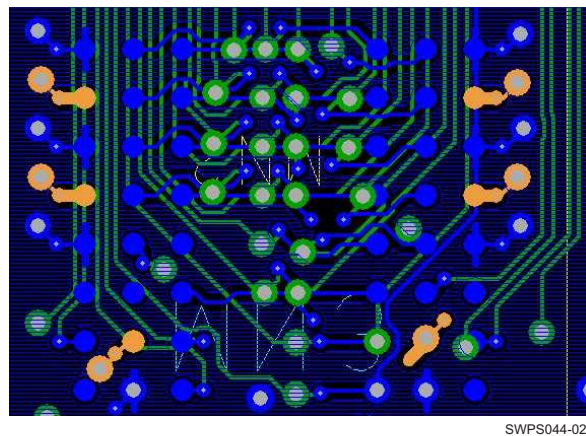
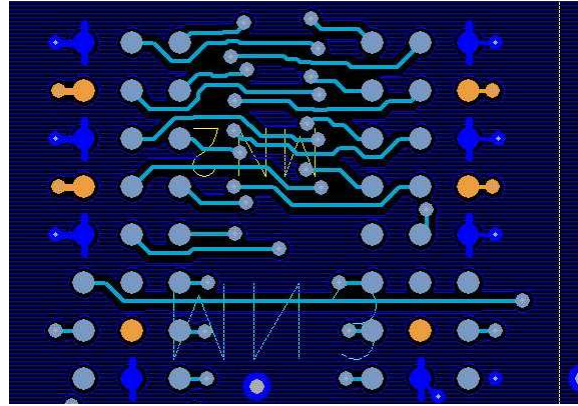


Figure 7-63. Command-Address Routing L1/L2



SWPS044-025

Figure 7-64. Command-Address Routing L6

8 Device and Documentation Support

8.1 Device Support

This device is currently in development. Experimental / Prototype devices are shipped against the following disclaimer:

“This product is still in development and is intended for internal evaluation purposes.”

Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, for experimental / prototype devices.

8.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development for OMAP platforms:

[OMAP5432 Pad Configuration Tool](#) is an interactive pad-configuration tool that allows the user to visualize the device pad configuration state on power-on reset and then customize the configuration of the pads for the specific use-case and identify the device register settings associated to that configuration.

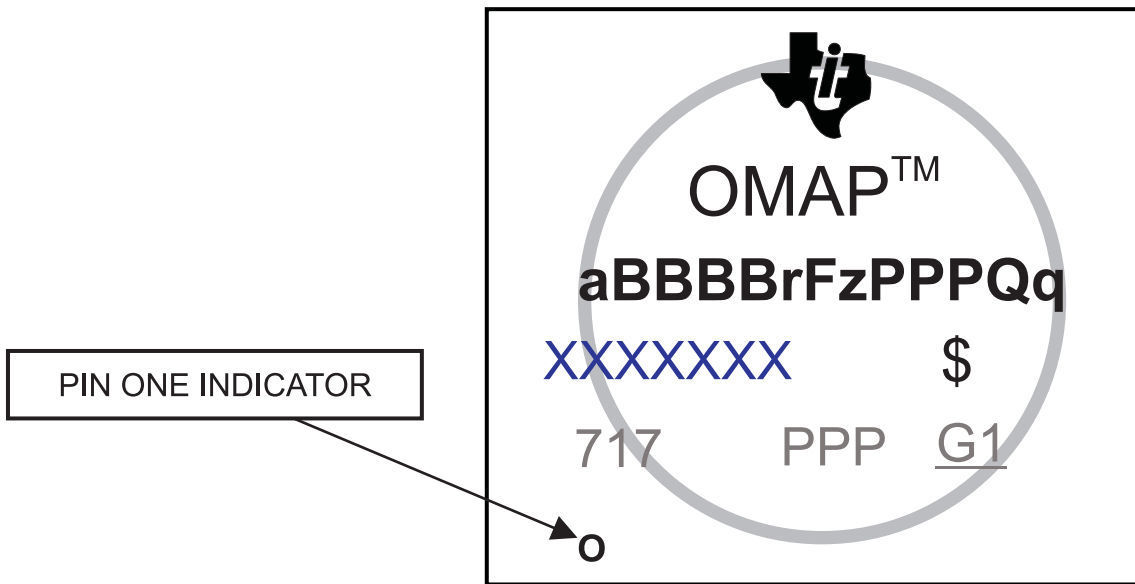
[OMAP Register Descriptor Tool](#) is an interactive OMAP register configuration tool that allows users to visualize the register state on power-on reset, and then customize the configuration of the device for the specific use-case.

[OMAP543x Clock Tree Tool](#) is interactive clock tree configuration software that allows the user to visualize the device clock tree, interact with clock tree elements and view the effect on PRCM registers, interact with the PRCM registers and view the effect on the device clock tree, and view a trace of all the device registers affected by the user interaction with the clock tree.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.1.2 Device Nomenclature

8.1.2.1 Standard Package Symbolization

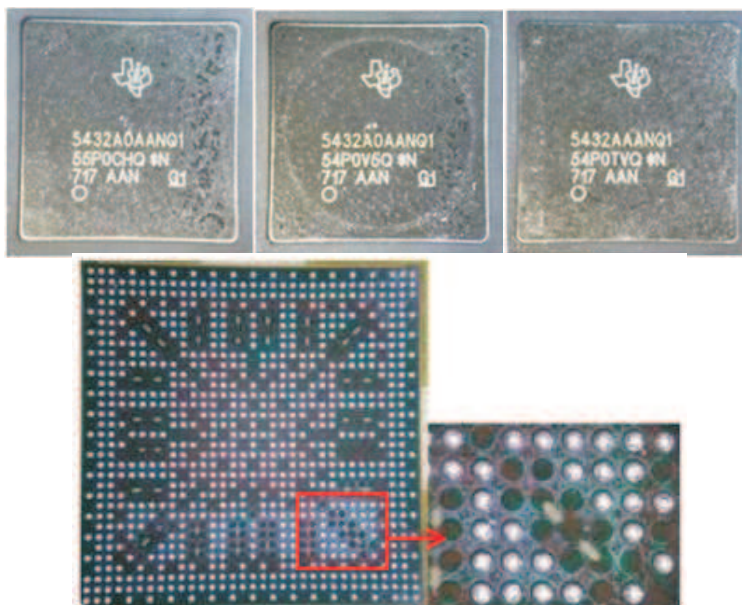


SWPS050-005

Figure 8-1. Printed Device Reference

NOTE

Some devices have a cosmetic circular marking visible on the top of the device package and/or other cosmetic markings on the top or bottom of the device package that are perceived as a roughness or texture of the surface of the device.



SWPS050-005A

Figure 8-2. Examples of Cosmetic Markings

8.1.2.2 Orderable Part Number

The actual part number used in the system follows this syntax:

- SAP part number: aBBBBrFzYyPPPRQq

8.1.2.3 Device Naming Convention

Table 8-1. Nomenclature Description

| FIELD PARAMETER | FIELD DESCRIPTION | VALUE | DESCRIPTION |
|-----------------|---|-------|--|
| a | Device evolution stage ⁽¹⁾ | X | Prototype |
| | | BLANK | Production |
| BBBB | Base production part number | 5432 | 17x17 mm DDR3 |
| r | Device revision | BLANK | 1.0 |
| | | A | 2.0 |
| F | Fabrication flow code ⁽²⁾ | BLANK | Production |
| | | A | Silicon Fab.: UMC12A, Assembly: AMKOR (Prototype only) |
| | | B | Silicon Fab.: UMC12A, Assembly: Shinko (Prototype only) |
| z | Device Speed | BLANK | High speed grade (Max MPU OPP = OPP_HIGH) |
| | | 0 | Nominal speed grade (Max MPU OPP = OPP_NOM) |
| Yy | Device type | BLANK | General purpose (Production) |
| | | GP | General purpose (Prototype) |
| | | XX | Reserved |
| PPP | Package designator | AAN | AAN S-PBGA-N754 (Prototype and Production) |
| R | Tape/Reel | BLANK | Tray |
| | | R | Tape/Reel |
| Qq | Automotive Designator | BLANK | not meeting automotive qualification |
| | | Q1 | meeting Q100 qualification requirements, with exceptions as specified in DM. |
| XXXXXXX | Lot Trace Code (LTC) | | |
| \$ | Fabrication designator, For TI use only | | |
| 717 | Production Code, For TI use only | | |
| O | Pin one designator | | |
| G1 | ECAT—Green package designator | | |

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices. Prototype devices are shipped against the following disclaimer:
 “This product is still in development and is intended for internal evaluation purposes.”
 Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

(2) The fabrication flow code will include the silicon fabrication site and / or assembly site and / or test site (Prototype only).

NOTE

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

8.2 Documentation Support

The following documents describe the OMAP5432 device. These documents are available at www.ti.com.

SWPU249 *OMAP543x Multimedia Device Technical Reference Manual [Public Version]* details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the OMAP543x family of devices.

SWPZ037 *OMAP543x Silicon Errata (Silicon Revision 2.0)* describes known advisories on silicon and provides workarounds.

SWCU130 *OMAP5432 EVM System Reference Manual* describes the OMAP5432 evaluation module (EVM) hardware and interfaces.

Tip: Search TI.com using literature numbers.

8.2.1 FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

8.2.2 Information About Cautions and Warnings

This book may contain cautions and warnings.

CAUTION

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

WARNING

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

8.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI Embedded Processors Wiki *Texas Instruments Embedded Processors Wiki*.

Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

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8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

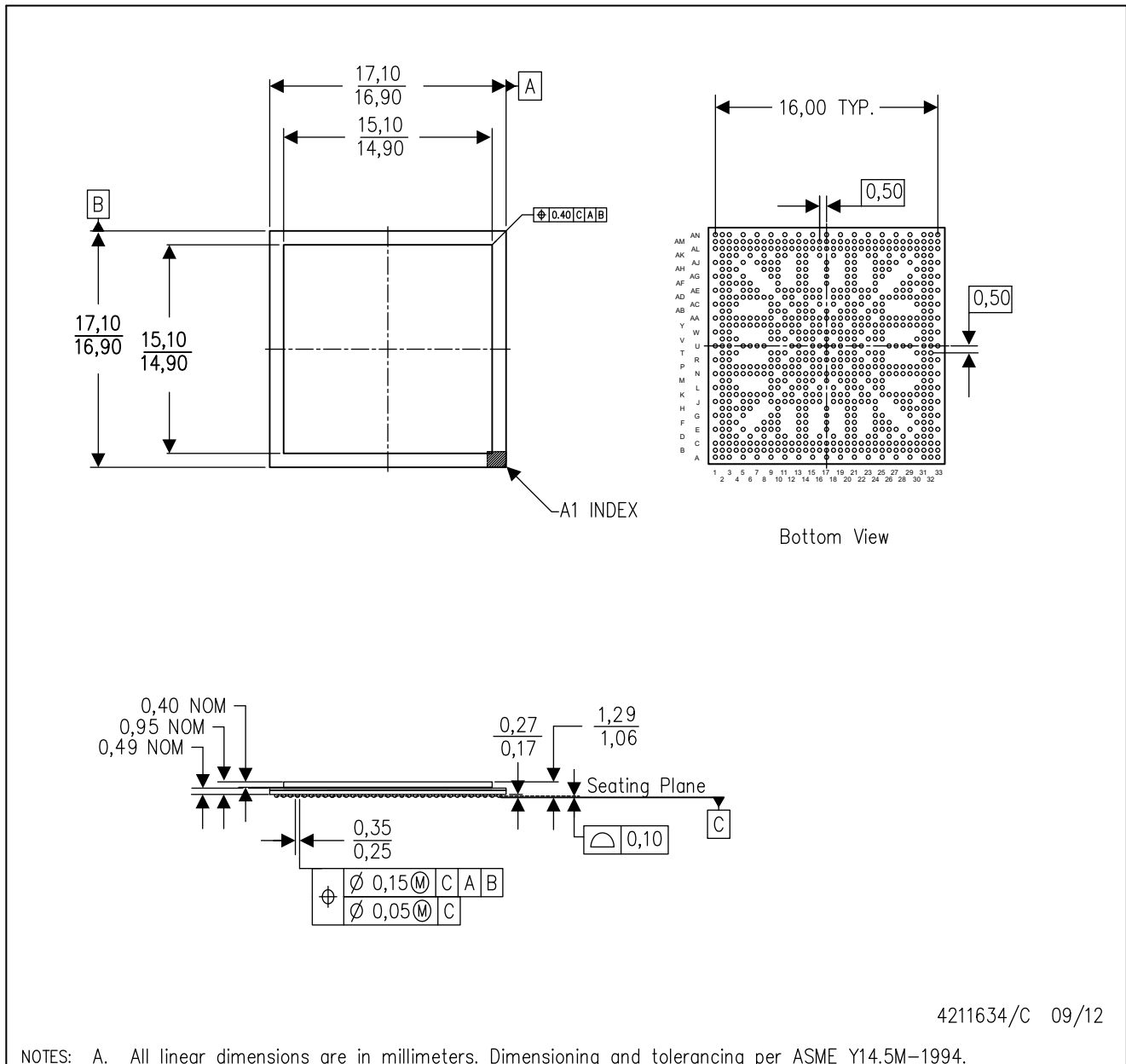
9 Mechanical Packaging and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Mechanical Data

AAN (S-PBGA-N754)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

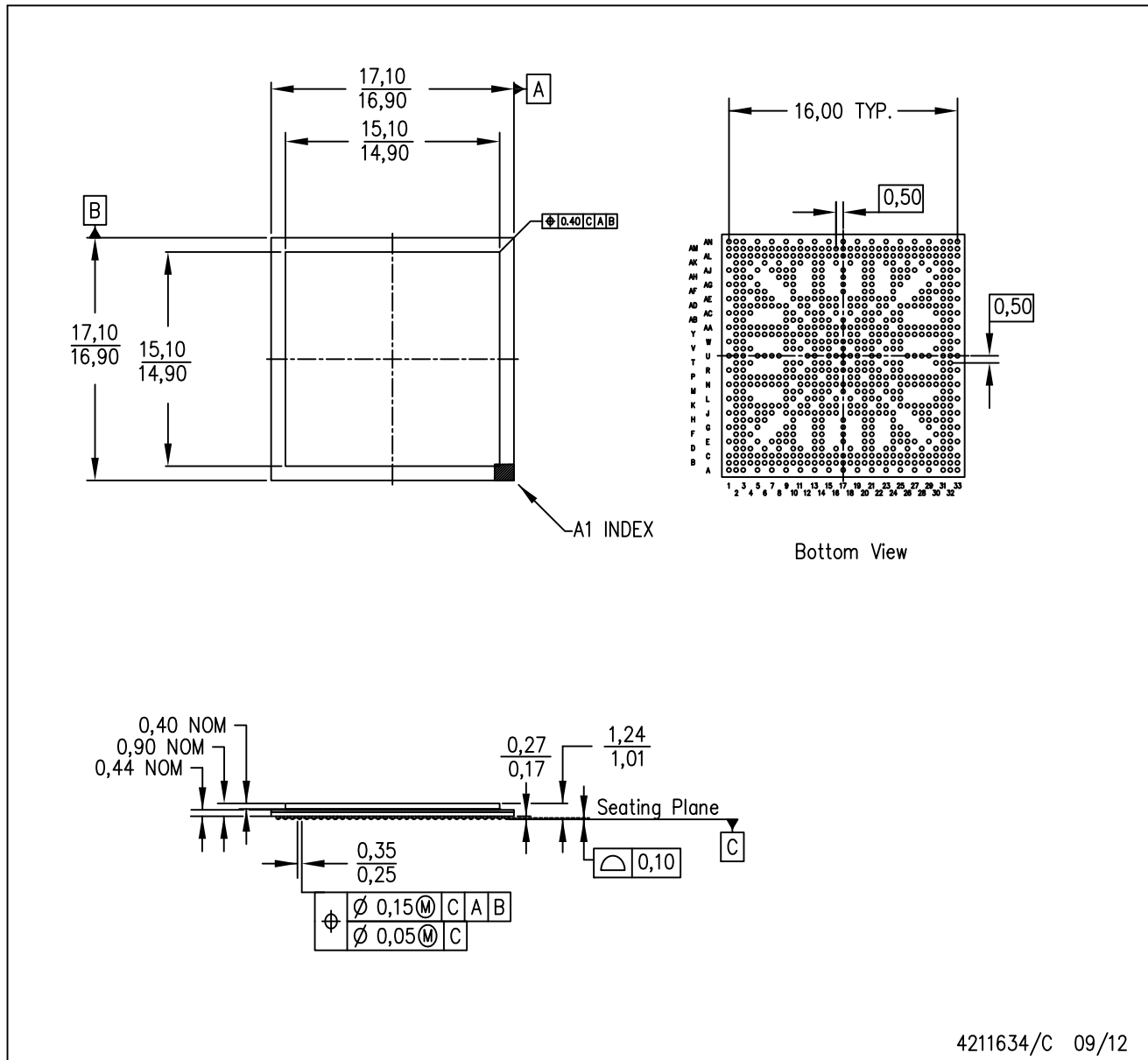
- B. This drawing is subject to change without notice.
- C. Flip chip application only.
- D. Pb-free die bump and solder ball.

SWPS050-001

Figure 9-1. Mechanical Package

AAN (S-PBGA-N754)

PLASTIC BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.
 C. Flip chip application only.
 D. Pb-free die bump and solder ball.

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