

SSD2858

Advance Information

Dual MIPI DSI Tx for WQXGA with Frame Buffer

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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SSD2858

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Appendix 1: IC Revision history of SSD2858 Specification

Version	Change Items	Effective Date
0.10	1 st Release	9-Aug-13
0.20	<ol style="list-style-type: none"> 1. Revise Pin59 as C11N 2. Revise storage temperature 3. Revsied DC characteristics 	11-Sep-13
1.0	<p>Initiail release of Advance Information</p> <ol style="list-style-type: none"> 1. Delete eFuse related information 2. Include frequency range of crystal (XTAL) 20~30MHz 3. Update DC characteristics 4. Revise min setting of VDPS = 10 5. Revise TE_SEL description 6. Include limitation on Special Register 0xFF 	28-Nov-13
1.1	<ol style="list-style-type: none"> 1. Update description for MIPITX – 0x000C, 0x0010 2. Include condition for DC characteristics 	17-Feb-14

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1 Device Overview

Introduction

This chapter presents an overview of the features of the SSD2858 architecture, component modules and subsystems. The pin table and the system memory map are described in the following chapters.

Features

Features of the SSD2858 include:

- MIPI input – 4 lanes, each up to 1.5Gbps
- Half-WUXGA (0.5 x 1920 x 1200 pixels) frame buffer
- Dual MIPI output – 2 x DSI with 2 individual clock lanes, sharing 4 lanes, each up to 1.5Gbps.
- Support both video and command MIPI input and splitting into 1 or 2 MIPI DSI video output
- Support compressed MIPI input as well as compressed MIPI output, allowing reduced bandwidth requirement at both MIPIRX and MIPITX links of SSD2858. 2 types of compression are supported.
 - SSL segment-based (4 pixels per segment) data compression/decompression with zero software overhead
 - Qualcomm line-based compression and decompression
- Image enhancement (Contrast, sharpness, brightness, hue correction, sunlight readability enhancement)
- Support rotation up to 1280x800 resolution with SSL Compression
- Support rotation up to 960x600 resolution without image compression
- Bi-cubic image scaler supporting fractional scaling
- Support independent bi-directional data transfer (forward link in High Speed and Low Power mode and reverse link in Low Power mode) for each DSI
- Support Ultra low power mode in idle state for all DSI engines
- On-chip PLL with variable output frequency which will allow lower video refresh rate for oxide-TFT panel
- Support MIPI (Video+Command) mode
- All MIPI packets re-transmission is done automatically once initial setup is performed
- Reduce power consumption and decrease EMI by using low amplitude signal over differential pair for serial data.
- Built-in high efficiency charge pump to generate 3.3V for VDDRAM
- Power supply: (VCORE and AVDD*) 1.2V +/-5%
- IO Power supply: (VDDIO and VCI*) 1.8 +/-5%
- Support of MIPI standard DSI(v1.01.00), DCS(v1.02.00), D-PHY (v1.1)
- Operating Temperature : -40 to 125 deg C

Overview

The SSD2858 is a MIPI in, MIPI out bridge chip with built-in half-WUXGA-RAM, high-quality fractional scaler, rotation engine, and data compression. It targets two main applications.

1. Low power system – The on-chip RAM allows self-refreshing of the panel, enabling the host application processor to go into ultra-low power mode.
2. Bridge host application processor (AP) and panel of different resolution – The fractional scaler allows any input resolution from the AP to be scaled to any resolution of the panel, up to WUXGA resolution.

Below shows the block diagram for SSD2858:

Note: While the diagram below shows 2 sets of (horizontal and vertical scaler), there is only one set in SSD2858. This means that either down-scaling before going into the RAM or up-scaling after reading from the RAM can be supported, but not both at the same time.

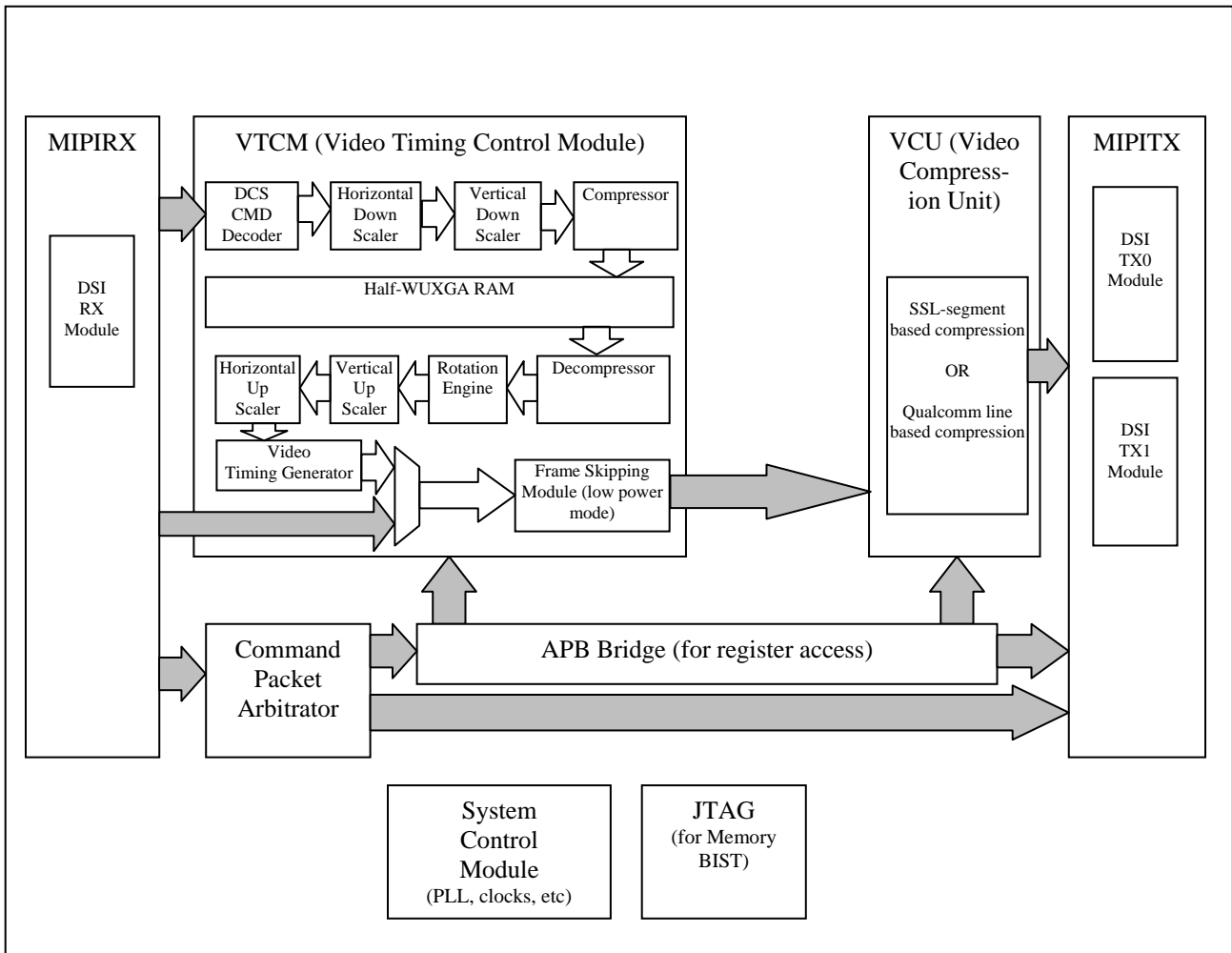


Figure 1-1: SSD2858 Block Diagram

Description

The following sections briefly describe the modules inside the SSD2858.

MIPI DSI RX (MIPIRX)

MIPI DSI RX is a MIPI compliant DSI receiver support up to 4 x 1.5Gbps lanes. It receives MIPI signals and converts them to parallel video and/or command interface to downstream modules. MIPIRX has the following features:

- High Speed transmission from 1 data lane to 4 data lanes
- Support up to 1.5Gbps per lane
- Support Video transfer in High Speed mode
- Support 16, 18 and 24 bit per pixel video transfer
- Support High Speed, Low Power and Ultra Low Power modes in forward link and Low Power mode in reverse link.
- Support of MIPI standard DSI(v1.0), DCS(v1.0), D-PHY (v1.0)

Video Timing Control Module (VTCM)

VTCM is the complex module within SSD2858, responsible for receiving video and commands from MIPI DSI RX module, storing them into on-chip frame buffer, and generating video timing to downstream modules. It is also responsible for DCS command decoding, compression/decompression, rotation and scaling. VTCM has the following features:

- DCS command or video bypass together with data compression (SSL segment-based & Qualcomm line-based) to reduce the bandwidth requirement during data transmission.
- Support real-time update of Qualcomm capabilities exchange
- 90 degree anti-clockwise rotation mode together with horizontal and vertical flip to complete the 90, 180 & 270 degree rotation.
- Horizontal & vertical scaler to up & down scale the video data
- Built-in frame buffer to support video data self-refresh, so the refresh frequency from application processor can be reduced or stopped during static frames.
- Low power mode support via frame skipping
- Variable pixel clock generation to dynamically change video refresh rate for power saving
- Various tearing output mode to support real time anti-tearing data update.
- Idle frame detection and controllable black/white frame insert to avoid sticky frame when input data are static

Video Compression Unit (VCU)

The Video compression unit allows compression of the video stream before going into MIPI DSI TX module for MIPI link transmission. This will reduce the MIPI link speed for lower power consumptions. It supports SSL-segment based compression

MIPI DSI TX (MIPITX)

MIPITX is a dual DSI TX module, support up to 2 clock lanes, 8 data lanes each capable of up to 1.5Gbps.

Clock Controller, Oscillator, and Phase Locked Loop (SCM)

The clock controller, oscillator, and PLL provide the various clocks required by the all the modules in the system. All these controls are encapsulated in SCM (System Control Module).

Charge Pump

This built-in charge pump uses flying capacitor architecture and is responsible to generate 3.3V power from 1.8V power. The 3.3V power is required for internal frame buffer as well as efuse

2 System Map

Introduction

This chapter provides information on the memory map of the SSD2858 for the various sub-modules. It also provides the various test modes of the chip.

All registers in SSD2858 are accessed via Generic Long Packets with 6 parameters, which will represent 16bit address and 32bit data, as shown below:

Parameter 0	REG_ADDR[15:8]
Parameter 1	REG_ADDR[7:0]
Parameter 2	REG_DATA[31:24]
Parameter 3	REG_DATA[23:16]
Parameter 4	REG_DATA[15:8]
Parameter 5	REG_DATA[7:0]

Table 2-1: Register Access Generic Long Packet

The generic long packets containing the above parameters are translated to AMBA APB interfaces internally as all modules' registers are accessed via APB interfaces.

Note: VTCM module, besides having registers accessed by APB interface, support registers defined by DCS commands, of which will be accessed by DCS command directly.

Memory Map

The following table provides the memory map of the modules that can be accessed by external AP.

Table 2-2: System Memory Map

Start	End	Range	Function	Remarks
0x0000	0x0FFF	4KB	SCM	
0x1000	0x1FFF	4KB	MIPIRX	
0x2000	0x2FFF	4KB	VTCM	
0x3000	0x3FFF	4KB	Reserved	
0x4000	0x4FFF	4KB	VCU	
0x5000	0x5FFF	4KB	GPIO	
0x6000	0x6FFF	4KB	MIPITX	
0x7000	0x7FFF	4KB	Reserved	
0x8000	0xFFFF	4KB	Reserved	

Command Retransmission (Special Generic Packet with Parameter 0 = 0xFF)

There are cases where MIPI Generic or DCS commands received from MIPIRX need to be retransmitted out of SSD2858 via MIPITX. These commands are not meant for SSD2858 internal usage. SSD2858 supports this use case by defining a packet to allow AP (Application Processor) to indicate whether the subsequent streams of command packets are meant for SSD2858 internal or for retransmission via MIPITX.

The special packet is a Generic Short or Long Packet (DATAID=0x23), with the following parameters

Parameter 0	0xFF
Parameter 1	0x0: means subsequent command packets are meant for SSD2858 internal registers 0x1: means subsequent commands are meant for retransmission via MIPITX 0xFF: means this particular command will be reconstructed as a generic (long/short) packet for retransmission via MIPITX with parameter0=0xFF
Parameter 2 and beyond	If Parameter 0 and Parameter 1 are both 0xFF, then parameter N will become the (N-1)th parameter of the packets reconstructed for retransmission via MIPITX. E.g. If incoming generic packet has the following parameters (in ascending order): 0xFF, 0xFF, 0xA1, 0xA2, then the outgoing generic packet at MIPITX would be 0xFF, 0xA1, 0xA2 <i>*SSD2858 will not support outgoing generic packet at MIPITX has more than 3 parametes in this case</i>

3 Package and Pin Description

Introduction

This chapter provides the pin information. It also provides information on the pin multiplexing arrangement between the various functions.

Pin Function

The following table shows the pin functions:

Table 3-1: Pin Description

Name	Description
Modes and Clock/Reset Signals	
TEST [1:0]	Test Mode Configuration For normal operation, TEST[1:0]=2'b01
XTAL_IN	20 ~ 30MHz crystal clock Input
XTAL_OUT	20 ~ 30MHz crystal feedback clock
RESET	External Reset Input (Active low)
PMU_BYPASS	Disable PMU circuitry for power-down (deep-sleep) mode
MIPIRX Signals	
MRX_CP	MIPI RX Clock lane Terminal +
MRX_CN	MIPI RX Clock lane Terminal -
MRX_DP0	MIPI RX Data lane 0 Terminal +
MRX_DN0	MIPI RX Data lane 0 Terminal -
MRX_DP1	MIPI RX Data lane 1 Terminal +
MRX_DN1	MIPI RX Data lane 1 Terminal -
MRX_DP2	MIPI RX Data lane 2 Terminal +
MRX_DN2	MIPI RX Data lane 2 Terminal -
MRX_DP3	MIPI RX Data lane 3 Terminal +
MRX_DN3	MIPI RX Data lane 3 Terminal -
MIPI TX Signals	
MTX_CP0	MIPI TX DSI0 Clock lane Terminal +
MTX_CN0	MIPI TX DSI0 Clock lane Terminal -
MTX_DP0	MIPI TX DSI0 Data lane 0 Terminal +
MTX0_DN0	MIPI TX DSI0 Data lane 0 Terminal -

MTX0_DP1	MIPI TX DSI0 Data lane 1 Terminal +
MTX0_DN1	MIPI TX DSI0 Data lane 1 Terminal -
MTX0_DP2	MIPI TX DSI0 Data lane 2 Terminal +
MTX0_DN2	MIPI TX DSI0 Data lane 2 Terminal -
MTX0_DP3	MIPI TX DSI0 Data lane 3 Terminal +
MTX0_DN3	MIPI TX DSI0 Data lane 3 Terminal -
MTX1_CP1	MIPI TX DSI1 Clock lane Terminal +
MTX1_CN1	MIPI TX DSI1 Clock lane Terminal -
MTX1_DP4	MIPI TX DSI1 Data lane 0 Terminal +
MTX1_DN4	MIPI TX DSI1 Data lane 0 Terminal -
MTX1_DP5	MIPI TX DSI1 Data lane 1 Terminal +
MTX1_DN5	MIPI TX DSI1 Data lane 1 Terminal -
MTX1_DP6	MIPI TX DSI1 Data lane 2 Terminal +
MTX1_DN6	MIPI TX DSI1 Data lane 2 Terminal -
MTX1_DP7	MIPI TX DSI1 Data lane 3 Terminal +
MTX1_DN7	MIPI TX DSI1 Data lane 3 Terminal -
Display Related Signals	
TE	Tearing Signal Output
Charge Pump Signals	
C11P	Flying Capacitor 1 Terminal + (1uF)
C11N	Flying Capacitor 1 Terminal -
C12P	Flying Capacitor 2 Terminal + (1uF)
C12N	Flying Capacitor 2 Terminal -
CPOUT	3.3V Charge Pump output. To be connected to VDD_URAM_IO. Storage cap of 4.7uF to be connected to this pin.
Test Signals	
BG_OUT	Internal Bandgap output
Power Pins	
VDDRAM	3.3V URAM power (Also the power for Efuse) – connect to CPOUT pin
VDDIO	1.8V IO power
VCORE	1.2V Core power
AVDD_RX	1.2V MIPI RX Analog Power

AVDD_TX	1.2V MIPI TX Analog Power
AVDD_PLL	1.2V PLL Analog Power
VCL_BG	1.8V Bandgap Analog Power
VCL_CP	1.8V Charge Pump Analog Power
VSS	Ground
AVSS_RX	MIPIRX analog ground
AVSS_TX	MIPITX analog ground
AVSS_PLL	PLL analog ground
VSS_BG	Bandgap analog ground
VSS_CP	Chargepump analog ground

SSD2858QL9 Pin Assignment

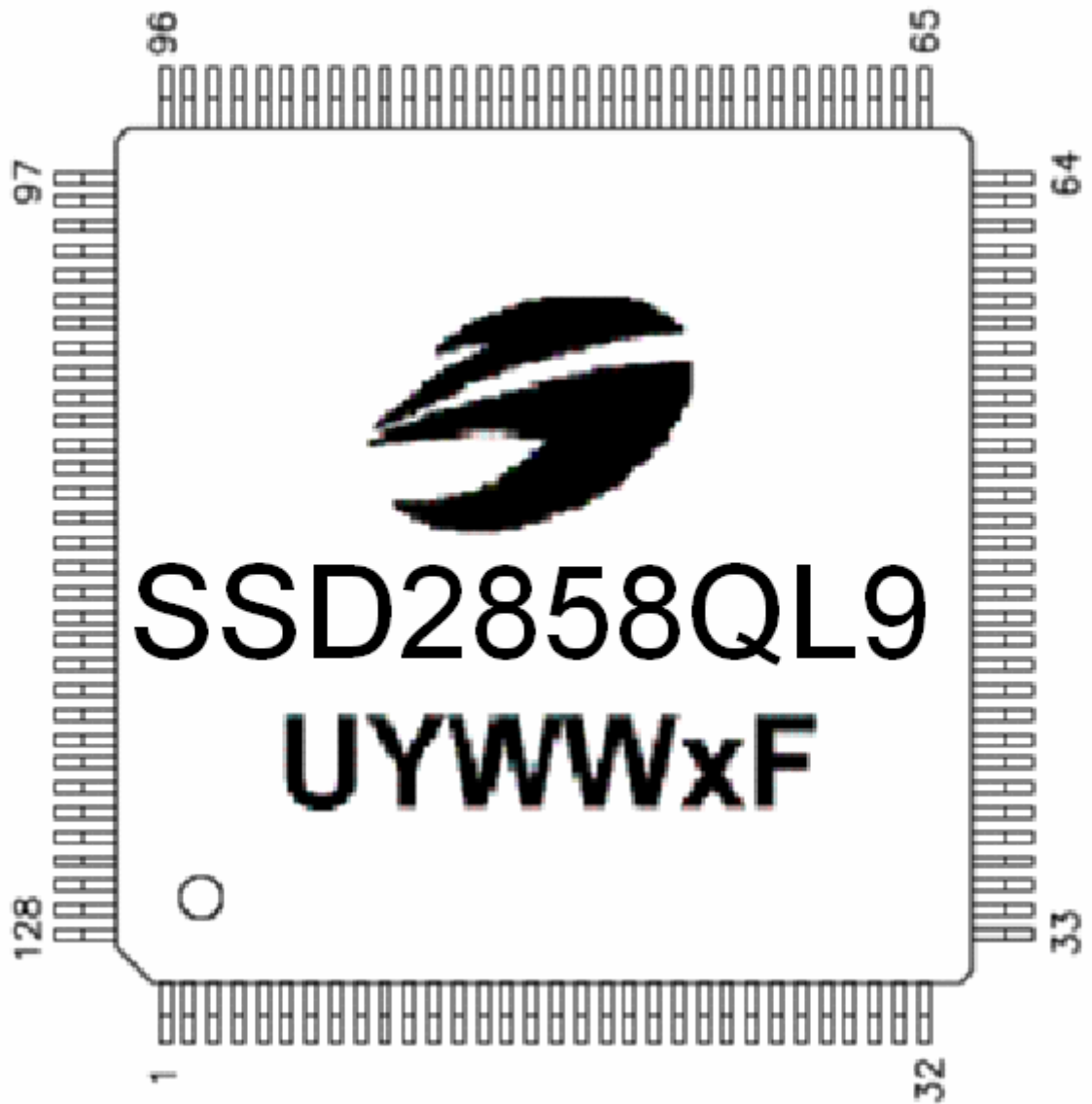


Figure 3-1: SSD2858QL9 Pinout Diagram – 128 LQFP

Pin Assignment Table

Pin #	QFP Pin name	Pin #	QFP Pin name	Pin #	QFP Pin name	Pin #	QFP Pin name
1	XTAL_OUT	33	RESET	65	C12N	97	AVSS
2	VDDIO	34	TEST1	66	VSS_CP	98	MTX_DP0
3	CLKOUT	35	TEST0	67	VDDRAM	99	MTX_DN0
4	VCORE	36	VSS	68	C12N	100	AVDD_TX
5	VSS	37	VCORE	69	VSS	101	MTX_DN1
6	VDDRAM	38	AVSS	70	VCORE	102	MTX_DP1
7	NC	39	MRX_DP3	71	NC	103	AVSS
8	NC	40	MRX_DN3	72	NC	104	MTX_CN0
9	NC	41	AVSS	73	NC	105	MTX_CP0
10	NC	42	AVDD_RX	74	NC	106	MTX_DN2
11	NC	43	MRX_DP2	75	NC	107	MTX_DP2
12	NC	44	MRX_DN2	76	NC	108	AVDD_TX
13	NC	45	MRX_CP	77	NC	109	AVSS
14	NC	46	MRX_CN	78	NC	110	MTX_DN3
15	NC	47	AVSS	79	NC	111	MTX_DP3
16	NC	48	MRX_DP1	80	NC	112	MTX_DN4
17	NC	49	MRX_DN1	81	NC	113	MTX_DP4
18	NC	50	AVDD_RX	82	NC	114	AVDD_TX
19	NC	51	MRX_DP0	83	NC	115	MTX_DN5
20	NC	52	MRX_DN0	84	NC	116	MTX_DP5
21	NC	53	AVDD_RX	85	NC	117	MTX_CN1
22	NC	54	VCORE	86	NC	118	MTX_CP1
23	NC	55	VCIBG	87	NC	119	AVSS
24	NC	56	BGOUT	88	NC	120	MTX_DN6
25	NC	57	VSS_BG	89	NC	121	MTX_DP6
26	NC	58	VSS_CP	90	NC	122	AVDD_TX
27	VDDRAM	59	C11N	91	VCORE	123	MTX_DP7
28	VSS	60	VCI_CP	92	AVSS	124	MTX_DN7
29	NC	61	C11P	93	AVSS	125	AVSS_PLL
30	TE	62	CPOUT	94	VSS	126	AVDD_PLL
31	VSSIO	63	C12P	95	VDDRAM	127	VCORE
32	VDDIO	64	VCI_CP	96	IBIAS_TX	128	XTAL_IN

Table 3-2: Pin assignment

Pin Selection

Pin selection is controlled via the GPIO module registers. A brief description is provided here and more details are available in the GPIO chapter. Pin selection is controlled in 2 levels. The first level selection allows functions to be selected between primary and alternate functions. At this level, the modules have direct control of the direction of signals. At the second level of selection, signal directions are fixed and are not under the control of the module.

Primary/Alternate pin selection

The primary signals are selected by default at power-up and the functions are active at the IO of SSD2858. Primary and alternate functions are selected via the GPIO Function Register. The direction of the signals is directly controlled by the module function that is enabled through the selection.

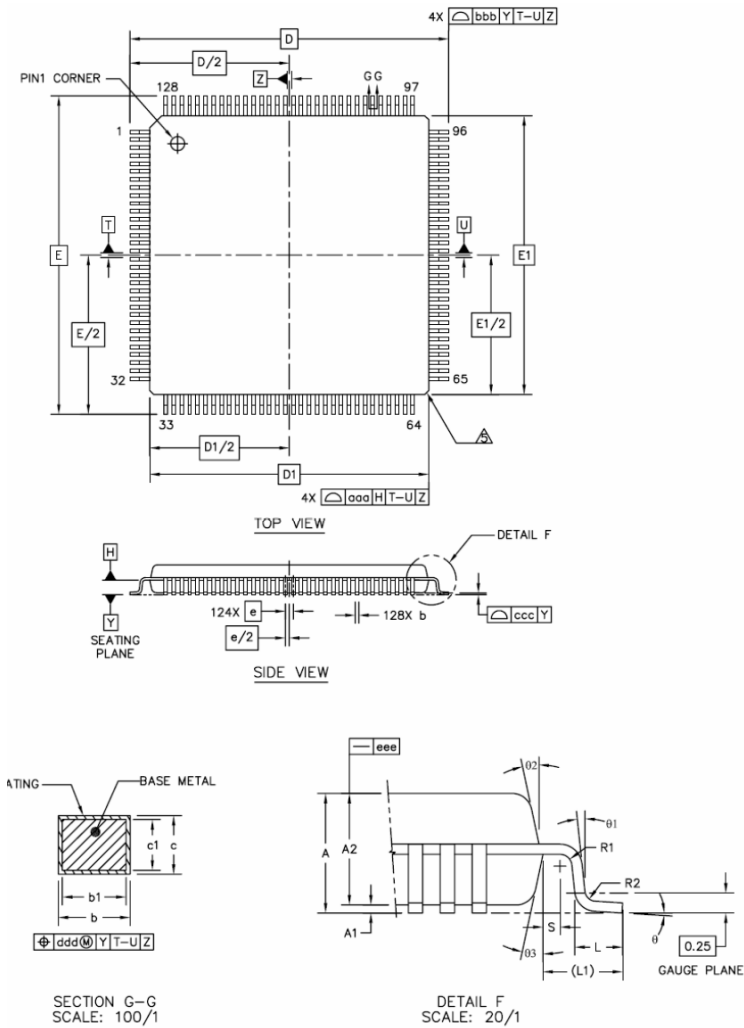
Ain/Bin/Cin/Aout/Bout

These groups of signals are selected through the second level of selection and controlled via the set of GPIO registers that control a set of IOMUXes at the pads. A signal in this group is enabled through the GPIO Mode Register. When a pin is configured as GPIO, the primary and alternate signals are blocked (not effective). This GPIO selection is performed through the GPIO Mode Register.

Once a pin has been configured as GPIO, then additional input and output configuration registers are used to select between Aout/Bout (external inputs with reference to SSD2858) and Ain, Bin, Cin (external outputs with reference to SSD2858). This selection is controlled via GPIO Input Source Select and GPIO Output Source Select Registers.

Dimension for SSD2858

Figure 3-2- Package Information



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	---	---	1.6
STAND OFF	A1	0.05	---	0.15
MOLD THICKNESS	A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)	b	0.13	0.16	0.23
LEAD WIDTH	b1	0.13	---	0.19
L/F THICKNESS(PLATING)	c	0.09	---	0.2
L/F THICKNESS	c1	0.09	---	0.16
	X	D	16 BSC	
	Y	E	16 BSC	
BODY SIZE	X	D1	14 BSC	
	Y	E1	14 BSC	
LEAD PITCH	e	0.4 BSC		
FOOTPRINT	L	0.45	0.6	0.75
	L1	1 REF		
	θ	0°	3.5°	7°
	$\theta 1$	0°	---	---
	$\theta 2$	11°	12°	13°
	$\theta 3$	11°	12°	13°
	R1	0.08	---	---
	R2	0.08	---	0.2
	S	0.2	---	---
PACKAGE EDGE TOLERANCE	ooo	0.2		
LEAD EDGE TOLERANCE	bbb	0.2		
COPLANARITY	ccc	0.08		
LEAD OFFSET	ddd	0.07		
MOLD FLATNESS	eee	0.05		

NOTES

- DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
- DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
- DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

Δ EXACT SHAPE OF EACH CORNER IS OPTIONAL.

TITLE:		PROJ.	DWG. NO.	REV.
PACKAGE OUTLINE				A
12BLD LQFP				SIZE
14 X 14 X 1.4 PKG. 0.4 PITCH				1 OF 1
2mm FOOTPRINT				A4
UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT		
MM	ASME Y14.5M	---		

Marking for SSD2858

Figure 3-3- Marking Information



4 Power Management

Introduction

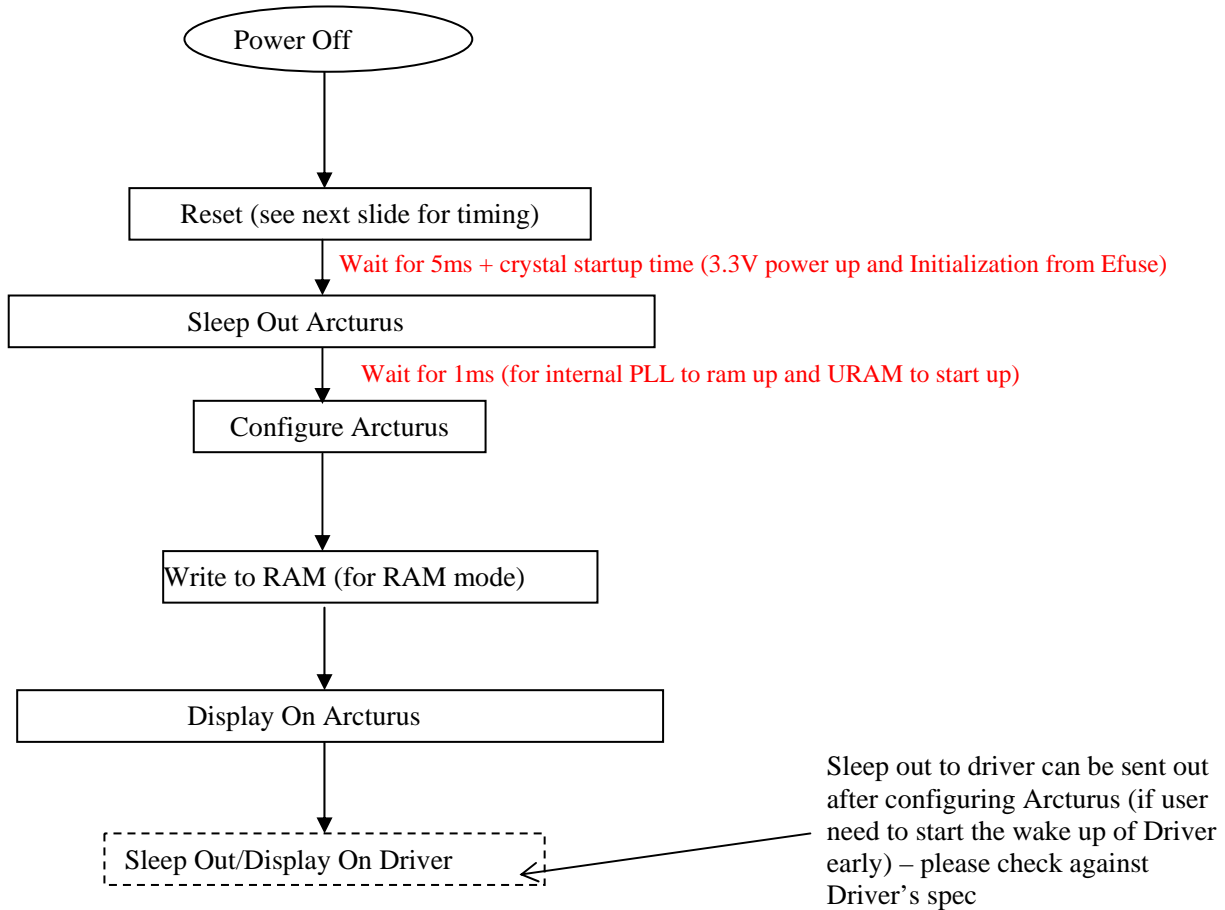
There are altogether 3 power modes for SSD2858.

1. Active Mode: Entered upon DCS sleep out command is received
2. Sleep Mode: Entered when DCS sleep in command is received
3. Power Down Mode: Entered by setting power cut bit in MIPIRX's 'Power Cut Register, and can only exit by resetting SSD2858

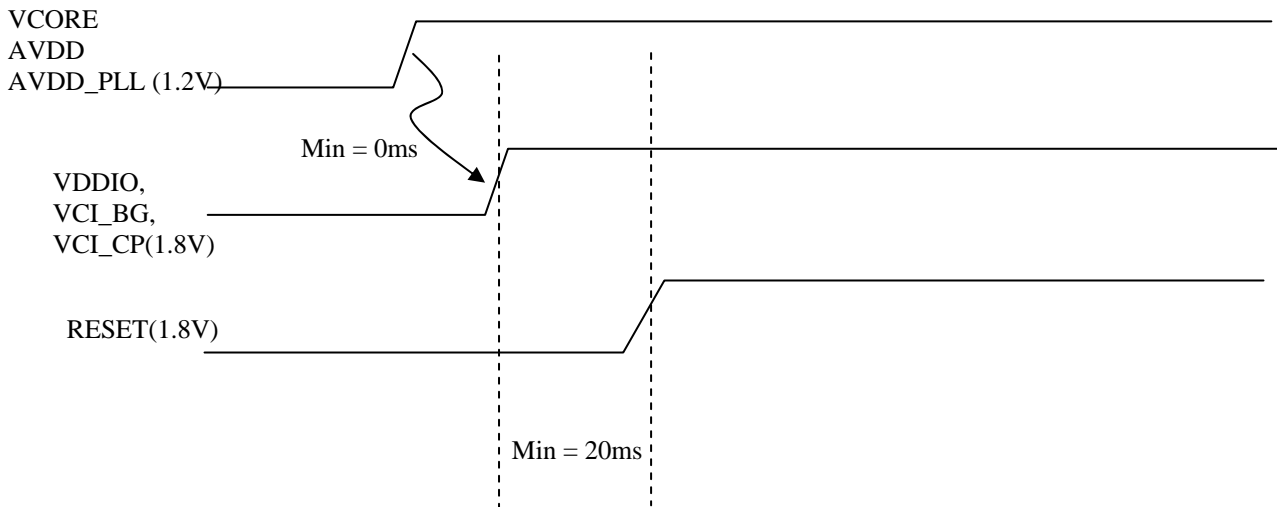
The subsequent section of this chapter will describe the power up/down sequences as well as the reset sequence

Power up Sequence

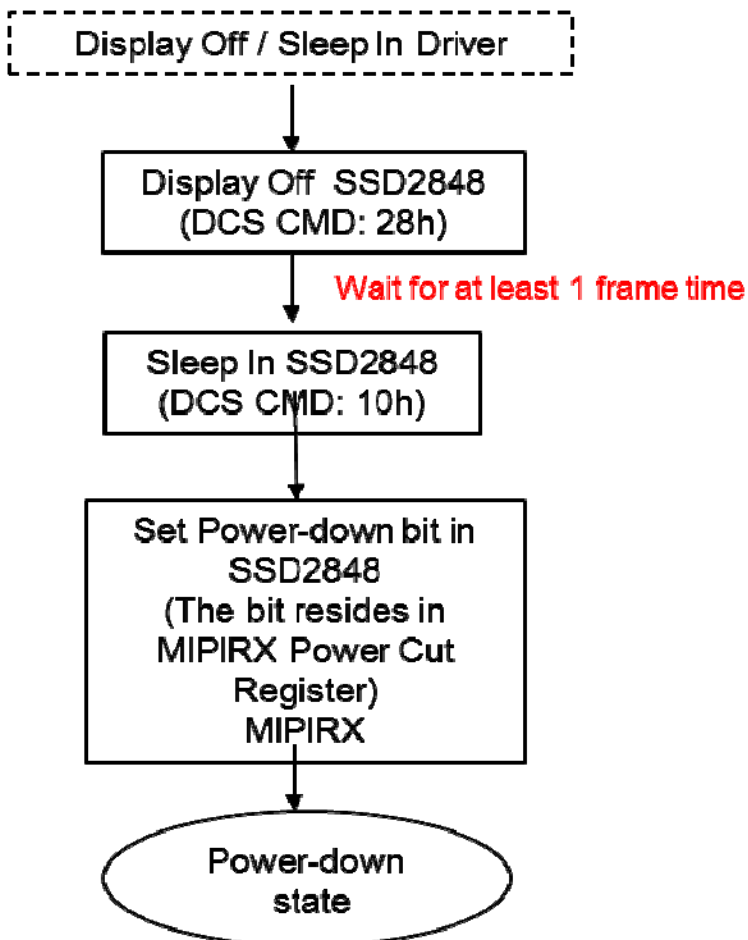
Note: After DCS Display On command is sent to SSD2858, then the TE signaling will start. If the application processor (AP) requires TE signal to write data into RAM, and in order not to have the first few frames displaying uninitialized memory content, VTCM module provides a programmable configuration (called 'Mask Frame Count') to allow the video timing to be generated only after Nth number of frames after Display On, where N=0-15.



Reset Sequence



Power down Sequence



5 System Control Module (SCM)

Features

This module controls the clocks and reset of SSD2858, and other miscellaneous chip functions.

The main clock diagram for the system is as shown below.

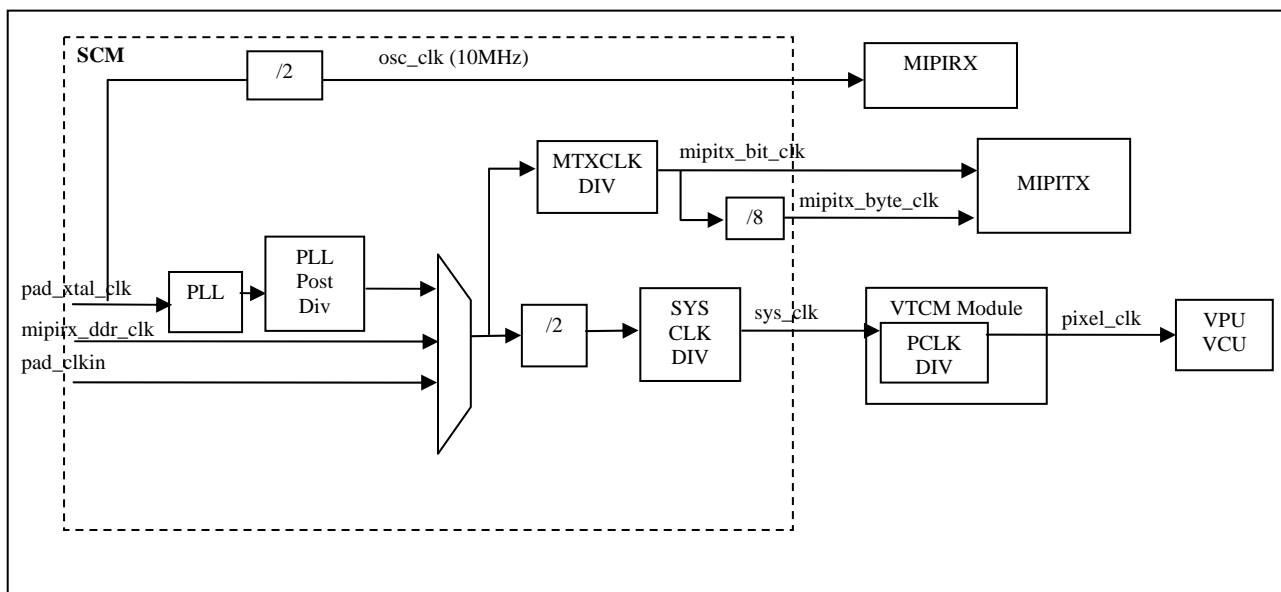


Figure 5-1 SSD2858 Clock Diagram

Programming Model

All reserved bits return zero on read and shall always be written with zero. Writing any other value to a reserved bit will result in indeterminate behavior.

Table 5–1: SCM Register Summary

Offset	Name	Mnemonic	Reset Value
0x0004	SCM Control Register	SCM_CTL	0x00000000
0x0008	SCM PLL Register	SCM_PLL	0x01F40132
0x000C	SCM Clock Control Register	SCM_CC	0x00000003
0x0010	SCM Miscellaneous Control 1 Register	SCM_MISC1	0xFFFFFFFF
0x0014	SCM Miscellaneous Control 2 Register	SCM_MISC2	0x0C77800F
0x001C	SCM MIPIRX PHY Control Register	SCM_MRXPHY	0x00001401
0x0020	SCM Analog Control 1 Register	SCM_ANACTL1	0x1592567D
0x0024	SCM Analog Control 2 Register	SCM_ANACTL2	0x00003300
0x0028	SCM Scratch Register	SCM_SCRATCH	0x00000000
0x002C	SCM Gap1 Register	SCM_GAP1	0x00000000
0x0030	SCM Gap2 Register	SCM_GAP2	0x00000000

1.1 Register Description

SCM Control Register

SCM_CTRL	SCM Control Register								Offset Address
									0x0004
BIT	31	30	29	28	27	26	25	24	
NAME									
TYPE									
RESET									
BIT	23	22	21	20	19	18	17	16	
NAME									
TYPE									
RESET									
BIT	15	14	13	12	11	10	9	8	
NAME									
TYPE									
RESET									
BIT	7	6	5	4	3	2	1	0	
NAME			PB						SWRST
TYPE			RO						RWAC
RESET									0

Table 5-2: SCM Control Description

Name	Description	Setting
Reserved Bit 31-6	Reserved	
PB Bit 5	PMU Bypass – Indicates the pin status of PMU_BYPASS	0: No PMU Bypass 1: PMU Bypass
TM Bit 4-1	Test Mode – Indicates the TM pin status	
SWRST Bit 0	SWRST – This bit all blocks except for MIPIRX block. This bit is self-clear. After this bit is set, user needs to wait for at least 1us before accessing any other registers in the entire device	0: No reset 1: All blocks are resetted except for MIPIRX

SCM PLL Register

Offset Address

SCM_PLL

SCM PLL Register

0x0008

BIT	31	30	29	28	27	26	25	24
NAME	LOCKCNT[15:8]							
TYPE	RW							
RESET	0	0	0	0	0	0	0	1
BIT	23	22	21	20	19	18	17	16
NAME	LOCKCNT[7:0]							
TYPE	RW							
RESET	1	1	1	1	0	1	0	0
BIT	15	14	13	12	11	10	9	8
NAME	OFF	MRX				POSTDIV		
TYPE	RW	RW				RW		
RESET	0	0			0	0	0	1
BIT	7	6	5	4	3	2	1	0
NAME				MULT				
TYPE				RW				
RESET		0	1	1	0	0	1	0

Table 5-3: SCM PLL Register Description

Name	Description	Setting
LOCKCNT Bit 31-16	PLL Lock count – This controls the time required for the PLL2 to be considered ‘lock’. It is counted based on input crystal clock divided-by 2 (10MHz for a 20MHz clock) – at least 30us is required	Number of 10MHz clock
OFF Bit 15	PLL OFF - This control the on/off of PLL	1=off 0=on (Default)
MRX Bit 14	MIPIRX DDR Clock – This using MIPIRX DDR clock to replace PLL clock output	0: PLL clock is used 1: MIPIRX DDR clock is used as ‘PLL clock’
Reserved Bit 13-12	Reserved	
POSTDIV Bit 11-8	Output Divide Ratio – This divider control the divide ratio of the output clock from PLL (or MIPIRX DDR clock when MRX bit is set)	0 = Divide by 1 1 = Divide by 2 (Default) 2 = Divide by 3 3 = Divide by 4 ... 15 = Divide by 16
Reserved Bit 7-6	Reserved	
MULT Bit 6-0	PLL Multiplier Ratio – This controls the multiplier setting of the PLL PLL output frequency (before post-divider) = Input frequency x MULT	0=Reserved 1=multiply by 1 2=multiply by 2 ...

Name	Description	Setting
	Input frequency = crystal input (20MHz)	Not all setting is allowed. The output frequency range of PLL is from 1GHz to 1.5GHz.

SCM Clock Control Register

SCM_CC									Offset Address
SCM Clock Control Register									0x000C
BIT	31	30	29	28	27	26	25	24	
NAME									
TYPE									
RESET									
BIT	23	22	21	20	19	18	17	16	
NAME									
TYPE									
RESET									
BIT	15	14	13	12	11	10	9	8	
NAME									
TYPE									
RESET									
BIT	7	6	5	4	3	2	1	0	
NAME	MTXDIV				SYSDIV				
TYPE	0	0	0	0	0	0	1	1	
RESET									

Table 5-4: SCM Clock Control Register Description

Name	Description	Setting
Reserved Bit 31-8	Reserved	
MTXDIV Bit 7-4	MIPITX Bit Clock Divider – This controls the divide ratio from PLL output clock (after post-divider), to generate the MIPITX bit clock. See clock diagram at the beginning of this chapter. <u>Only even division is allowed</u>	0 = Divide by 1 (Default) 1 = Divide by 2 3 = Divide by 4 ... 15 = Divide by 16
SYSDIV Bit 3-0	System Clock Divider – This controls the divide ratio from PLL output clock (after post-divider and a further divide-by-2), to generate the system clock. See clock diagram at the beginning of this chapter	0 = Divide by 1 1 = Divide by 2 2 = Divide by 3 (Default) 3 = Divide by 4 ... 15 = Divide by 16

SCM Miscellaneous Control 1 Register

Offset Address

SCM_MISC1

SCM Miscellaneous Control 1 Register

0x0010

BIT	31	30	29	28	27	26	25	24
NAME	DS_PA15		DS_PA14		DS_PA13		DS_PA12	
TYPE	RW		RW		RW		RW	
RESET	1	1	1	1	1	1	1	1
BIT	23	22	21	20	19	18	17	16
NAME	DS_PA11		DS_PA10		DS_PA9		DS_PA8	
TYPE	RW		RW		RW		RW	
RESET	1	1	1	1	1	1	1	1
BIT	15	14	13	12	11	10	9	8
NAME	DS_PA7		DS_PA6		DS_PA5		DS_PA4	
TYPE	RW		RW		RW		RW	
RESET	1	1	1	1	1	1	1	1
BIT	7	6	5	4	3	2	1	0
NAME	DS_PA3		DS_PA2		DS_PA1		DS_PA0	
TYPE	RW		RW		RW		RW	
RESET	1	1	1	1	1	1	1	1

Table 5-5: SCM Miscellaneous Control 1 Register Description

Name	Description	Setting
DS_PA15-0 Bit 31-0	Drive Strength Control for GPIO Port A, index 15, to 0	

SCM Miscellaneous Control 2 Register

Offset Address

SCM_MISC2

SCM Miscellaneous Control Register

0x0014

BIT	31	30	29	28	27	26	25	24
NAME			GPIOCKE	MTX3DSI	MTXVPF		MTXVVC	
TYPE			RW	RW	RW		RW	
RESET			0	0	1	1	0	0
BIT	23	22	21	20	19	18	17	16
NAME	MTXSLP	MRXEN	MRXLS		MRXVB	MRXECC	MRXCRC	MRXEOT
TYPE	RW	RW	RW		RW	RW	RW	RW
RESET	0	1	1	1	0	1	1	1
BIT	15	14	13	12	11	10	9	8
NAME	MRXEE	MRXCE						
TYPE	RW	RW						
RESET	1	0						
BIT	7	6	5	4	3	2	1	0
NAME	CLKOUT_SEL				DS_PA17		DS_PA16	
TYPE	RW				RW		RW	
RESET	0	0	0	0	1	1	1	1

Table 5-6: SCM Miscellaneous Control 2 Description

Name	Description	Setting
Reserved Bit 31-28	Reserved	
Reserved Bit 30	Reserved	
GPIOCKE Bit 30	GPIO Clock Enable – Enable GPIO clock for interrupt mode enable	0=Disable 1=Enable
MTX3DSI Bit 28	MIPITX 3 DSI Mode Enable – Enable 3 DSI mode for MIPITX (2 lanes each only)	0=Disable 1=Enable
MTXVPF Bit 27-26	MIPITX Video Pixel Format – Pixel format of video output from MIPITX	0 = Reserved 1 = 16bpp 2 = 18bpp 3 = 24bpp
MTXVVC Bit 25-24	MIPITX Video Virtual Channel (VC) – Determines to VC field of the video packet to be sent out from MIPITX	VC field
MTXSLP Bit 23	MIPITX Sleep – When set, MIPITX will send out ULPM sequence and goes to sleep	0 = MIPITX exits from sleep 1 = MIPITX send out ULPM and enter sleep state
MRXEN Bit 22	MIPIRX Mode Enable – It will enable the MIPIRX	0 = MIPIRX Enable 1 = Reserved
MRXLS Bit 21-20	MIPIRX Lane Select – Selects number of lane to be used for MIPIRX	0 = 1 lane 1 = 2 lanes 2 = 3 lanes 3 = 4 lanes (default)

Name	Description	Setting
MRXVB Bit 19	MIPIRX Video Bypass – Indicates whether video packets into MIPIRX is bypassing the RAM and goes directly towards MIPITX	0 = No bypass (video packets goes into RAM) 1 = Bypass (video packets bypass RAM)
MRXECC Bit 18	MIPIRX ECC Enable – Indicates whether ECC check is enabled in MIPIRX	0 = ECC Disabled 1 = ECC Enabled
MRXCRC Bit 17	MIPIRX CRC Enable – Indicates whether CRC check is enabled in MIPIRX	0 = CRC Disabled 1 = CRC Enabled
MRXEOT Bit 16	MIPIRX EOT Enable – Indicates whether EOT check is enabled in MIPIRX	0 = Disabled 1 = Enabled
MRXEE Bit 15	MIPIRX Error Enable – Indicates whether error check is enabled in MIPIRX	0 = Disabled 1 = Enabled
MRXCE Bit 14	MIPIRX Clear Error – Write 1, follows by a zero to clear the error in MIPIRX	0 = No action 1 = Clear MIPIRX Error (need to write 0 after writing 1)
Reserved Bit 13-12	Reserved	
Reserved Bit 11-10	Reserved	
Reserved Bit 9-8	Reserved	
CLKOUT_SEL Bit 7-4	Clock Out Select – Select which internal clocks is routed out to clkout_pin for debugging purpose	
DS_PA17-16 Bit 3-0	Drive Strength Control for GPIO Port A, index 17 to 16	

SCM MIPIRX PHY Control Register

Offset Address

SCM_MRXPHY

SCM MIPIRX PHY Control Register

0x001C

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE								
RESET								
BIT	23	22	21	20	19	18	17	16
NAME				ATCI		ATCV		
TYPE				RW	RW	RW	RW	RW
RESET				0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	TMEB	GFE	STE	HSRXTI				
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	1	0	1	0	0
BIT	7	6	5	4	3	2	1	0
NAME	THFT		TLFT		LPTXDS		HSRXRS	
TYPE	RW		RW		RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	1

Table 5-7: SCM MIPIRX PHY Control Register Description

Name	Description	Setting
ATCI Bit 20-19	ATCI - This selects bias current output to test pad	
ATCV Bit 18-16	ATCV - This selects voltage reference output to test pad	
TMEB Bit 15	Termination Enable - This enables the termination in MIPIRX PHY	1 = Disable 0 = Enable (Active low)
GFE Bit 14	Glitch Filter Enable - This enables the glitch filter in MIPIRX PHY	0 = Disable 1 = Enable
STE Bit 13	Schmitt Trigger Enable - This enables Schmitt trigger at the input in MIPIRX PHY	0 = Disable 1 = Enable
HSRXTI Bit 12-8	HS Receiver Termination Impedance – Selects the termination impedance for HS receiver	
THFT Bit 7-6	LPRX Input High Threshold Tuning – Selects the high threshold of LPRX input	
TLFT Bit 5-4	LPRX Input Low Threshold Tuning – Selects the low threshold of LPRX input	
LPTXDS Bit 3-2	LPTX Drive Strength Select - This selects the drive strength of LPTX	
HSRXRS Bit 1-0	HS RX Drive Strength Select - This selects the drive strength of HS RX	

SCM Analog Control 1 Register

Offset Address

SCM_ANACTRL1

SCM Analog Control 1 Register

0x0020

BIT	31	30	29	28	27	26	25	24
NAME	TE2	TE1	BGIEXT	BGEN	BGHZ	TC		BUFE
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	1	0	1	0	1
BIT	23	22	21	20	19	18	17	16
NAME	VREFTRIM					VREFHZ	CREFEN	CREFIXT
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	1	0	0	1	0	0	1	0
BIT	15	14	13	12	11	10	9	8
NAME	ITUNETX		ITUNERX		ITUNECX		CPEN	CPUNR
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	1	0	1	0	1	1	0
BIT	7	6	5	4	3	2	1	0
NAME	CREFTRIM				CPREG			CPDP
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	1	1	1	1	1	0	1

Table 5-8: SCM Analog Control 1 Register Description

Name	Description	Setting
TSEL2 Bit 37-35	TEST Internal Signal Select – This selects the internal signal to analog_test2_pad for debugging in test mode.	000 CPSOFTSTART_T2 001 ENABLE_T2 010 CLK1_VCI_T2 011 VIN_T2 100 IREF_TEST 101 IBIAS_EXT 110 VBE 111 VBER
TSEL1 Bit 34-32	TEST Internal Signal Select – This selects the internal signal to analog_test1_pad for debugging in test mode.	000 VINP_BG 001 VINN_BG 010 VREF 011 VREF_CREF 100 CREF_EXT 101 VTAP_T1 110 CMPOUT_T1 111 SSCLK1_VCI_T1
TE2 Bit 31	Test Enable 2 - This enables the test output at analog_test2_pad	0 = Disable 1 = Enable
TE1 Bit 30	Test Enable 1 - This enables the test output at analog_test1_pad	0 = Disable 1 = Enable
BGIEXT Bit 29	Bandgap External Input Enable - Enable the use of external reference current	0 = Disable 1 = Enable
BGEN Bit 28	Bandgap Enable - This enables internal bandgap for current reference generation circuit and Chargepump	0 = Disable 1 = Enable

Name	Description	Setting
BGHZ Bit 27	Bandgap Output Hi-Z Enable - This enables high-impedance of bandgap output. External bandgap reference can be fed in	0 = Disable 1 = Enable
TC Bit 26-25	Temperature Coefficient - This selects the temperature coefficient of BGOUT	0 = TC=-0.1%; 1 = TC=-0.05%; 2 = TC=0; 3 = TC=+0.05%
BUFE Bit 24	Bandgap Buffer Enable - This enables the bandgap buffer	0 = Disable 1 = Enable
VREFTRIM Bit 23-19	VREF Trim Select – This trims the reference voltage	0x00 = 1.2246 0x01 = 1.2330 0x02 = 1.2415 0x03 = 1.2502 0x04 = 1.2590 0x05 = 1.2679 0x06 = 1.2770 0x07 = 1.2862 0x08 = 1.2955 0x09 = 1.3049 0x0A = 1.3145 0x0B = 1.3242 0x0C = 1.3341 0x0D = 1.3441 0x0E = 1.3543 0x0F = 1.3646 0x10 = 1.3751 0x11 = 1.3858 0x12 = 1.4002 0x13 = 1.4076 0x14 = 1.4187 0x15 = 1.4301 0x16 = 1.4416 0x17 = 1.4533 0x18 = 1.4652 0x19 = 1.4773 0x1A = 1.4896 0x1B = 1.5021 0x1C = 1.5148 0x1D = 1.5278 0x1E = 1.5409 0x1F = 1.5543
VREFHZ Bit 18	VREF Output Hi-Z Enable - This enables high-impedance of VREF output.	0 = Disable 1 = Enable
CREFEN Bit 17	Current Reference Enable - This enables the current reference generation for MIPIRX, MIPITX and Chargepump	0 = Disable 1 = Enable
CREFIXT Bit 16	Current Reference Output Hi-Z Enable - This enables high-impedance of current reference output to MIPIRX, MIPITX and Chargepump. External current reference can be fed in via analog_test_pad in testmode	0 = Disable 1 = Enable
ITUNETX Bit 15-14	Current Output Reference Tuning for MIPITX - This tunes the output reference current for MIPITX	0 = 2.5uA 1 = 5uA 2 = 7.5uA 3 = 10uA
ITUNERX	Current Output Reference Tuning for MIPIRX	0 = 2.5uA

Name	Description	Setting
Bit 13-12	- This tunes the output reference current for MIPIRX	1 = 5uA 2 = 7.5uA 3 = 10uA
ITUNECP Bit 11-10	Current Output Reference Tuning for Chargepump - This tunes the output reference current for MIPIRX	0 = 0.5uA 1 = 1uA 2 = 1.5uA 3 = 2uA
CPEN Bit 9	Charge Pump Enable	0 = Disable 1 = Enable
CPUNR Bit 8	Charge Pump Unregulated Mode - This enables the unregulated mode of charge pump	0 = Disable 1 = Enable
CREFTRIM Bit 7-4	VREF Trim Select – This trims the reference current	0x0 = 4.13mA 0x1 = 4.25mA 0x2 = 4.38mA 0x3 = 4.50mA 0x4 = 4.63mA 0x5 = 4.75mA 0x6 = 4.87mA 0x7 = 5.00mA 0x8 = 5.12mA 0x9 = 5.25mA 0xA = 5.37mA 0xB = 5.49mA 0xC = 5.62mA 0xD = 5.74mA 0xE = 5.87mA 0xF = 5.99mA
CPREG Bit 3-1	CP Regulated Mode Setting - This set the CP output voltage in regulated mode	0 = 2.94V 1 = 3.00V 2 = 3.06V 3 = 3.12V 4 = 3.18V 5 = 3.24V 6 = 3.30V (POR) 7 = 3.36V
CPDP Bit 0	CP Dual Phase Mode Enable – When enabled, C11P, C11N & C12P, C12N flying caps pads are required	0 = Disable 1 = Enable

SCM Analog Control 2 Register

Offset Address

SCM_ANACTRL2

SCM Analog Control 2 Register

0x0024

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE								
RESET								
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE								
RESET								
BIT	15	14	13	12	11	10	9	8
NAME			CPSS	CPSAM		CPPER		
TYPE			RW	RW		RW		
RESET			1	1	0	0	1	1
BIT	7	6	5	4	3	2	1	0
NAME	CPNOV		TSEL1			TSEL2		
TYPE	RW		RW			RW		
RESET	0	0	0	0	0	0	0	0

Table 5-9: SCM Analog Control 1 Register Description

Name	Description	Setting
Reserved Bit 31-14	Reserved	
CPSS Bit 13	Charge Pump Softstart enable - This enables the charge pump softstart.	0 = Disable 1 = Enable
CPSAM Bit 12-11	Charge Pump Sampling Frequency - This selects the charge pump sampling frequency	0 = 1xCPCLK 1 = 2xCPCLK 2 = 4xCPCLK 3 = 8xCPCLK
CPPER Bit 10-8	Charge Pump Clock Frequency – Sets the clock frequency of CPCLK.	0 = 24 OSC clk period 1 = 32 OSC clk period 2 = 64 OSC clk period 3 = 96 OSC clk period 4 = 128 OSC clk period 5 = 160 OSC clk period 6 = 240 OSC clk period 7 = 320 OSC clk period
CPNOV Bit 7-6	Charge Pump Clock Non-overlapping interval – This selects the non-overlapping interval of the CPCLK	0 = 1 OSC clk period 1 = 2 OSC clk period 2 = 3 OSC clk period 3 = 4 OSC clk period
TSEL1 Bit 5-3	Test Select for analog_test1_pad	
TSEL2 Bit 2-0	Test Select for analog_test1_pad	

SCM Scratch Register

Offset Address

SCM_SCRATCH

SCM Scratch Register

0x0028

BIT	31	30	29	28	27	26	25	24
NAME	SCRATCH0[31:24]							
TYPE	RW							
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	SCRATCH0[23:16]							
TYPE	RW							
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	SCRATCH0[15:8]							
TYPE	RW							
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	SCRATCH0[7:0]							
TYPE	RW							
RESET	0	0	0	0	0	0	0	0

Table 5-10: SCM Scratch 0 Register Description

Name	Description	Setting
SCRATCH Bit 31-0	Scratch 0 Register – User can use this register to store any value	NA

SCM GAP1 Register

Offset Address

SCM_GAP1

SCM GAP1 Register

0x002C

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE								
RESET								
BIT	23	22	21	20	19	18	17	16
NAME						START1[11:8]		
TYPE						RW		
RESET					0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME						START1[7:0]		
TYPE						RW		
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME						WIDTH1		
TYPE						RW		
RESET	0	0	0	0	0	0	0	0

Table 5-11: SCM GAP1 Register Description

Name	Description	Setting
Reserved Bit 31-20	Reserved	
START1 Bit 19-8	Start of 1st Gap - Start pixel (horizontal) position for 1 st gap	0 = pixel 0 1 = pixel 1 ...
WIDTH1 Bit 7-0	Width of 1st Gap – The width of 1 st gap in terms of number of pixels	0 = No gap 1 = 1 pixel gap ...

SCM GAP2 Register

Offset Address

SCM_GAP2

SCM GAP2 Register

0x0030

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE								
RESET								
BIT	23	22	21	20	19	18	17	16
NAME						START2[11:8]		
TYPE						RW		
RESET					0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME						START2[7:0]		
TYPE						RW		
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME						WIDTH2		
TYPE						RW		
RESET	0	0	0	0	0	0	0	0

Table 5-12: SCM GAP2 Register Description

Name	Description	Setting
Reserved Bit 31-20	Reserved	
START2 Bit 19-8	Start of 2nd Gap - Start pixel (horizontal) position for 1 st gap	0 = pixel 0 1 = pixel 1 ...
WIDTH2 Bit 7-0	Width of 2nd Gap – The width of 1 st gap in terms of number of pixels	0 = No gap 1 = 1 pixel gap ...

6 MIPI DSI RX (MIPIRX)

The MIPI RX IP supports MIPI DSI interface. It receives MIPI signals and converts them to SSL Video Interface output (VIF) for MIPI DSI Video Packets and SSL Command Interface (SCBIF) output for MIPI command packets.

Features

- High Speed transmission from 1 data lane to 4 data lanes
- Support up to 1.5Gbps per lane
- Support Video transfer in High Speed mode
- Support 16, 18 and 24 bit per pixel video transfer
- Support SSL 32-bit SCB Interface
- Support SSL double pixel VIF outputs
- Support High Speed, Low Power and Ultra Low Power modes in forward link and Low Power mode in reverse link.
- Support of MIPI standard DSI(v1.01), DCS(v1.02), D-PHY (v1.1)

References

MIPI DSI, DCS, D-PHY Standard

Definitions

HS High Speed

LP Low Power

MCU Proprietary parallel interface between the MIPI RX IP and display display driver, which is for display driver register and memory access

RGB MIPI Alliance Standard for Display Pixel Interface v2.0 (DPI-2)

VC Virtual Channel

Architecture

Overview

Below is the interface diagram for the MIPI 4-lane RX IP.

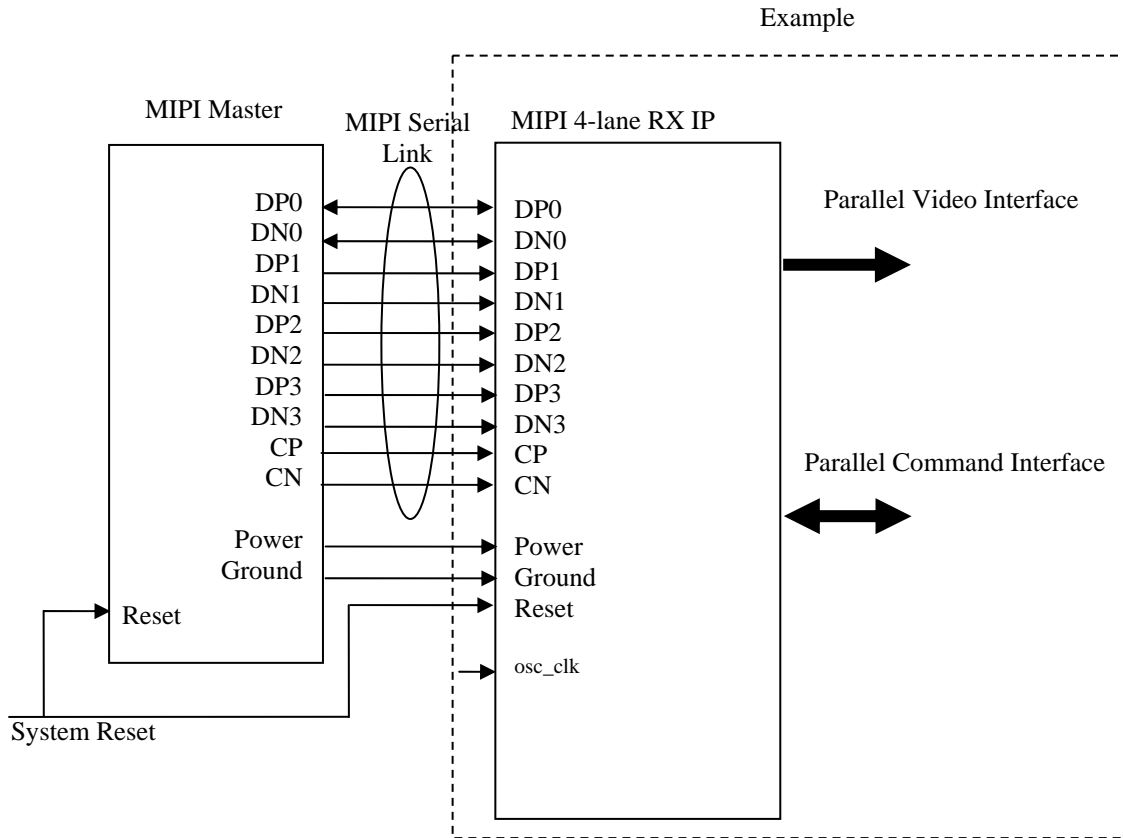


Figure 6-1: MIPI RX IP interface Diagram

Detailed Description

The block diagram for the modules inside the MIPI RX IP is given below.

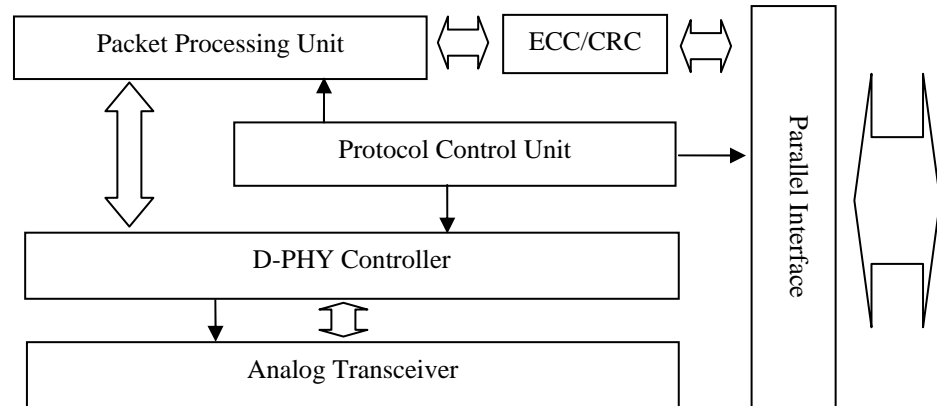


Figure 6-2: MIPI RX IP Block Diagram

D-PHY controller

The D-PHY controller is in charge of the communication with the analog transceiver. During reception, it detects the start and stop of the received data stream. It receives data from analog receiver in serial format and passes the data in parallel format to the PPU for further processing. At the same time, it is also performing the handshaking process, such as, bus turn around and switching between different modes (HS to LP, vice versa). During transmission, it receives data from PPU and drives the analog transmitter to transmit the data back to MIPI master.

Parallel Interface

The parallel interface is in charge of the communication between MIPI RX IP and the display driver. It generates signals for 2 kinds of interfaces, e.g. the RGB interface for dumb display data transmission, the MCU interface for display driver's register access. The control signals for RGB and MCU interfaces are separate with each interface has its own control signals. The details are described in 0.

The parallel interface module uses the packet type of the received packets to decide which interface to write data out. If the packet is video packet, the video interface will be used. If the packet is DCS packet or generic packet, command interface will be used.

Protocol Control Unit (PCU)

The PCU is in charge of the handling of incoming and outgoing data stream. It has a state machine to decide how to disassemble the received packet and write the correct data to the display driver memory and registers. It will also handle read request and send back desired data to the MIPI master.

Packet Processing Unit (PPU)

The PPU is in charge of packet assembly and disassembly. During transmission, it will form the packet according to the instruction from the PCU. During reception, it will extract necessary information from the packet and pass to the PCU.

Error Correction Code/ Cyclic Redundancy Check (ECC/CRC)

During reception, the ECC/CRC module will check the correctness of the ECC and CRC field of the incoming stream.

If there is 1 bit of error in the data and ECC field, this error will be corrected by the ECC module. If there are more than 1 bit of error in the data and ECC field, the ECC module will detect the error and report it. If there is at least 1 bit of error in the data and CRC field, the CRC module will detect the error and report it.

During transmission, ECC/CRC module will calculate the ECC and CRC value for every outgoing packet.

Analog Transceiver

The Analog Transceiver receives the MIPI link signals in HS mode and packs them into 4-bit parallel data before sending it to the DPHY controller. There are 4 HS receiver blocks that handle the 4 data lane traffic. During LP mode, only 1 receiver block is receiving the LP signals and the single ended signals are sent to the DPHY controller without packing.

The LP transmitter block will return LP data when there is a reverse link request from the master.

The analog transceiver also detects contention and reports it to the DPHY controller.

Programming Model

Table 4-1: MIPI RX IP Register Summary

Offset	Name	Mnemonic	Reset Value
0x0004	Configuration Control Register	CCR	0x00000088
0x0008	Delay Configuration Register	DCR	0x01200245
0x000C	HS RX Timer Register	HRTR	0x00100000
0x0010	LP TX Timer Register	LTTR	0x00100000
0x0014	SOT Count Register	SCR	0x2010FFFF
0x0018	Phy Error Register	PER	0x00000000
0x001C	Analog Control Register 1	ACR1	0x88888888
0x0020	Analog Control Register 2	ACR2	0x00000000
0x0024	Initialization Register	INIR	0x000009C4
0x0028	Power Cut Register	PCR	0x00000000
0x002C	DSI Error Register	DER	0x00000000
0x0030	Error Count Register	ECR	0x00000000

1.2 Register Description

Configuration Control Register

CCR

Configuration Control Register

0x0004

Bit 7-0	TEE	TEP	0	0	CO	END	0	POR
Bit 15-8	ERM[7:0]							1000_1000
Bit 23-16	ERM[15:8]							0000_0000
Bit 31-24	0	EIC[4:0]				TM[1:0]		0000_0000

Table 6-1: Configuration Control Register Description

Bit	Description	Setting
2	ENDian - This bit specifies the endian-ness of the data received over the serial link. During video mode transmission, this bit must be set to 0 so as to follow the MIPI DSI specification	0 – Least significant byte sent first 1 – Most significant byte sent first
3	Color Order – This bit specifies the order of the color component in the received pixel. During video mode transmission, this bit must be set to 1 so as to follow the MIPI DSI specification.	0 – RGB. R is in the higher portion of the pixel. 1 – BGR. B is in the higher portion of the pixel.
5	Select Nibble B input – This bit bypasses the automatic selection of the nibble data stream A, B and C and permanently uses stream B for data decoding.	0 – Automatic selection of A or B or C 1 – Permanently select B input
6	Tearing Effect Polarity – This bit controls whether to detect the rising or falling edge of the TE input.	0 – Rising edge detection 1 – Falling edge detection
7	Tearing Effect Enable – This bit controls whether to enable MIPI IP to detect the TE input and send back the TE trigger packet to the MIPI host at the second BTA when 2 consecutive BTAs are received by the MIPI IP.	0 – Disable 1 – Enable
15:8	ERror Emask[7:0] – These bit controls whether to enable the detection of MIPI DSI error. The bit position correspond to the Error Report defined in the DSI specification.	0 – Disable 1 – Enable
23:16	ERror Emask[15:8]	0 – Disable 1 – Enable
25:24	Test Mode - These bits control whether to inject ECC/CRC error for the outgoing streams. This is for testing only. They should be set to 00 during normal mode.	00 – Normal mode 01 – Inject CRC error 10 – Inject 1 bit ECC error 11 – Inject 2 bit ECC error
30:26	Error Injection Control – These bits control the position of the error being injected for testing. It is only applicable for TM=01. This is for testing only.	
31	<i>Reserved</i>	

Delay Configuration Register

DCR

Delay Configuration Register

0x0008

Bit 7-0	TGO[3:0]		TGET[3:0]		POR
Bit 15-8	HST[7:0]				0100_0101
Bit 23-16	TAT[7:0]				0000_0010
Bit 31-24	0	ATP	TDM	ATUN	EOT[3:0] 0010_0000

Table 6-2: Delay Configuration Register Description

Bit	Description	Setting
7:0	TA GET Delay – These bits specifies the number of T_{LFX} for TA get delay period T_{TA-GET} .	
15:8	TA GO Delay – These bits specifies the number of T_{LFX} for TA go delay period T_{TA-GO} .	
23:16	Turnaround Ack Timer – These bits specify the turnaround acknowledge timer timeout value. <code>sys_clk</code> is used to increment an internal timer.	
7:0	HS Settle Time – These bits specifies the duration of $T_{HS-SETTLE}$, when the data lane switch from LP to HS mode. The period is for the MIPI RX IP not to sample the incoming HS data, as the line is in transition stage. The duration is counted using the HS nibble clock. The HS nibble clock frequency is one quarter of the data rate on the data lane. For example, if the serial link is running at 200Mbps, the nibble clock is 50MHz.	
3:0	End Of Transmission – These bits specify the number of bits in the $T_{HS-TRAIL}$ period that are used for DPHY EOT detection. Please see MIPI DPHY spec for the details.	The minimum value should be 1. 0 is not allowed in this field.
4	ATUN – A-Phy lane tuning enable This bit enables the automatic tuning of the data and clock lane delay settings. The tuning circuit will check for the MIPI packet errors and adjust the 3 bit delays for each individual lane of the A-Phy.	0 = Disable 1 = Enable
5	TDM – Tuning data masked This bit controls the masking of the received data from the MIPI RX, to be sent to the MIPI TX DSI for processing.	0 = Do not mask data to TX 1 = Mask data to TX
6	ATP – A-Phy tuning Passed Once ATUN is enabled, the internal tuning circuit will detect for any error in the MIPI packet and if a packet is received successfully, ATP will be set to 1.	0 = Tuning Failed 1 = Tuning Passed
7	<i>Reserved</i>	

HS RX Timer Register

HRTR HS RX Timer Register 0x000C

									POR
Bit 7-0	HRT[7:0]								0000_0000
Bit 15-8	HRT[15:8]								0000_0000
Bit 23-16	HRT[23:16]								0001_0000
Bit 31-24	HRT[31:24]								0000_0000

Table 6-3: HS RX Timer Register Description

Parameter	Bit	Description	Setting
1	7:0	HS RX Timer[7:0] – These bits specify the HS RX timer timeout value. Sys_clk is used to increment an internal timer.	
2	7:0	HS RX Timer[15:8]	
3	7:0	HS RX Timer[23:16]	
4	7:0	HS RX Timer[31:24]	

LP TX Timer Register

LTTR

LP TX Timer Register

0x0010

									POR
Bit 7-0	LTT[7:0]								0000_0000
Bit 15-8	LTT[15:8]								0000_0000
Bit 23-16	LTT[23:16]								0001_0000
Bit 31-24	LTT[31:24]								0000_0000

Table 6-4: LP TX Timer Register Description

Bit	Description	Setting
31:0	<p>LP TX Timer[31:0] – These bits specify the LP TX timer timeout value. <code>sys_clk</code> is used to increment an internal timer.</p> <p>The timer starts when the MIPI RX IP enters LP transmit mode. When the MIPI RX IP exits from LP transmit mode, the timer will be reset. If the timer expires before exiting from LP transmit mode, the MIPI RX IP will signal an error and switch to LP receive mode. The DPHY will wait until a stop state (LP11) comes before accept any incoming data.</p>	

SOT Count Register

SCR

SOT Count Register

0x0014

									POR
Bit 7-0	SC[7:0]								1111_1111
Bit 15-8	SC[15:8]								1111_1111
Bit 23-16	TEPW[7:0]								0001_0000
Bit 31-24	CEXT[7:0]								0010_0000

Table 6-5: SOT Count Register Description

Bit	Description	Setting
15:0	<p>SOT Count[15:0]– These bits determines when the MIPI RX IP will stop searching for the SoT sequence defined in MIPI D-PHY.</p> <p>The searching starts after the HS Settle Time has been passed. Once the searching starts, a counter will start counting from zero. The searching will stop, if a SoT sequence has been identified or the counter reaches the value specified in this register or the data lane enters LP mode. The counter uses nibble_clk for counting.</p>	
23:16	<p>Tearing Effect Pulse Width– These bits determine how the MIPI RX IP qualifies the pulse width of the TE input signal. A valid TE signal is considered when the TE input signal is greater than the TEPW count. The TE pulse is counted using the sys_clk.</p>	
31:24	<p>Clock EXTender – These bits extend the clocks after the end of a request transaction. The counter will be reset once another new request is received before current counter expire.</p>	<p>0 = Extends by 1 clocks. 1 = Extends by 1 clocks. 2 = Extends by 2 clocks. 255 = Clock is always on.</p>

Phy Error Register

PER

Phy Error Register

0x0018

									POR
Bit 7-0	SSE_3	SSE_2	SSE_1	SSE_0	SE_3	SE_2	SE_1	SE_0	0000_0000
Bit 15-8	EME_3	EME_2	EME_1	EME_0	ESE_3	ESE_2	ESE_1	ESE_0	0000_0000
Bit 23-16	0	0	0	0	FCE_3	FCE_2	FCE_1	FCE_0	0000_0000
Bit 31-24	0	0	0	PV_4	PV_3	PV_2	PV_1	PV_0	0000_0000

Table 6-6: Phy Error Register Description

Bit	Description	Setting
0	SOT Error 0 – This bit reflects the SoT Error detected by the MIPI RX IP at the lane 0. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
1	SOT Error 1 – This bit reflects the SoT Error detected by the MIPI RX IP at the lane 1. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
2	SOT Error 2 – This bit reflects the SoT Error detected by the MIPI RX IP at the lane 2. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
3	SOT Error 3 – This bit reflects the SoT Error detected by the MIPI RX IP at the lane 3. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
4	SOT Sync Error 0 – This bit reflects the SoT Sync Error detected by the MIPI RX IP at the lane 0. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
5	SOT Sync Error 1 – This bit reflects the SoT Sync Error detected by the MIPI RX IP at the lane 1. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
6	SOT Sync Error 2 – This bit reflects the SoT Sync Error detected by the MIPI RX IP at the lane 2. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
7	SOT Sync Error 3 – This bit reflects the SoT Sync Error detected by the MIPI RX IP at the lane 3. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
8	EOT Sync Error 0 – This bit reflects the EoT Sync Error detected by the MIPI RX IP at the lane 0. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
9	EOT Sync Error 1 – This bit reflects the EoT Sync Error detected by the MIPI RX IP at the lane 1. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
10	EOT Sync Error 2 – This bit reflects the EoT Sync Error detected by the MIPI RX IP at the lane 2. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
11	EOT Sync Error 3 – This bit reflects the EoT Sync Error detected by the MIPI RX IP at the lane 3. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
12	Escape Mode Error 0 – This bit reflects the Escape Mode Entry Command Error detected by the MIPI RX IP at the lane 0. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
13	Escape Mode Error 1 – This bit reflects the Escape Mode Entry Command Error detected by the MIPI RX IP at the lane 1. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred

14	Escape Mode Error 2 – This bit reflects the Escape Mode Entry Command Error detected by the MIPI RX IP at the lane 2. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
15	Escape Mode Error 3 – This bit reflects the Escape Mode Entry Command Error detected by the MIPI RX IP at the lane 3. Please see MIPI DSI spec for the details.	0 – Not error 1 – Error has occurred
16	False Control Error 0 – This bit reflects the False Control Error detected by the MIPI RX IP at the lane 0.	0 – Not error 1 – Error has occurred
17	False Control Error 1 – This bit reflects the False Control Error detected by the MIPI RX IP at the lane 1.	0 – Not error 1 – Error has occurred
18	False Control Error 2 – This bit reflects the False Control Error detected by the MIPI RX IP at the lane 2.	0 – Not error 1 – Error has occurred
19	False Control Error 3 – This bit reflects the False Control Error detected by the MIPI RX IP at the lane 3.	0 – Not error 1 – Error has occurred
23:20	<i>Reserved</i>	
24	Protocol Violation Error Type 0 – This bit reflects EOT packet is not detected by MIPI RX IP at the end of the HS transmission.	0 – Not error 1 – Error has occurred
25	Protocol Violation Error Type 1 – This bit reflects BTA sequence is not detected by MIPI RX IP after receiving the read packet.	0 – Not error 1 – Error has occurred
26	Protocol Violation Error Type 2 – This bit reflects BTA timer out error.	0 – Not error 1 – Error has occurred
27	Protocol Violation Error Type 3 – This bit reflects video timing mismatched in Non-burst mode has error.	0 – Not error 1 – Error has occurred
28	Protocol Violation Error Type 4 – This bit reflects local MIPI bus transactor has encountered error.	0 – Not error 1 – Error has occurred
31:29	<i>Reserved</i>	

Analog Control Register 1

ACR1

Analog Control Register 1

0x001C

									POR
Bit 7-0		D0_DLY[3:0]				D0_CDLY[3:0]			1000_1000
Bit 15-8		D1_DLY[3:0]				D1_CDLY[3:0]			1000_1000
Bit 23-16		D2_DLY[3:0]				D2_CDLY[3:0]			1000_1000
Bit 31-24		D3_DLY[3:0]				D3_CDLY[3:0]			1000_1000

Table 6-7: Analog Control Register 1 Description

Bit	Description	Setting
3:0	Data lane 0 Sample CDeLaY – These bits control the tap delay for Data lane 0 de-serializer sample clock.	
7:4	Data lane 0 Sample DeLaY – These bits control the tap delay for Data lane 0 de-serializer data.	
11:8	Data lane 1 Sample CDeLaY – These bits control the tap delay for Data lane 1 de-serializer sample clock.	
15:12	Data lane 1 Sample DeLaY – These bits control the tap delay for Data lane 1 de-serializer data.	
19:16	Data lane 2 Sample CDeLaY – These bits control the tap delay for Data lane 2 de-serializer sample clock.	
23:20	Data lane 2 Sample DeLaY – These bits control the tap delay for Data lane 2 de-serializer data.	
27:24	Data lane 3 Sample CDeLaY – These bits control the tap delay for Data lane 2 de-serializer sample clock.	
31:28	Data lane 3 Sample DeLaY – These bits control the tap delay for Data lane 2 de-serializer data.	

Analog Control Register 2

ACR2

Analog Control Register 2

0x0020

									POR
Bit 7-0	0	0	0	0	0	0			0000_0000
Bit 15-8	0	0	0	0	0	0	0	0	0000_0000
Bit 23-16	0	0	0	0	0	0	0	0	0000_0000
Bit 31-24	0	0	0	0	0	0	0	0	0000_0000

Table 6-8: Analog Control Register 2 Description

Bit	Description	Setting
1:0	Select SoT Edge – These bits control the detection of SOT using positive or negative edge clock or both.	SSE[1:0]

Initialization Register

INIR

Initialization Register

0x024

									POR
Bit 7-0	INIT[7:0]								1100_0100
Bit 15-8	INIT[15:8]								0000_1001
Bit 23-16	INIT[23:16]								0000_0000
Bit 31-24	INIT[31:24]								0000_0000

Table 6-9: Initialization Register Description

Bit	Description	Setting
7:0	<i>Init</i> [7:0]	
15:8	<i>Init</i> [15:8]	
23:16	<i>Init</i> [23:16]	
31:24	<i>Init</i> [31:24]	

Power Cut Register

PCR

Power Cut Register

0x028

									POR
Bit 7-0	0	0	0	0	0	0	0	PWC	0000_0000
Bit 15-8	0	0	0	0	0	0	0	0	
Bit 23-16	0	0	0	0	0	0	0	0	
Bit 31-24	0	0	0	0	0	0	0	0	

Table 6-10: Power Cut Register Description

Bit	Description	Setting
0	PoWer Cut – This bit will enable power cut to the whole chip and only global reset can restore the power supply to the chip.	

DSI Error Register

DER

DSI Error Register

0x02C

									POR
Bit 7-0	CE	FCE	HRTE	LTSE	EME	ESE	SSE	SE	0000_0000
Bit 15-8	DPV	LTTE	ITL	VCE	DTE	CRC	ECC2	ECC1	
Bit 23-16	0	0	0	0	0	0	0	0	
Bit 31-24	0	0	0	0	0	0	0	0	

Table 6-11: DSI Error Register Description

Bit	Description	Setting
0	<p>SE - SoT Error</p> <p>This bit reflects the SoT Error detected by the MIPI RX DSI. Refer to PER register for more information.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
1	<p>SSE - SoT Sync Error</p> <p>This bit reflects the SoT Sync Error detected by the MIPI RX DSI. Refer to PER register for more information.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
2	<p>ESE - EoT Sync Error</p> <p>This bit reflects the EoT Sync Error detected by the MIPI RX DSI. Refer to PER register for more information.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
3	<p>EME - Escape Mode Error</p> <p>This bit reflects the Escape Mode Entry Command Error detected by the MIPI RX DSI. Refer to PER register for more information.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
4	<p>LTSE - Low power Transmit Sync Error</p> <p>This bit reflects the Low Power Transmit Sync Error detected by the MIPI RX DSI.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
5	<p>HRTE - High speed Receive Timeout Error</p> <p>This bit reflects the High Speed Receive Timeout Error detected by the MIPI RX DSI.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>

6	<p>FCE - False Control Error</p> <p>This bit reflects the False Control Error detected by the MIPI RX DSI. Refer to PER register for more information.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
7	<p>CE - Contention Error</p> <p>This bit reflects the contention is detected by the MIPI RX DSI.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
8	<p>ECC1 - ECC Error 1</p> <p>This bit reflects the ECC Error, single bit, detected by the MIPI RX DSI.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
9	<p>ECC2 - ECC Error 2</p> <p>This bit reflects the ECC Error, multiple bits, detected by the MIPI RX DSI.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
10	<p>CRC - CRC Error</p> <p>This bit reflects the Checksum Error detected by the MIPI RX DSI.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
11	<p>DTE - Data Type Error</p> <p>This bit reflects the DSI Data Type Not Recognized detected by the MIPI RX DSI.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
12	<p>VCE - VC ID Error</p> <p>This bit reflects the Invalid DSI VC ID detected by the MIPI RX DSI.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
13	<p>ITL - Invalid Transmission Length</p> <p>This bit reflects the Invalid Transmission Length error detected by the MIPI RX DSI.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
14	<p>LTTE - Low Power Transmit Timeout Error</p> <p>This bit reflects the Low Power Transmit Timeout Error detected by the MIPI RX DSI.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>
15	<p>DPV - DSI Protocol Violation</p> <p>This bit reflects the DSI Protocol Violation error detected by the MIPI RX DSI.</p> <p>Please see MIPI DSI spec for the details.</p>	<p>0 = Not error 1 = Error has occurred</p>

Error Count Register

DER

DSI Error Register

0x030

									POR
Bit 7-0	ERR_COUNT[7:0]								0000_0000
Bit 15-8	ERR_COUNT[15:8]								0000_0000
Bit 23-16	0	0	0	0	0	0	0	0	
Bit 31-24	0	0	0	0	0	0	0	0	

Table 6-12: Error Count Register Description

Bit	Description	Setting
15:0	<p>ERR_COUNT – Error counter for ECC and CRC errors.</p> <p>These bits provide the accumulation of ECC and CRC errors collected by MIPI RX. When Bit[15] is set, it will remains set.</p>	

Operating Modes

The MIPI RX IP internal state machine controls the receiving and sending of the data packet over the serial link. It is triggered by receiving a packet defined in MIPI DSI specification or a request to read back register.

During reception, the state machine gets raw data packets from D-PHY. It disassembles the data packets and extracts all the information. If the packet contains video data, it will write the data to the display driver using video signals. If the packet contains register programming, it will write the content into the appropriate register in the display driver using MCU interface. If the packet contains an event, it will perform according to the current state and the event.

The MIPI RX IP supports all the packet type defined in the MIPI DSI specification. But, whether to transfers the packet to the display driver or not, it will looks at the packet type. The following sections describe how the MIPI RX IP reacts with each DSI packet.

The parallel interface between MIPI RX IP and display driver supports 2 types of interface, RGB(Video) and MCU(Command) interface.

End of Transmission (EOT)

An EOT packet has been defined in MIPI DSI to indicate the end of a HS transmission.

EOT (0x08)

When this packet is received in HS mode, MIPI RX IP will stop processing any further received data. MIPI RX IP will wait until the data lane goes into stop state (LP11). Afterwards, MIPI RX IP will process the new data sent in either HS or LP mode.

When this packet is received in LP mode, MIPI RX IP will ignore the packet.

If an MIPI master does not implement the EOT packet defined in MIPI DSI, the MIPI RX IP will not get such packet at the end of the HS transmission. As a result, the MIPI RX IP will see the EoT sequence defined in MIPI DPHY. In this case, the MIPI RX IP will still be able to end the HS transmission as defined in the MIPI DPHY specification. However, the last few bytes in the T_{EOT} period of the HS transmission might be received as an unknown packet and affect the error status reported to the MIPI master. This is a known issue for MIPI DSI. Hence, we recommend using MIPI master with EOT packet support, so that the line status is more accurately reported to the MIPI master.

The VC ID of the EOT packet should be 0x0.

Contention Detection and Timer

Two timers have been defined in MIPI RX IP to resolve the potential contention issue on the bus. The two timers are the HS RX timer and LP TX timer. Please see the register description for the detailed usage.

Whenever the receiver sees the two data lines are in LP 11 state, it will reset MIPI RX IP and enter the default mode, which is RX low power idle mode. Whenever the receiver sees a contention being detected, it will reset MIPI RX IP and enter the default mode, which is LP RX idle mode.

Error Report

The MIPI RX IP implements the error report scheme as described in the MIPI DSI specification. It will accumulate the error status since last report to the MIPI master. On BTA after a read, the MIPI RX IP will return the error status since the last report. The protocol violation error is stored in **ESR1**. Low level error for each lane is stored in the **ESR1** and **ESR2**.

On top of that, the MIPI RX IP has also implemented an error accumulation output. It counts how many ECC and CRC error has happened since the last read from these registers. It is cleared by the display driver. After which it starts to accumulate the number of errors again, until the next read.

D-PHY operation

D-PHY controls the operation of the analog transceiver. It determines whether the serial link is in high speed or low power mode and whether it is in transmit or receive mode.

The MIPI RX IP can support both continuous and non-continuous clock behavior on the clock lane. During reception, when switching from HS to LP mode, the data lane must enter the low power mode first, and the clock lane can enter LP mode afterwards. The minimum timing defined in MIPI DPHY specification needs to be satisfied. When switching from LP to HS mode, the clock lane must enter HS mode first, and the data lane can enter high speed mode afterwards. The minimum timing defined in MIPI DPHY specification needs to be satisfied too. All the switching procedure is handled by the D-PHY.

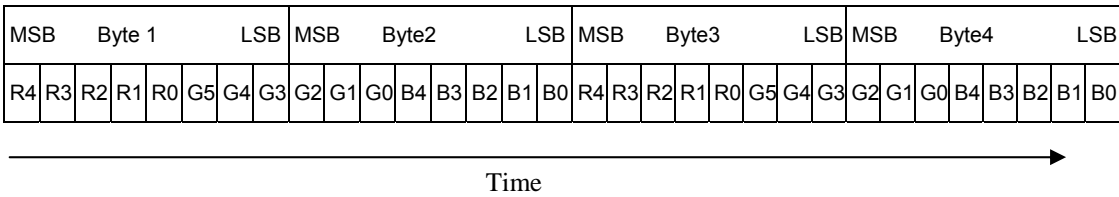
The D-PHY will perform the handshaking for BTA too.

Data Bit Operation

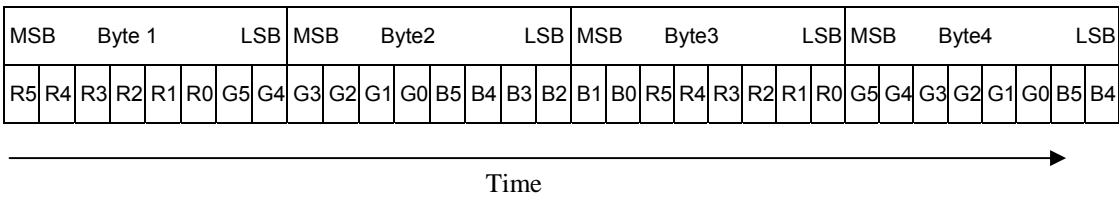
Two control bit **END** and **CO** are defined in MIPI RX IP for more flexibility to support different requirement from the display driver. They are not required for DCS and DSI compliant devices. In some special case, the user needs to use them to adjust the output. The usage of the two control bits are given below. For MIPI video packets, the **END** bit must be 1 and **CO** bit must be 0 in order to be compliant with the standard.

Below is the order to receive the display data over the serial link, when the **END** bit is 1 and **CO** bit is 0

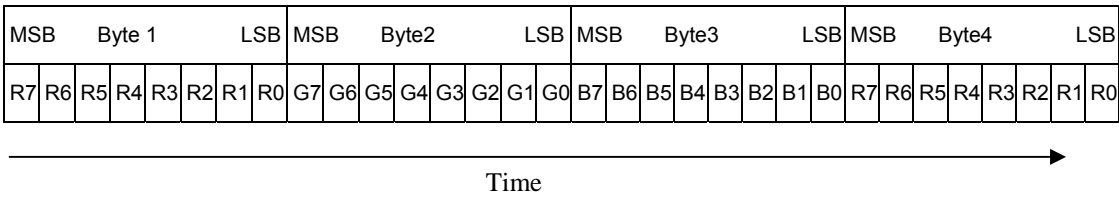
For 16 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.



For 18 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

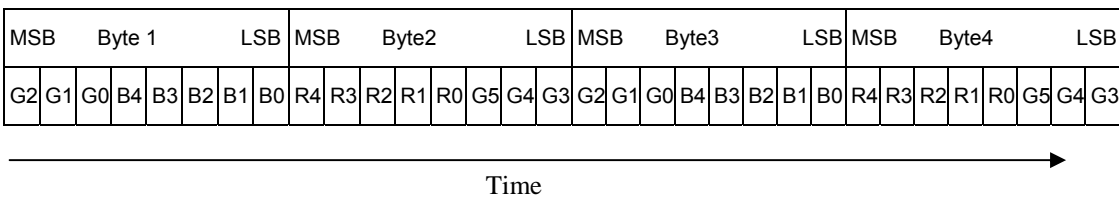


For 24 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

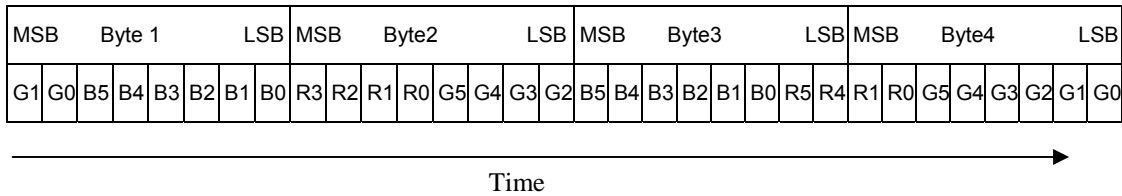


Below is the order to send the display data over the serial link, when the **END** bit is 0 and **CO** bit is 0.

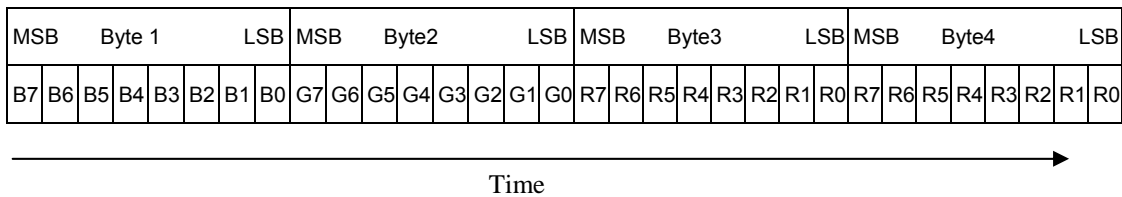
For 16 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.



For 18 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

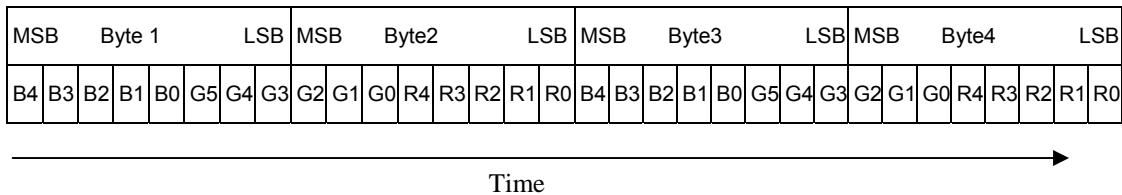


For 24 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

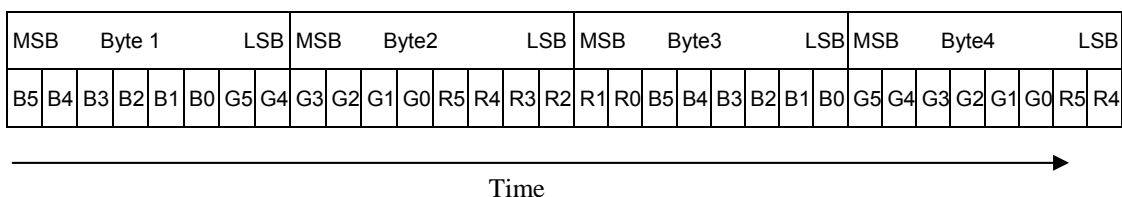


Below is the order to send the display data over the serial link, when the **END** bit is 1 and **CO** bit is 1.

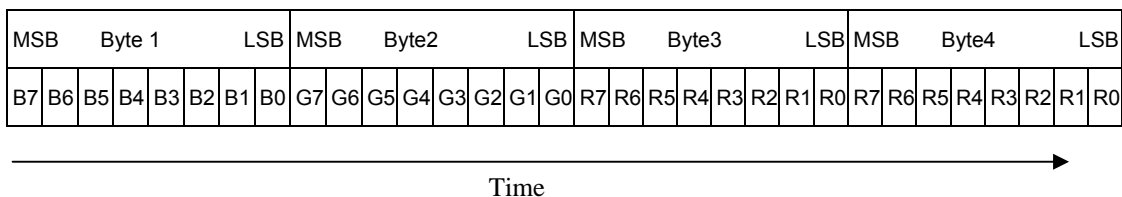
For 16 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.



For 18 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.



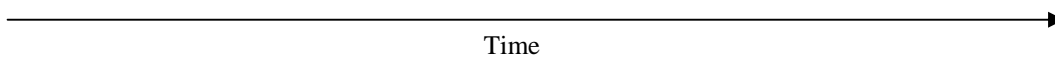
For 24 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.



Below is the order to send the display data over the serial link, when the **END** bit is 0 and **CO** bit is 1.

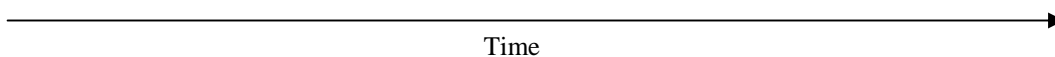
For 16 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB	Byte 1								LSB	MSB	Byte2								LSB	MSB	Byte3								LSB	MSB	Byte4								LSB
G2	G1	G0	R4	R3	R2	R1	R0	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R4	R3	R2	R1	R0	B4	B3	B2	B1	B0	G5	G4	G3								



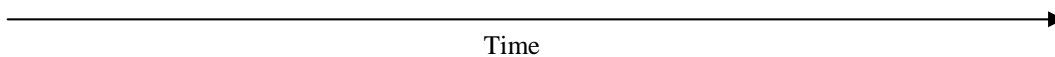
For 18 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB	Byte 1									LSB	MSB	Byte2									LSB	MSB	Byte3									LSB	MSB	Byte4									LSB
G1	G0	R5	R4	R3	R2	R1	R0	B3	B2	B1	B0	G5	G4	G3	G2	R5	R4	R3	R2	R1	R0	B5	B4	B1	B0	G5	G4	G3	G2	G1	G0												



For 24 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB	Byte 1									LSB	MSB	Byte2									LSB	MSB	Byte3									LSB	MSB	Byte4									LSB
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0												



7 Video Timing Control Module (VTCM)

Features

- DCS command or video bypass together with data compression (SSL segment-based & Qualcomm line-based) to reduce the bandwidth requirement during data transmission.
- Support real-time update of Qualcomm capabilities exchange
- 90 degree anti-clockwise rotation mode together with horizontal and vertical flip to complete the 90, 180 & 270 degree rotation.
- Horizontal & vertical scaler to up & down scale the video data
- Built-in frame buffer to support video data self-refresh, so the refresh frequency from application processor can be reduced or stopped during static frames.
- Low power mode support via frame skipping
- Variable pixel clock generation to dynamically change video refresh rate for power saving
- Various tearing output mode to support real time anti-tearing data update.
- Idle frame detection and controllable black/white frame insert to avoid sticky frame when input data are static

Below shows the block diagram for VTCM:

Note: While the diagram below shows 2 sets of (horizontal and vertical scaler), there is only one set in VTCM. This means that either down-scaling before going into the RAM or up-scaling after reading from the RAM can be supported, but not both at the same time.

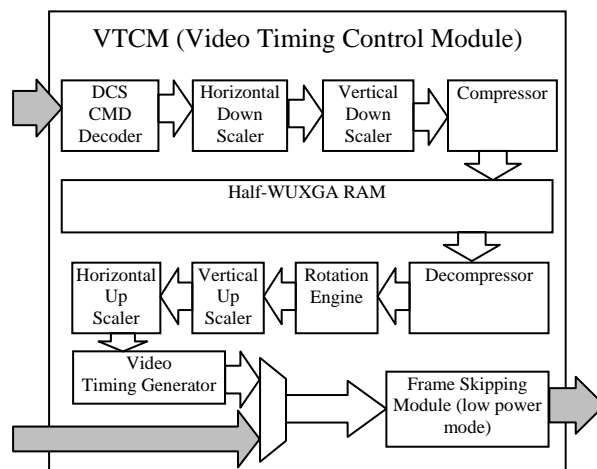


Figure 7-1: VTCM Block Diagram

References

- MIPI® Alliance Specification for Display Command Set (DCS) – Version 1.08 – 22 November 2011
- Qualcomm Frame Buffer Compression Algorithm and Design Document – Updated 27 September 2012
- AMBA™ Specification – Rev 2.0 – 13 May 1999

Limitations

- In command mode, if there is a continuous frame send, a minimum of 4 bclk pause is require between frames.

- There are minimum setting requirement for display period start (a.k.a. back porch), which are 8 for horizontal and 9 for vertical.
- The minimum display size is 32x32 resolutions.
- For frame width setting, have to be 8-pixels aligned before rotation, if compressed data input, then is 4-pixels aligned.
- For SSL segment based compression, minimum segment for partial update is 8 pixels.
- For Qualcomm line-based compression, minimum segment for partial update is 1 line.
- Limitation for scaler
 - Upscale only at the output of RAM
 - Downscale only at the input of RAM, and can only support full-frame update (left-to-right, top-to-bottom update only)
 - No concurrent upscale and downscale
- Limitation for rotation
 - SSL Compression: Up to 1280x800 resolution
 - No Compression: Up to 960x600 resolution
 - Qualcomm Compression: Not supported
 - Full Frame update only (no partial update allowed)
 - No partial display support.

Programming Model

For partial display setting, the start row and end row are referring to Display Height

All reserved bits return zero on read and shall always be written with zero. Writing any other value to a reserved bit will result in indeterminate behavior.

Table 7–1: VTCM Register Summary

Offset	Name	Mnemonic	Reset Value
0x0000	VTCM Device Identification Register	VTCM_IDR	0x03810440
0x0004	VTCM Capabilities Register	VTCM_CAPR	0x00003737
0x0008	VTCM Control Register	VTCM_CTRLR	0x00000000
0x000C	VTCM Configuration Register	VTCM_CFGR	0x00000000
0x0010	VTCM Pixel Clock Frequency Ratio Register	VTCM_PCFRR	0x00010001
0x0014	VTCM Horizontal Display Configuration Register	VTCM_HDCFGR	0x04A40036
0x0018	VTCM Vertical Display Configuration Register	VTCM_VDCFGR	0x08400060
0x001C	VTCM Memory Size Register	VTCM_MSZR	0x07800438
0x0020	VTCM Display Size Register	VTCM_DSZR	0x07800438
0x0024	VTCM Panel Size Register	VTCM_PSZR	0x07800438
0x0028	VTCM Idle Frame & URAM Configuration Register	VTCM_IFNURCFGR	0x11110000
0x002C	VTCM Idle Frame Count Register	VTCM_IFCTRLR	0x00000000
0x0030	VTCM URAM Control Register	VTCM_UCTRLR	0x00000008
0x0034	VTCM Panel Offset Start Register	VTCM_POSR	0x00000000
0x0038	VTCM Panel Offset End Register	VTCM_POER	0x07800438
0x003C	VTCM Image Size Register	VTCM_ISZR	0x07800438
0x0040	VTCM Vertical Scaler Control 1 Register	VTCM_VSCTRL1R	0x00000000
0x0044	VTCM Vertical Scaler Control 2 Register	VTCM_VSCTRL2R	0x00000000
0x0048	VTCM Vertical Scaler Low Register 0	VTCM_VSLR0	0x00000000
0x004C	VTCM Vertical Scaler High Register 0	VTCM_VSHR0	0x00000000
0x0050	VTCM Vertical Scaler Low Register 1	VTCM_VSLR1	0x00000000
0x0054	VTCM Vertical Scaler High Register 1	VTCM_VSHR1	0x00000000
0x0058	VTCM Vertical Scaler Low Register 2	VTCM_VSLR2	0x00000000
0x005C	VTCM Vertical Scaler High Register 2	VTCM_VSHR2	0x00000000

Offset	Name	Mnemonic	Reset Value
0x0060	VTCM Vertical Scaler Low Register 3	VTCM_VSLR3	0x00000000
0x0064	VTCM Vertical Scaler High Register 3	VTCM_VSHR3	0x00000000
0x0068	VTCM Vertical Scaler Low Register 4	VTCM_VSLR4	0x00000000
0x006C	VTCM Vertical Scaler High Register 4	VTCM_VSHR4	0x00000000
0x0070	VTCM Horizontal Scaler Control 1 Register	VTCM_HSCTRL1 R	0x00000000
0x0074	VTCM Horizontal Scaler Control 2 Register	VTCM_HSCTRL2 R	0x00000000
0x0078	VTCM Horizontal Scaler Low Register 0	VTCM_HSLR0	0x00000000
0x007C	VTCM Horizontal Scaler High Register 0	VTCM_HSHR0	0x00000000
0x0080	VTCM Horizontal Scaler Low Register 1	VTCM_HSLR1	0x00000000
0x0084	VTCM Horizontal Scaler High Register 1	VTCM_HSHR1	0x00000000
0x0088	VTCM Horizontal Scaler Low Register 2	VTCM_HSLR2	0x00000000
0x008C	VTCM Horizontal Scaler High Register 2	VTCM_HSHR2	0x00000000
0x0090	VTCM Horizontal Scaler Low Register 3	VTCM_HSLR3	0x00000000
0x0094	VTCM Horizontal Scaler High Register 3	VTCM_HSHR3	0x00000000
0x0096	VTCM Horizontal Scaler Low Register 4	VTCM_HSLR4	0x00000000
0x009C	VTCM Horizontal Scaler High Register 4	VTCM_HSHR4	0x00000000
0x00A0	VTCM Qualcomm FBC Control Register	VTCM_QFBCCTR LR	0x00004151
0x00A4	VTCM Qualcomm FBC Size Register	VTCM_QFBCSZR	0x07800438
0x00A8	VTCM Qualcomm FBC Configuration Register	VTCM_QFBCCFG R	0xC21C4534
0x00AC	VTCM Qualcomm FBC Control 2 Register	VTCM_QFBCCTR L2R	0x00000005
0x00B0	VTCM Qualcomm FBC Control 3 Register	VTCM_QFBCCTR L3R	0x02008000
0x00B4	VTCM Qualcomm FBC Status Register	VTCM_QFBCSTS R	0x00000000
0x0FFC	VTCM Test Register	VTCM_TSTR	0x00000000

Register Description

VTCM Device Identification Register

VTCM_IDR		VTCM Identification Register							Offset Address	
									0x0000	
BIT	31	30	29	28	27	26	25	24		
NAME	CLID[15:8]									
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0	0	0	0	0	0	1	1		
BIT	23	22	21	20	19	18	17	16		
NAME	CLID[7:0]									
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	1	0	0	0	0	0	0	0	1	
BIT	15	14	13	12	11	10	9	8		
NAME	DSGNR[5:0]						MJR[3:2]			
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0	0	0	0	0	1	0	0		
BIT	7	6	5	4	3	2	1	0		
NAME	MJR[1:0]		MNR[5:0]							
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0	1	0	0	0	0	0	0	0	

Table 7-2: VTCM Device Identification Register Description

Name	Description	Setting
CLID[15:0] Bit 31-16	PCI Class Code – This field represents the PCI class code of the VTCM.	0x0381
DSGNR[5:0] Bit 15-10	Design Number – This field represents the design number of the VTCM.	0x01
MAJOR[3:0] Bit 9-6	Major Revision Number – This field represents the major release of the VTCM.	0x01
MINOR[5:0] Bit 5-0	Minor Revision Number – This field represents the minor release of the VTCM.	0x00

VTCM Capabilities Register

Offset Address

VTCM_CAPR

VTCM Capabilities Register

0x0004

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME			VBM	LPM		DS	VS	HS
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	1	1	0	1	1	1
BIT	7	6	5	4	3	2	1	0
NAME			SSLC	QCC		VF	HF	ROT90
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	1	1	0	1	1	1

Table 7-3: VTCM Capabilities Register Description

Name	Description	Setting
Reserved Bit 31–14	Reserved	
VBM Bit 13	Video Bypass Mode Support – Support of video bypass operation.	0 = Not supported 1 = Supported
LPM Bit 12	Low Power Mode Support – Support of low power mode.	0 = Not supported 1 = Supported
Reserved Bit 11–10	Reserved	
DS Bit 10	Down Scale Support – Support of down scale operation.	0 = Not supported 1 = Supported
VS Bit 9	Vertical Scaler Support – Support of vertical scaler operation.	0 = Not supported 1 = Supported
HS Bit 8	Horizontal Scaler Support – Support of horizontal scaler operation.	0 = Not supported 1 = Supported
Reserved Bit 7–6	Reserved	
SSLC Bit 5	SSL Compressor/De-compressor Support – Support of SSL compressor/de-compressor.	0 = Not supported 1 = Supported
QCC Bit 4	Qualcomm Compressor/De-compressor Support – Support of Qualcomm compressor/de-compressor.	0 = Not supported 1 = Supported
Reserved Bit 3	Reserved	
VF	Vertical Flip – Support of vertical flip.	0 = Not supported

Name	Description	Setting
Bit 2		1 = Supported
HF Bit 1	Horizontal Flip – Support of horizontal flip.	0 = Not supported 1 = Supported
ROT90 Bit 0	Rotate 90° Support – Support of rotation of 90° (anti-clockwise).	0 = Not supported 1 = Supported

VTCM Control Register

Offset Address

VTCM_CTRLR

VTCM Control Register

0x0008

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	MF_CNT[3:0]				IU	DOWN_SC ALE		EN
TYPE	RW	RW	RW	RW	RW	RW	RO	RW
RESET	0	0	0	0	0	0	0	0

Table 7-4: VTCM Control Register Description

Name	Description	Setting
Reserved Bit 31–8	Reserved	
MF_CNT Bit 7-4	Mask Frame Count – These bits specified the number of frame that will be mask off after initial display on (after received DCS set_display_on, command 29h from application processor)..	0 = no mask off frame 1 = mask off 1 frame : F = mask off 15 frame
IU Bit 3	In Use – This bit indicates whether the software has finished updating the VTCM Pixel Clock Frequency Ratio Register or not. After software finishes the updating, the new register setting will take effect. Otherwise, the previous setting will take effect.	0 = Software has finished updating 1 = Software is still updating
DOWN_SCAL E Bit 2	Down Scale – This bit select the operation mode of the VTCM module. If this bit is cleared, then both the vertical scaler and horizontal scaler are place after the memory fetching, else they will place before the memory is written.	0 = Up scale select. 1 = Down scale select
Reserved Bit 1	Reserved	
EN Bit 0	Module Enable – This bit enables VTCM.	0 = Disabled 1 = Enabled

VTCM Configuration Register

Offset Address

VTCM_CFGR

VTCM Configuration Register

0x000C

BIT	31	30	29	28	27	26	25	24
NAME	FLPM[15:8]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	FLPM[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME				PAD_PIXE L_SEL			SPLIT_ME M	ROT90
TYPE	RO	RO	RO	RW	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME			ENDIAN	WRAP		VBP	TE_SEL	TEP
TYPE	RO	RO	RW	RW	RO	RW	RW	RW
RESET	0	0	0	0	0	0	0	0

Table 7-5: VTCM Configuration Register Description

Name	Description	Setting
Reserved Bit 31–24	Reserved	
FLPM Bit 27-16	Frame Low Power Mode – These bits indicates number of frame skip in low power mode.	0 : Normal frame scanning (LPM disabled) 1 : Skip 1 frames : FFF : Skip 4097 frames
Reserved Bit 15–13	Reserved	
PAD_PIXEL_SEL Bit 12	Padding Pixel Select – This bit select the pixel to display for the padding period.	0 = Select padding pixels to be 0x000000. 1 = Select padding pixels to be 0xffff
Reserved Bit 11–10	Reserved	
SPLIT_MEM Bit 9	Split Memory – This bit enable the splitting of frame buffer memory. If this bit set, then the whole frame buffer will be used for the display, else frame buffer memory is split into 2 pieces. For display other than 0°, this bit need to set to 1.	0 = No splitting of frame buffer memory 1 = Split frame buffer memory.
ROT90 Bit 8	Rotate 90° – This bit enable the output frame data to rotate 90° (anti-clock wise).	0 = No rotation 1 = Rotate 90° anti-clock wise
Reserved Bit 7–6	Reserved	
ENDIAN	Endian - This bit indicates the endianness of the data	0 = Little Endian (send out LSB)

Bit 5	that send in from the MIPI interface	first) 1 = Big Endian (send out MSB first)
WRAP Bit 4	Wrap - This bit indicates excess video data that come in from MIPI interface.	0 = Excess video data will be discarded. 1 = Excess video data will be wrapped to the beginning of the defined memory starting address (DCS command Start Page Address & Start Column Address).
Reserved Bit 3	Reserved	
VBP Bit 2	Video Bypass - This bit enable/disable the video input path.	0 = Disabled 1 = Enabled
TE_SEL Bit 1	Tear Select - This bit select the tear signal is generated from data fetching unit or display interface unit.	0 = Tear signal from data fetching unit 1 = Tear signal from display interface unit
TEP Bit 0	Tear Polarity - This bit specify the polarity of vtc _m _rgb_te signal.	0 = Active high 1 = Active low

VTM Pixel Clock Frequency Ratio Register

Offset Address

VTM_PCFRR

VTM Pixel Clock Frequency Ratio Register

0x0010

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	PCLKDEN[7:0]							
TYPE	RW							
RESET	0x1							
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	PCLKNUM[6:0]							
TYPE	RO	RW						
RESET	0	0x1						

Table 7-6: VTCM Pixel Clock Frequency Ratio Register Description

Name	Description	Setting
Reserved Bit 31-24	Reserved	
PCLKDEN Bit 23-16	Pixel Clock Divider Denominator – This is the denominator of the clock divider for Pixel Clock.	The minimum value of this field is 0x1.
Reserved Bit 15-7	Reserved	
PCLKNUM Bit 6-0	Pixel Clock Divider Numerator – This is the numerator of the clock divider for Pixel Clock.	The minimum value of this field is 0x1.

Note:

Pixel clock frequency = System clock frequency x divider ratio

Divider ratio = PCLKNUM / PCLKDEN

VTCM Horizontal Display Configuration Register

Offset Address

VTCM_HDCFGR

VTCM Display Horizontal Configuration Register

0x0014

BIT	31	30	29	28	27	26	25	24
NAME	HT[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	0	0
BIT	23	22	21	20	19	18	17	16
NAME	HT[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	1	0	1	0	0	1	0	0
BIT	15	14	13	12	11	10	9	8
NAME	HDPS[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	HDPS[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	1	1	0	1	1	0

Table 7-7: VTCM Display Horizontal Configuration Register Description

Name	Description	Setting
Reserved Bit 31–29	Reserved	
HT Bit 28-16	Horizontal Total – These bits define the Horizontal Total period. The Horizontal Total is the sum of the Horizontal Display period and the Horizontal Non-Display period.	The value of Horizontal Total (in number of pixels)
Reserved Bit 15–13	Reserved	
HDPS Bit 12-0	Horizontal Display Period Start – These bits define the start position of Horizontal Display Period. When VBP (Video Bypass bit of VTCM Control Register) is set, these bits are mean to set the minimum horizontal back porch.	When VBP = 0 – Start position in 1 pixel resolution. Minimum setting is 8 and need to be in even number. When VBP = 1 – Setting of minimum horizontal back porch.

VTCM Vertical Display Configuration Register

Offset Address

VTCM_VDCFGR

VTCM Vertical Display Configuration Register

0x0018

BIT	31	30	29	28	27	26	25	24
NAME	VT[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	1	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	VT[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	1	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	VDPS[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	VDPS[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	1	1	0	0	0	0	0

Table 7-8: VTCM Vertical Display Configuration Register Description

Name	Description	Setting
Reserved Bit 31–29	Reserved	
VT Bit 28-16	Vertical Total – These bits define the Vertical Total period, in 1 line resolution. The Vertical Total is the sum of the Vertical Display Period and the Vertical Non-Display Period.	The value of Vertical Total (in number of lines).
Reserved Bit 15–13	Reserved	
VDPS Bit 12-0	Vertical Display Period Start – These bits define the start position of Vertical Display Period.	Position in 1 line resolution. Minimum setting is 10.

VTCM Memory Size Register

Offset Address
0x001C

VTCM_MSZR		VTCM Memory Size Register						
BIT	31	30	29	28	27	26	25	24
NAME	MHEIGHT[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	1	1
BIT	23	22	21	20	19	18	17	16
NAME	MHEIGHT[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	1	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	MWIDTH[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	0	0
BIT	7	6	5	4	3	2	1	0
NAME	MWIDTH[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	1	1	1	0	0	0

Table 7-9: VTCM Memory Size Register Description

Name	Description	Setting
Reserved Bit 31–29	Reserved	
MHEIGHT Bit 28-16	Memory Height – These bits specify the Memory Vertical Display period, in 1 line resolutions. The Vertical Display period should be less than the Vertical Total to allow for a sufficient Vertical Non-Display period. The height refers to the height of the window before rotation.	Vertical Display Period (in number of lines)
Reserved Bit 15–13	Reserved	
MWIDTH Bit 12-0	Memory Width – These bits specify the Memory Horizontal Display period, in 1 pixel resolution. The Horizontal Display period should be less than the Horizontal Total to allow for a sufficient Horizontal Non-Display period. The width refers to the width of the window before rotation.	Horizontal Display Period (in number of pixels)

Note: These are the setting after the down scale.

VTCM Display Size Register

Offset Address

VTCM_DSZR

VTCM Display Size Register

0x0020

BIT	31	30	29	28	27	26	25	24
NAME	DHEIGHT[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	1	1
BIT	23	22	21	20	19	18	17	16
NAME	DHEIGHT[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	1	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	DWIDTH[15:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	0	0
BIT	7	6	5	4	3	2	1	0
NAME	DWIDTH[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	1	1	1	0	0	0

Table 7-10: VTCM Display Size Register Description

Name	Description	Setting
Reserved Bit 31–29	Reserved	
DHEIGHT Bit 28-16	Display Height – These bits specify the Vertical Display period, in 1 line resolutions. The Vertical Display period should be less than the Vertical Total to allow for a sufficient Vertical Non-Display period. The height refers to the height of the window after rotation.	Vertical Display Period (in number of lines)
Reserved Bit 15–13	Reserved	
DWIDTH Bit 12-0	Display Width – These bits specify the Horizontal Display period, in 1 pixel resolution. The Horizontal Display period should be less than the Horizontal Total to allow for a sufficient Horizontal Non-Display period. The width refers to the width of the window after rotation.	Horizontal Display Period (in number of pixels)

Note: These are the setting after the down scale and before the up scale.

VTCM Panel Size Register

Offset Address

VTCM_PSZR

VTCM Panel Size Register

0x0024

BIT	31	30	29	28	27	26	25	24
NAME	PHEIGHT[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	1	1
BIT	23	22	21	20	19	18	17	16
NAME	PHEIGHT[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	1	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	PWIDTH[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	0	0
BIT	7	6	5	4	3	2	1	0
NAME	PWIDTH[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	1	1	1	0	0	0

Table 7-11: VTCM Panel Size Register Description

Name	Description	Setting
Reserved Bit 31–29	Reserved	
PHEIGHT Bit 28-16	Panel Height – These bits specify the Panel Vertical Display period, in 1 line resolutions. The Vertical Display period should be less than the Vertical Total to allow for a sufficient Vertical Non-Display period. The height refers to the height of the window after rotation.	Vertical Display Period (in number of lines)
Reserved Bit 15–13	Reserved	
PWIDTH Bit 12-0	Panel Width – These bits specify the Panel Horizontal Display period, in 1 pixel resolution. The Horizontal Display period should be less than the Horizontal Total to allow for a sufficient Horizontal Non-Display period. The width refers to the width of the window after rotation.	Horizontal Display Period (in number of pixels)

Note: These are the setting after the down scale and up scale.

VTM Idle Frame & URAM Configuration Register

Offset Address

VTM_IFNURCFGR

VTM Idle Frame & URAM Configuration Register

0x0028

BIT	31	30	29	28	27	26	25	24
NAME	TMWLSA[3:0]				TMSA2CS[3:0]			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	1	0	0	0	1
BIT	23	22	21	20	19	18	17	16
NAME	TMPSCS[3:0]				TMCS2PR[3:0]			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	1	0	0	0	1
BIT	15	14	13	12	11	10	9	8
NAME			FORCE_R AM_CENB	FORCE_R AM_CLK			TMEQ2WL	BYPASS
TYPE	RO	RO	RW	RW	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME						IDLE_MOD E	IDLE_PIXE L_SEL	IDLE_FRA ME_EN
TYPE	RO	RO	RO	RO	RO	RW	RW	RW
RESET	0	0	0	0	0	0	0	0

Table 7-12: VTCM Idle Frame & URAM Configuration Register Description

Name	Description	Setting
TMWLSA Bit 31–28	TMWLSA – Wordline to FSA enable delay. Only and exactly 1 bit is set to 1, and the default setting is h'1.	
TMSA2CS Bit 27-24	TMSA2CS – FSA enable to CSL delay. Only and exactly 1 bit is set to 1, and default setting is h'1.	
TMPSCS Bit 23-20	TMPSCS – CSL pulse delay. Only and exactly 1 bit is set to 1, and the default setting is h'1.	
TMCS2PR Bit 19-16	TMCS2PR – CSL to wordline precharge delay. Only and exactly 1 bit is set to 1, and default setting is h'1.	
Reserved Bit 15–14	Reserved	
FORCE_RAM_CENB Bit 13	Force RAM CENB – This bit enable the forcing of URAM chip enable. If this bit is set to 1, then the URAM chip enable will always assert.	
FORCE_RAM_CLK Bit 12	Force RAM CLK – This bit enable the forcing of URAM clock enable. If this bit is set to 1, then the URAM clock will always on.	
Reserved Bit 11–10	Reserved	
TMEQ2WL Bit-9	TMEQ2WL – Equalize falling to wordline rising delay. The default setting is logic 0.	
BYPASS Bit-8	BYPASS – ECC Off control Signal.	
Reserved	Reserved	

Bit 7-3		
IDLE_MODE Bit 2	IDLE Mode - This bit select the idle mode.	0 = Black/White frame will be output back to back. 1 = Black/White frame will be output one frame follow by 2 frame from frame buffer and then follow by one more black/white frame.
IDLE_PIXEL_SEL Bit 1	Idle Pixel Select – This bit select the pixel to display when there is no video data update from the application processor for period specified in Idle Period .	0 = Select output pixels during idle frame to be 0x000000. 1 = Select output pixels during idle frame to be 0xffff
IDLE_FRAME_EN Bit 0	Idle Frame Enable – This bit enable the idle frame feature.	0 = Idle frame detection disable 1 = Idle frame detection enable

VTM Idle Frame Count Register

Offset Address

VTM_IFCNTR

VTM Idle Frame Count Register

0x002C

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	IDLE_PERIOD[15:8]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	IDLE_PERIOD[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0

Table 7-13: VTM Idle Frame Count Register Description

Name	Description	Setting
Reserved Bit 31-16	Reserved	
IDLE_PERIOD Bit 15-0	Idle Period – These bits define the number of frame that will be consider a continuous idle period (no DCS write_memory_start or write_memory_continue is receive from the application processor). These bits setting will start a down-counter, in anytime if there is any DCS write_memory_start or write_memory_continue command received, the down-counter will be restart from Idle Period . If the down-counter continues to count to zero, then an idle frame with Idle Pixel Select will be sent out, and the process continues.	

VTM URAM Control Register

Offset Address

VTM_UCTRLR

VTM URAM Control Register

0x0030

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	REF_PERIOD[15:8]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	REF_PERIOD[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	1	0	0	0

Table 7-14: VTM URAM Control Register Description

Name	Description	Setting
Reserved Bit 31-16	Reserved	
REF_PERIOD Bit 15-0	Refresh Period – These bits define the refresh period of the URAM (period is refer to sysclk divide by 4, and the refresh period should be set to maximum of 1us).	

VTCM Panel Offset Start Register

Offset Address

VTCM_POSR

VTCM Panel Offset Start Register

0x0034

BIT	31	30	29	28	27	26	25	24
NAME	PHEIGHT_OFF_START[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	PHEIGHT_OFF_START[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	PWIDTH_OFF_START[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	PWIDTH_OFF_START[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0

Table 7-15: VTCM Panel Offset Start Register Description

Name	Description	Setting
Reserved Bit 31–29	Reserved	
PHEIGHT_OFF_START Bit 28-16	Panel Height Offset Start – These bits specify the panel height offset start, in 1 line resolutions.	
Reserved Bit 15–13	Reserved	
PWIDTH_OFF_F_START Bit 15-0	Panel Width Offset Start – These bits specify the panel width offset start, in 1 pixel resolution.	

VTCM Panel Offset End Register

Offset Address

VTCM_POER

VTCM Panel Offset End Register

0x0038

BIT	31	30	29	28	27	26	25	24
NAME	PHEIGHT_OFF_END[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	1	1
BIT	23	22	21	20	19	18	17	16
NAME	PHEIGHT_OFF_END[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	1	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	PWIDTH_OFF_END[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	0	0
BIT	7	6	5	4	3	2	1	0
NAME	PWIDTH_OFF_END[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	1	1	1	0	0	0

Table 7-16: VTCM Panel Offset End Register Description

Name	Description	Setting
Reserved Bit 31–29	Reserved	
PHEIGHT_O FF_END Bit 28-16	Panel Height Offset End – These bits specify the panel height offset end, in 1 line resolutions.	
Reserved Bit 15–13	Reserved	
PWIDTH_OF F_END Bit 12-0	Panel Width Offset End – These bits specify the panel width offset end, in 1 pixel resolution.	

VTCM Image Size Register

Offset Address

VTCM_ISZR

VTCM Image Size Register

0x003C

BIT	31	30	29	28	27	26	25	24
NAME	IHEIGHT[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	1	1
BIT	23	22	21	20	19	18	17	16
NAME	IHEIGHT[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	1	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	IWIDTH[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	0	0
BIT	7	6	5	4	3	2	1	0
NAME	IWIDTH[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	1	1	1	0	0	0

Table 7-17: VTCM Image Size Register Description

Name	Description	Setting
Reserved Bit 31–29	Reserved	
IHEIGHT Bit 28-16	Image Height – These bits specify the Image Vertical Display period, in 1 line resolutions.	(in number of lines)
Reserved Bit 15–13	Reserved	
IWIDTH Bit 12-0	Image Width – These bits specify the Image Horizontal Display period, in 1 pixel resolution.	(in number of pixels)

VTM Vertical Scaler Control 1 Register

Offset Address

VTM_VSCTRL1R

VTM Vertical Scaler Control 1 Register

0x0040

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME				SSF[4:0]				
TYPE	RO	RO	RO	RW				
RESET	0	0	0	0x0				
BIT	15	14	13	12	11	10	9	8
NAME	SSS[11:4]							
TYPE	RW							
RESET	0							
BIT	7	6	5	4	3	2	1	0
NAME	SSS[3:0]						VALIGN	EN
TYPE	RW				RO	RO	RW	RW
RESET	0				0	0	0	0

Table 7-18: VTCM Vertical Scaler Control 1 Register Description

Name	Description	Setting
Reserved Bit 31-21	Reserved	
SSF Bit 20-16	Step Size Fullpel – These bits specify the full pel step size of vertical scaling operation.	
SSS Bit 15-4	Step Size Subpel – These bits specify the subpel step size of vertical scaling operation.	
Reserved Bit 3-2	Reserved	
VALIGN Bit 1	Vertical Alignment – This bit specifies the alignment of vertical scaling operation.	
EN Bit 0	Enable – This bit enable/disable the vertical scaling operation.	0 = Disabled 1 = Enabled

VTCM Vertical Scaler Control 2 Register

VTCM_VSCTRL2R		VTCM Vertical Scaler Control 2 Register							Offset Address
									0x0044
BIT	31	30	29	28	27	26	25	24	
NAME									
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16	
NAME									
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8	
NAME					SS[11:8]				
TYPE	RO	RO	RO	RO	RW				
RESET	0	0	0	0	0x0				
BIT	7	6	5	4	3	2	1	0	
NAME	SS[7:0]								
TYPE	RW								
RESET	0x0								

Table 7-19: VTCM Vertical Scaler Control 2 Register Description

Name	Description	Setting
Reserved Bit 31-12	Reserved	
SS Bit 11-0	Step Start – These bits specify the step start position of vertical scaling operation	

VTCM Vertical Scaler Low Register <N>

VTCM_VSLR<N>

VTCM Vertical Scaler Low Register <N>

Offset Address

0x0048 + 8*<N>

(N = 0 – 4)

BIT	31	30	29	28	27	26	25	24
NAME	C1[9:8]							
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	C1[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	C0[9:8]							
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	C0[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0

Table 7-20: VTCM Vertical Scaler Low Register <N> Description

Name	Description	Setting
Reserved Bit 31-26	Reserved	
C1 Bit 25-16	C1 – These bits specify the coefficient C1 of vertical scaling operation.	-512 to 511
Reserved Bit 15-10	Reserved	
C0 Bit 9-0	C0 – These bits specify the coefficient C0 of vertical scaling operation.	-512 to 511

VTCM Vertical Scaler High Register <N>

VTCM_VSHR<N>

VTCM Vertical Scaler High Register <N>

Offset Address

0x004C + 8* <N>

(N = 0 – 4)

BIT	31	30	29	28	27	26	25	24
NAME	C3[9:8]							
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	C3[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	C2[9:8]							
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	C2[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0

Table 7-21: VTCM Vertical Scaler High Register <N> Description

Name	Description	Setting
Reserved Bit 31-26	Reserved	
C3 Bit 25-16	C3 – These bits specify the coefficient C3 of vertical scaling operation.	-512 to 511
Reserved Bit 15-10	Reserved	
C2 Bit 9-0	C2 – These bits specify the coefficient C2 of vertical scaling operation.	-512 to 511

VTCM Horizontal Scaler Control 1 Register

Offset Address

VTCM_HSCTRL1R

VTCM Horizontal Scaler Control 1 Register

0x0070

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME					SSF[3:0]			
TYPE	RO	RO	RO	RO	RW			
RESET	0	0	0	0	0x0			
BIT	15	14	13	12	11	10	9	8
NAME	SSS[11:4]							
TYPE	RW							
RESET	0							
BIT	7	6	5	4	3	2	1	0
NAME	SSS[3:0]						HALIGN	EN
TYPE	RW				RO	RO	RW	RW
RESET	0				0	0	0	0

Table 7-22: VTCM Horizontal Scaler Control 1 Register Description

Name	Description	Setting
Reserved Bit 31-20	Reserved	
SSF Bit 19-16	Step Size Fullpel – These bits specify the full pel step size of horizontal scaling operation.	
SSS Bit 15-4	Step Size Subpel – These bits specify the subpel step size of horizontal scaling operation.	
Reserved Bit 3-2	Reserved	
VALIGN Bit 1	Horizontal Alignment – This bit specifies the alignment of horizontal scaling operation.	
EN Bit 0	Enable – This bit enable/disable the horizontal scaling operation.	0 = Disabled 1 = Enabled

VTCM Horizontal Scaler Control 2 Register

VTCM_HCTRL2R		VTCM Horizontal Scaler Control 2 Register							Offset Address
									0x0074
BIT	31	30	29	28	27	26	25	24	
NAME									
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16	
NAME									
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8	
NAME					SS[11:8]				
TYPE	RO	RO	RO	RO	RW				
RESET	0	0	0	0	0x0				
BIT	7	6	5	4	3	2	1	0	
NAME	SS[7:0]								
TYPE	RW								
RESET	0x0								

Table 7-23: VTCM Horizontal Scaler Control 2 Register Description

Name	Description	Setting
Reserved Bit 31-12	Reserved	
SS Bit 11-0	Step Start – These bits specify the step start position of horizontal scaling operation	

VTCM Horizontal Scaler Low Register <N>

VTCM_HSLR<N>

VTCM Horizontal Scaler Low Register <N>

Offset Address

0x0078 + 8* <N>

(N = 0 – 4)

BIT	31	30	29	28	27	26	25	24
NAME	C1[9:8]							
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	C1[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	C0[9:8]							
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	C0[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0

Table 7-24: VTCM Horizontal Scaler Low Register <N> Description

Name	Description	Setting
Reserved Bit 31-26	Reserved	
C1 Bit 25-16	C1 – These bits specify the coefficient C1 of horizontal scaling operation.	-512 to 511
Reserved Bit 15-10	Reserved	
C0 Bit 9-0	C0 – These bits specify the coefficient C0 of horizontal scaling operation.	-512 to 511

VTCM Horizontal Scaler High Register <N>

VTCM_HSHR<N>

VTCM Horizontal Scaler High Register <N>

Offset Address

0x007C + 8* <N>

(N = 0 – 4)

BIT	31	30	29	28	27	26	25	24
NAME	C3[9:8]							
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	C3[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	C2[9:8]							
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	C2[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0

Table 7-25: VTCM Horizontal Scaler High Register <N> Description

Name	Description	Setting
Reserved Bit 31-26	Reserved	
C3 Bit 25-16	C3 – These bits specify the coefficient C3 of horizontal scaling operation.	-512 to 511
Reserved Bit 15-10	Reserved	
C2 Bit 9-0	C2 – These bits specify the coefficient C2 of horizontal scaling operation.	-512 to 511

VTCM Qualcomm FBC Control Register

Offset Address

VTCM_QFBCCTRLR

VTCM Qualcomm FBC Control Register

0x00A0

BIT	31	30	29	28	27	26	25	24
NAME							NON_INT_BIAS[9:8]	
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	NON_INT_BIAS[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	OPMODE	PADDING	OPMODE1_CUT		ENC_SWAP	BIT_SWAP	SUBPIX_SWAP	PIX_SWAP
TYPE	RW	RW	RW	RO	RW	RW	RW	RW
RESET	0	1	0	0	0	0	0	1
BIT	7	6	5	4	3	2	1	0
NAME	DEC_MODE[1:0]		COM_MODE[1:0]					FBC_ENABLE
TYPE	RW	RW	RW	RW	RO	RO	RO	RW
RESET	0	1	0	1	0	0	0	1

Table 7-26: VTCM Qualcomm FBC Control Register Description

Name	Description	Setting
Reserved Bit 31–26	Reserved	
NON_INT_BIAS Bit 25-16	Non Interleave Bias – These bits will affect the decision of interleave/progressive mode of the encoder. The larger the value, the more likely for the encoder to choose the progressive mode.	
OPMODE Bit 15	Operation Mode – This bit selects the encoder operation mode.	0 = Both lossless & lossy 1 = Lossless only
PADDING Bit 14	Padding – This bit enabled the padding function of the encoder.	0 = disable 1 = enable
OPMODE1_CUT Bit 13	Operation Mode 1 Cut – This bit is only applicable if OPMODE is 1. If OPMODE is 1: the output bitstream will not exceed the TARGET_SIZE . If OPMODE is 0: encoder will output all the bitstream regardless of the TARGET_SIZE .	
Reserved Bit 12	Reserved	
ENC_SWAP Bit 11	Encoder Swap – This bit specify whether to enable the swap for compressor.	0 = no swap 1 = swap
BIT_SWAP Bit 10	Bit Swap – This bit specify whether to swap the de-compressor input bit order of the sub-pixel.	0 = no swap 1 = swap
SUBPIX_SWAP Bit 9	Sub-pixel Swap – This bit specify whether to swap the de-compressor input sub-pixel order of the pixel.	0 = no swap 1 = swap

PIX_SWAP Bit 10	Pixel Swap – This bit specify whether to swap the de-compressor input pixel order of the double pixel order.	0 = no swap 1 = swap
DEC_MODE Bit 7-6	De-compressor Mode – These bits select the de-compressor use for read data from frame buffer.	00 = Bypass de-compressor 01 = SSL de-compressor select. 10 = Qualcomm de-compressor select. 11 = Select the following de-compression algorithm. Read (24 bits to 48 bits): output the MSB of the pixels with the RAM contents, LSB of the pixels could be zeros, or padding MSB bit {4{B[23]}}, {4{B[15]}}, {4{B[7]}}.
COM_MODE Bit 5-4	Compressor Mode – These bits select the compressor use for write data to frame buffer.	00 = Bypass compressor 01 = SSL compressor select. 10 = Qualcomm compressor select. 11 = Select the following compression algorithm. Write (48 bits to 24 bits) : write MSB of the pixels: B[23:20],B[15:12],B[7:4], into the RAM
Reserved Bit 3-1	Reserved	
FBC_ENABLER Bit 0	FBC Enable – This bit enable FBC.	0 = Disabled 1 = Enabled

VTCM Qualcomm FBC Size Register

Offset Address

VTCM_QFBCSZR

VTCM Qualcomm FBC Size Register

0x00A4

BIT	31	30	29	28	27	26	25	24
NAME	HEIGHT[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	1	1
BIT	23	22	21	20	19	18	17	16
NAME	HEIGHT[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	1	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	WIDTH[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	0	0
BIT	7	6	5	4	3	2	1	0
NAME	WIDTH[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	1	1	1	0	0	0

Table 7-27: VTCM Qualcomm FBC Size Register Description

Name	Description	Setting
Reserved Bit 31–29	Reserved	
HEIGHT Bit 28-16	Height – These bits set the frame height.	0–8192
Reserved Bit 15–13	Reserved	
WIDTH Bit 12-0	Width – These bits set the frame width.	0–8192

VTCM Qualcomm FBC Configuration Register

Offset Address

VTCM_QFBCCFGR

VTCM Qualcomm FBC Configuration Register

0x00A8

BIT	31	30	29	28	27	26	25	24
NAME	PATTERN_ENABLE	BFLC_ENABLE		OWIDTH[12:8]				
TYPE	RW	RW	RO	RW	RW	RW	RW	RW
RESET	1	1	0	0	0	0	1	0
BIT	23	22	21	20	19	18	17	16
NAME	OWIDTH[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	1	1	1	0	0
BIT	15	14	13	12	11	10	9	8
NAME	LOSSY_RGB_THD[3:0]				EXTRA_BUDGET_LEVEL[3:0]			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	1	0	0	0	1	0	1
BIT	7	6	5	4	3	2	1	0
NAME		LOSSY_Y_MODE_INDEX[2:0]			TARGET_SIZE[3:0]			
TYPE	RO	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	1	1	0	1	0	0

Table 7-28: VTCM Qualcomm FBC Configuration Register Description

Name	Description	Setting
PATTERN_ENABLE Bit 31	Pattern Enable – This bit enable pattern.	0 = Disabled 1 = Enabled
BFLC_ENABLE Bit 30	BFLC Enable – This bit enable BFLC.	0 = Disabled 1 = Enabled
Reserved Bit 29	Reserved	
OWIDTH Bit 28-16	Output Width – These bits set the output frame width. Output Width should be programmed as follow: if ((ceil(WIDTH*(TARGET_SIZE+8)/24)%4)==0) OWIDTH = ceil(WIDTH*(TARGET_SIZE+8)/24); else OWIDTH = ceil(WIDTH*(TARGET_SIZE+8)/24)+4-ceil(WIDTH*(TARGET_SIZE+8)/24)%4; Where ceil (n) returns the nearest integer value which is larger than n, and n is a float number.	0-8192
LOSSY_RGB_THD Bit 15-12	Lossy RGB Threshold – If chroma block decision is 444 for a block, and number of chroma bits per pixel is less than this register, use RGB space rather than YC ₀ C _g space (set to 0 to disable).	0-6
EXTRA_BUDGET_LEVEL Bit 11-8	Extra Budget Level – Extra budget for early blocks in each line or frame. Increased chance of lossless block at cost of uniformity.	0-9
Reserved Bit 7	Reserved	

LOSSY_MODE_Y_INDEX Bit 6-4	Lossy Mode Y Index – LUT index for lossy_y_bits vector.	0-7
TARGET_SIZE Bit 3-0	Target Size – These bits select the target size.	0 = 8/24 1 = 9/24 ... 10 = 18/24

VTCM Qualcomm FBC Control 2 Register

Offset Address

VTCM_QFBCCTRL2R

VTCM Qualcomm FBC Control 2 Register

0x0AC

BIT	31	30	29	28	27	26	25	24
NAME	PER_LINE_EXTRA_BUDGET[11:8]							
TYPE	RO	RO	RO	RO	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	PER_LINE_EXTRA_BUDGET[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	PER_BLK_BUDGET[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	YUV_422						VLC_ENABLE	
TYPE	RO	RO	RO	RO	RW	RW	RW	RW
RESET	0	0	0	0	0	1	0	1

Table 7-29: VTCM Qualcomm FBC Control 2 Register Description

Name	Description	Setting
Reserved Bit 31–28	Reserved	
PER_LINE_EXTRA_BUDGET Bit 27-16	Per Line Extra Budget – Additional bit budget or each line (increased chance of lossless blocks at the beginning of the line).	0-2304
PER_BLK_BUDGET Bit 15-8	Per Block Budget – Bit budget for each block.	0-192
Reserved Bit 7–4	Reserved	
YUV_422 Bit 3-1	YUV 422 – Bias for chroma subsampling.	0-5 0 = favor 444 5 = favor 422
VLC_ENABLE Bit 0	VLC Enable – This bit enable VLC.	0 = Disabled 1 = Enabled

VTCM Qualcomm FBC Control 3 Register

Offset Address

VTCM_QFBCCTRL3R

VTCM Qualcomm FBC Control 3 Register

0x00B0

BIT	31	30	29	28	27	26	25	24
NAME							LOSSLESS_MODE_THD [9:8]	
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	LOSSLESS_MODE_THD[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	LOSSY_MODE_THD[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	1	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME								CALC_422 QUANT_EN
TYPE	RO	RO	RO	RO	RO	RO	RO	RW
RESET	0	0	0	0	0	0	0	0

Table 7-30: VTCM Qualcomm FBC Control 3 Register Description

Name	Description	Setting
Reserved Bit 31–28	Reserved	
LOSSLESS_MODE_THD Bit 25-16	Lossless Mode Threshold – If the bit budget exceeds this register, then blocks can be encoded in lossless mode, even if the block requires more than MAX_LOSSLESS_BITS_PER_PX bits.	128-1023
LOSSY_MODE_THD Bit 15-8	Lossy Mode Threshold – Maximum bits for a lossless block.	128-192
Reserved Bit 7–1	Reserved	
CALC_422_QUANT_EN Bit 0	Calculate 422 Quantization Enable – Calculate quantization error in addition to interpolation error for making 422/444 chroma decision.	0 = Disabled 1 = Enabled

VTCM Qualcomm FBC Status Register

Offset Address

VTCM_QFBCSTSR

VTCM Qualcomm FBC Status Register

0x00B4

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME							DATA_OVR R	LOSSY_ST ATUS
TYPE	RO	RO	RO	RO	RO	RO	RW1C	RW1C
RESET	0	0	0	0	0	0	0	0

Table 7-31: VTCM Qualcomm FBC Status Register Description

Name	Description	Setting
Reserved Bit 31–2	Reserved	
DATA_OVR Bit 1	Data Overrun – This bit indicate compressor data overrun detected.	0 = Compressor data overrun not detected 1 = Compressor data overrun detected
LOSSY_STAT US Bit 0	Lossy Status – This bit indicate lossy compression detected.	0 = Lossy Compression not detected 1 = Lossy Compression detected

VTCM Test Register

Offset Address

VTCM_TSTR

VTCM Test Register

0x0FFC

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	RAM_SEL[3:0]				SIG_GRP_SEL[3:0]			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0

Table 7-32: VTCM Test Register Description

Name	Description	Setting
Reserved Bit 31–8	Reserved	
RAM_SEL Bit 7-4	RAM Select – These bits select the RAM to output the test signals.	
SIG_GRP_SEL L Bit 3-0	Signal Group Select – These bits select the signal group to output test signals.	

Note: Refer to vcm_dbg_signal_mux.xls for signal muxing.

DCS Command Support

Besides having registers accessed by APB interface, VTCM support registers defined by DCS commands, of which will be accessed by DCS command directly.

Following are the DCS commands that are supported by the VTCM module.

1. enter_normal_mode – 13h
2. enter_partial_mode – 12h
3. get_address_mode – 0Bh
4. get_pixel_format – 0Ch
5. get_scanline – 45h
6. read_memory_continue – 3Eh
7. read_memory_start – 2Eh
8. set_address_mode – 36h
9. set_column_address – 2Ah
10. set_page_address – 2Bh
11. set_partial_row – 30h
12. set_pixel_format – 3Ah
13. set_tear_off – 34h
14. set_tear_on – 35h
15. set_tear_scanline – 44h
16. write_memory_continue – 3Ch
17. write_memory_start – 2Ch

The following DCS commands are decoded in VTCM, but are mean for other module. They will output as vtc_sleep_mode (1 = sleep mode) and vtc_display_on (1 = display on).

1. enter_sleep_mode – 10h
2. exit_sleep_mode – 11h
3. set_display_off – 28h
4. set_display_on – 29h

There are certain DCS command bits that are not used in VTCM module. VTCM module will return the register setting that is previously programmed through DCS command interface.

1. Display Device Line Refresh Order (bit [4] of set_address_mode – 36h)
2. Display Data Latch Data Order (bit [2] of set_address_mode – 36h)
3. Flip Horizontal (bit [1] of set_address_mode – 36h)
4. Flip Vertical (bit [0] of set_address_mode – 36h)
5. DPI Pixel Format Definition (bit [6:4] of set_pixel_format – 3Ah)

Qualcomm Compression Command Support

Besides DCS commands, VTCM also responsible to decode some predefined Qualcomm FBC (Frame Buffer Compression) registers. Below are the registers that are defined under Qualcomm FBC Capability Exchange.

- ### Capability Exchange

The Frame Buffer Compression parameter are transmitted using a “generic short write” packet with dataID=0x23. This packet contains four bytes: DataID, register address, register parameter and an ECC byte.



Figure 7–2: Transmission of first capability exchange byte using DSI generic short write packet

The following parameters are for capability exchange. If only the first byte is sent (register 0xC0), then all remaining parameters may be initialized to default values.

Table 7-33: Bitplane for capability exchange

Capability Exchange									
Register Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
0xC0	Reserved [6:0]							FBC_ENABLE	0x01
0xC1	WIDTH [7:0]								0x80
0xC2	Reserved[4:0]				WIDTH [10:8]				0x07
0xC3	HEIGHT [7:0]								0x38
0xC4	Reserved[4:0]				HEIGHT [10:8]				0x04
0xC5	Reserved[1:0]		PAT_ENABLE	BFLC_ENABLE	TARGET_SIZE [3:0]				0x34
0xC6	LOSSY_RGB_THD [3:0]				EXTRA_BUDGET_LEVEL [3:0]				0x05
0xC7	Reserved[4:0]				LOSSY_Y_MODE_INDEX [2:0]				0x03

Note that registers PER_BLK_BURGET AND PER_LINE_EXTRA_BURGET are not required to transmit, since these can be computed from available information by the decoder. In addition, the register YUV_422 does not need to be transmitted, since this parameter is only required for the encoder.

For register address 0xC6, the special case for RGB PCM Lossy mode may be enabled using the LOSSY_RGB_THD register. This register defaults to 0 (disabled). If this features is enabled, the value LOSSY_RGB_THD=4 is recommended. In this case, register 0xC6 will be set to 0x45

- ### Profile ID

The profile ID is used to describe the capability of the decoder to AP. SSD2858 will transmit this profile ID to AP over DSI. Once AP receives the profile ID, FBC encoder parameter will be set based on the capability of SSD2858 decoder.

Currently, the profile ID uses two bits to describe the capability of the decoder to AP. Bit 0 is used for lossy RGB PCM mode and bit 1 is used for pattern mode. If the decoder supports lossy RGB PCM mode, then bit 0 should be set to 0b1. If the decoder supports pattern mode decoding, then bit 1 should be set to 0b0. Other bits in the profile ID are reserved for future use.

Table 7-34: Bitplane for Profile ID Byte

Profile ID									
Register Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
0xC8	Reserved [5:0]						PAT Mode	Lossy RGB PCM Mode	0x01

0: supported 1: not supported	←	←	←	←	←	←	←	←	←
									0: not supported 1: supported

Communication between SSD2858 and AP is demonstrated in Figure 7–3. First, AP transmit a **Set maximum return size** command (DataID=0x37) with value 1 to SSD2858. Next, AP transmits a **Generic read request** packet (DataID=0x14) with register 0xC8. SSD2858 will then respond with a **Generic read response** packet (DataID=0x11) containing the Profile ID byte.

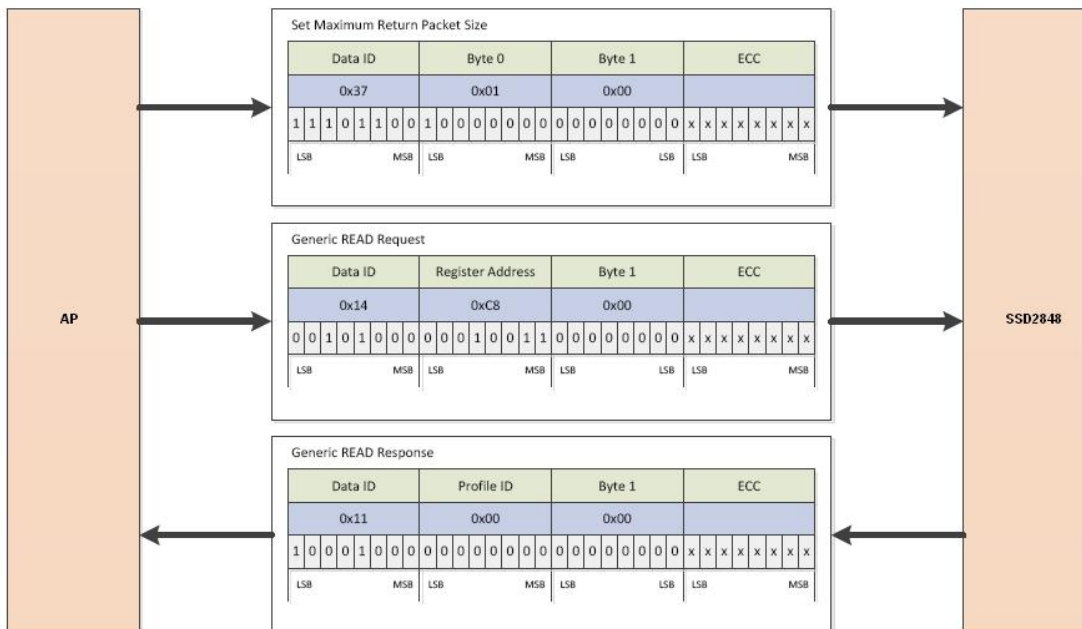


Figure 7–3: Communication between AP and SSD2858 for negotiating SSD2858’s Profile ID. In this example, SSD2858’s Profile ID is 0x00

- ### Transmission using DSI Video Mode Packets

The compressed bitstream can be transmitted from AP to SSD2858 using DSI Video Mode. In this case, video packets containing the compressed bitstream are transmitted along with Hsync, Vsync and blanking packets. Interface timing for DSI Video Mode is shown in Figure 7-4 with an example bitstream in Figure 7-5. The ordering of specific packets is shown in Figure 7-6 with a description of each packet type in Table 7-35.

As is also the case for DSI Command Mode, MIPI specifies that all bytes are transmitted LSB-first. This will be true for all DSI command packets. However, the compressed bitstream will be transmitted MSB-first. This is demonstrated in Figure 7-5. Notice that, for example, the Data ID byte (0x3E) is transmitted from least to most significant bits (0111 1100). In contrast, the first byte of the compressed bitstream (0x17) will be transmitted from most to least significant bit (0001 0111).

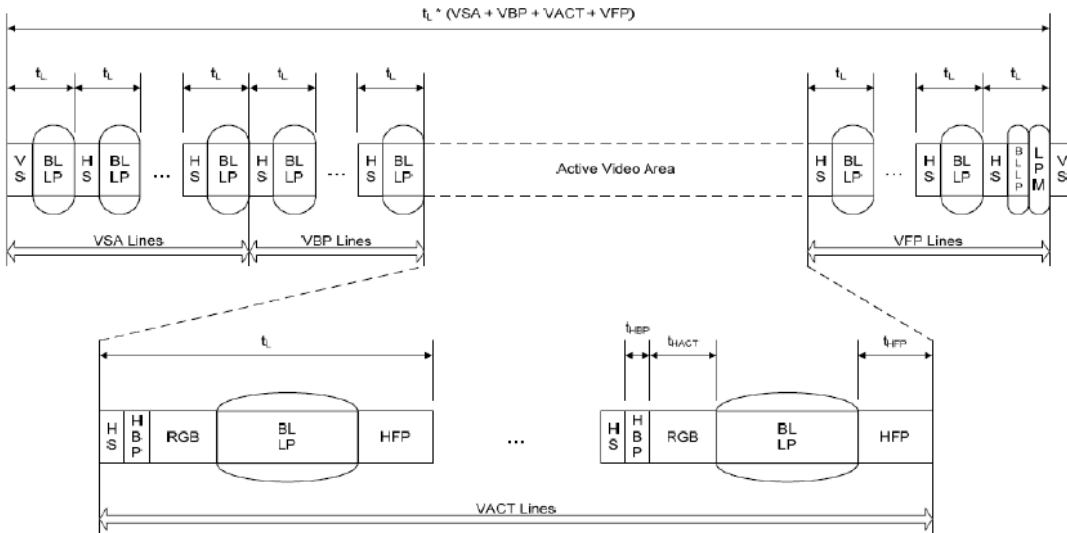


Figure 7-4: DSI video mode interface timing

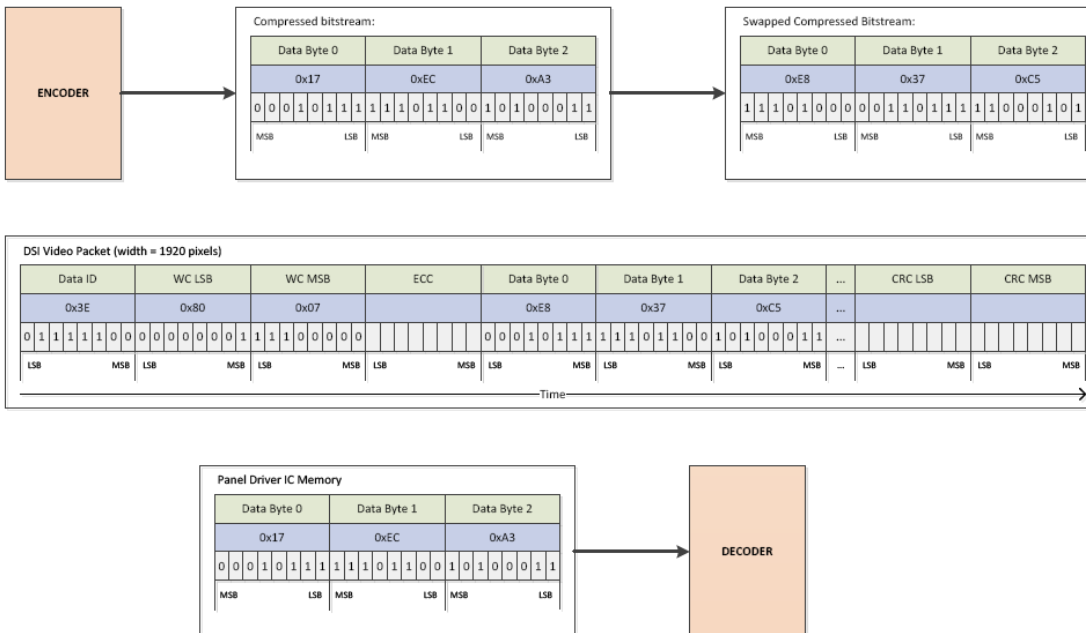


Figure 7-5: DSI Video Mode packet for line width of 1920 pixels. The first bit of the compressed bitstream will be the first bit received by SSD2858

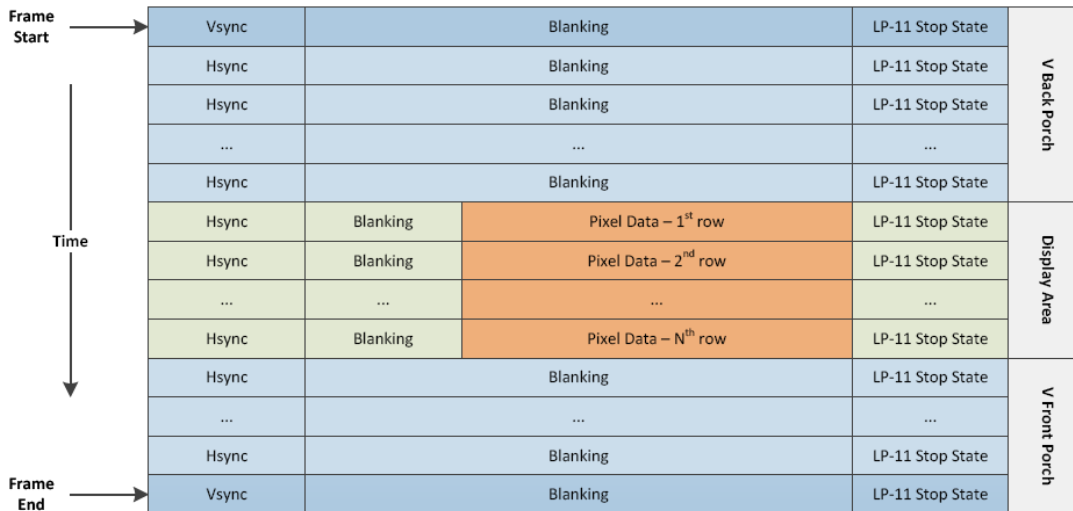


Figure 7–6: Packet Ordering for DSI Video Mode

Table 7-35: DSI Video Mode Packet Formats

Packet	Packet Type	Data ID	Payload (short packet) or Word Count (long packet)	ECC	Payload	CRC
Vsync	Short	0x01	Payload = 0x00, 0x00	Required	N/A	N/A
Hsync	Short	0x21	Payload = 0x00, 0x00	Required	N/A	N/A
Blanking	Long	0x19	Word Count	Required		Required
Pixel Data	Long	0x3E	Word Count	Required		Required

- ### Transmission using DSI Command Mode Packets

The compressed bitstream can be transmitted from AP to SSD2858 using DSI Command Mode. In this mode, each DSI header byte is transmitted LSB first. The compressed bitstream is transmitted MSB first as demonstrated in Figure 7–7. The data ID for a DSI command-mode packet is 0x39, and the long packet format is used. In addition to the compressed bitstream, one extra byte is included in the payload to specify whether the transmitted line is the first in the frame. This is the first byte in the payload (Data 0), and will be 0x2C for the first line in a frame, and 0x3C for any other line.

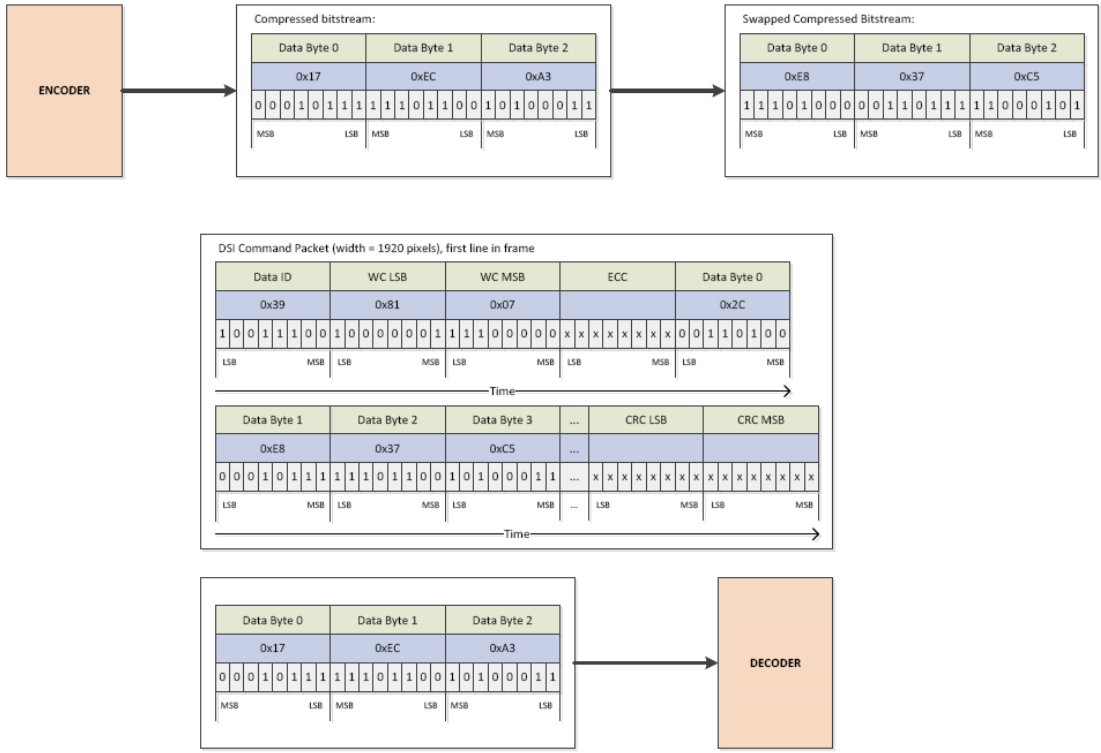


Figure 7–7: DSI Command Mode packet for line width of 1920 pixels. Data byte 0 = 0x2C for first line of the frame. The first bit of the compressed bitstream will be the first bit received by SSD2858

Operating Modes

Tearing

There are two different type of tear signal will be generated; from driver interface unit or data fetching unit. The selection is base on the TE_SEL (Tear Select) bit of VTCM Configuration Register. If TE_SEL is 0 then tear signal is from Data Fetching Unit is selected. If TE_SEL is 1 then tear signal is from Driver Interface Unit is selected.

Tear Signal Generated From Driver Interface Unit

Tear signal from Driver Interface Unit will be generated based on the following condition.

1. set_tear_on command is sent (Tear On = 1).
 - a. If tear_scanline is set to 0
 - i. If tear_mode is 0 (send set_tear_on command with M bit set to 0), tear signal will be generated on the vertical blanking period (non-display period).

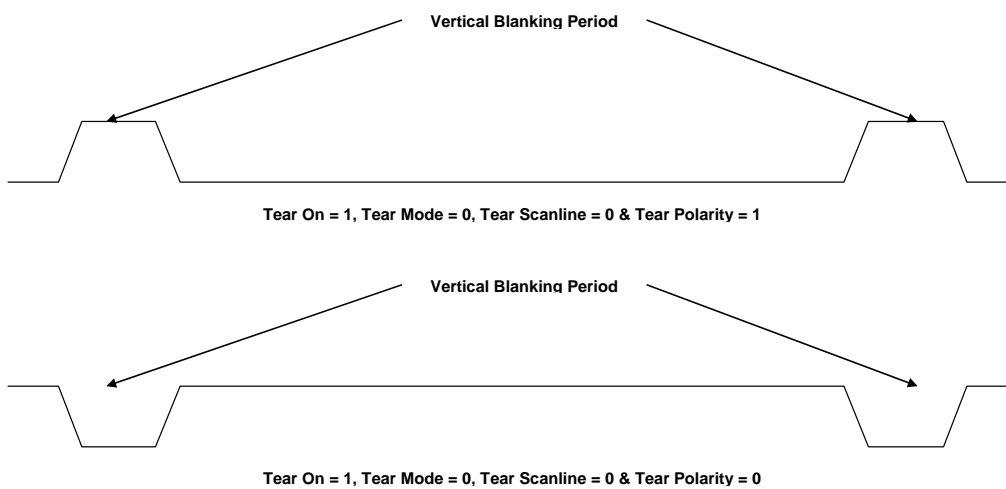


Figure 7-8: Tear On = 1, Tear Mode = 0 & Tear Scanline = 0

- ii. If tear_mode is 1 (send set_tear_on command with M bit set to 1), tear signal will be generated on the vertical blanking and horizontal blanking period (non-dispkay period)..

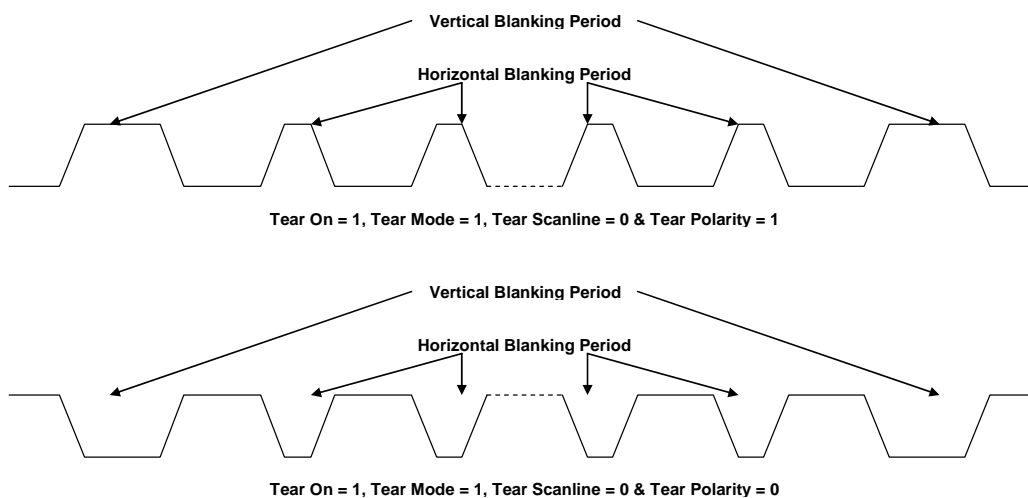


Figure 7-9: Tear On = 1, Tear Mode = 1 & Tear Scanline = 0

- b. If tear_scanline is set to greater than 0
 - i. Regardless of tear_mode setting, tear signal will be generated similar to Mode 0 except that the whole signal will be shift by number of line depend on tear_scanline value.

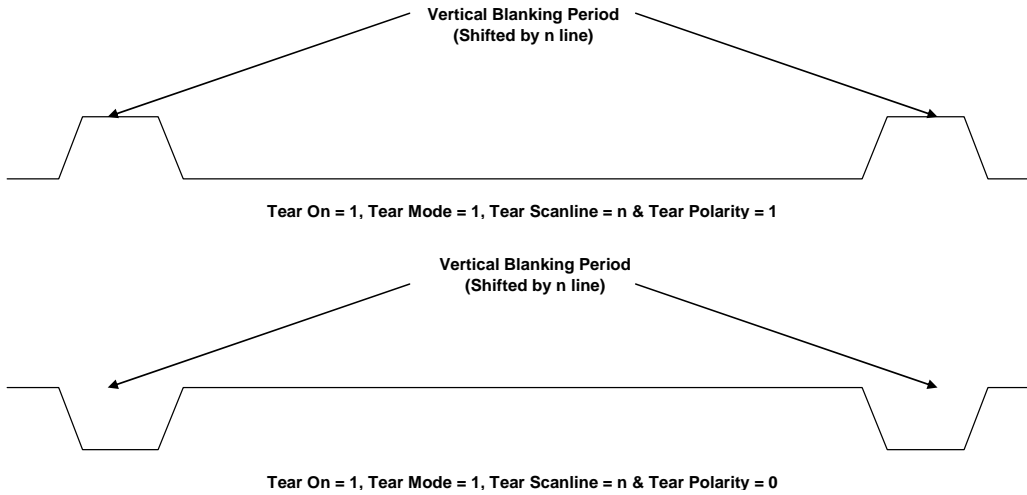


Figure 7-10: Tear On = 1, Tear Mode = 1 & Tear Scanline = n

- 2. set_tear_off command is sent (Tear On = 0), tear signal will be static to 1 or 0 depend on TEP (Tear Polarity) bit of VTCM Configuration Register.
 - a. If TEP = 1, then tear signal is set to 1.

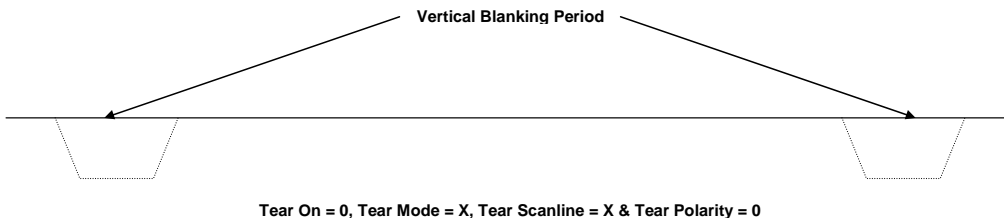


Figure 7-11: Tear On = 0, Tear Mode = X, Tear Scanline = X & Tear Polarity = 1

- b. If TEP = 0, then tear signal is set to 0 (default).

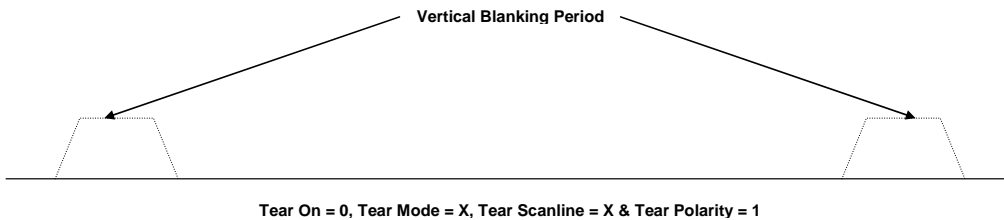


Figure 7-12: Tear On = 0, Tear Mode = X, Tear Scanline = X & Tear Polarity = 0

Tear Signal Generated From Data Fetching Unit

Tear signal from Data Fetching Unit will be generated only based on tear_on and TEP. It will be like following.

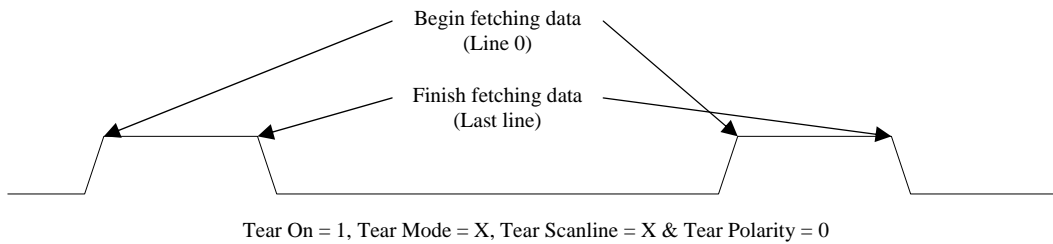


Figure 7-13: Tear On = 1, Tear Mode = X, Tear Scanline = X & Tear Polarity = 0

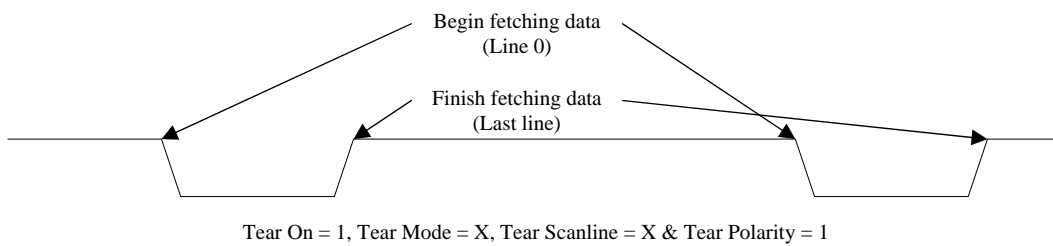


Figure 7-14: Tear On = 1, Tear Mode = X, Tear Scanline = X & Tear Polarity = 1

Please note that there is a pre-fetch mechanism in place for data fetching unit. Data fetching is happening 8 line before the first data valid is generated. Hence, using tear signal that is generated from data fetching unit is more accurate, but the drawback is it cannot shift like tear signal generated from driver interface unit.

Address Mode

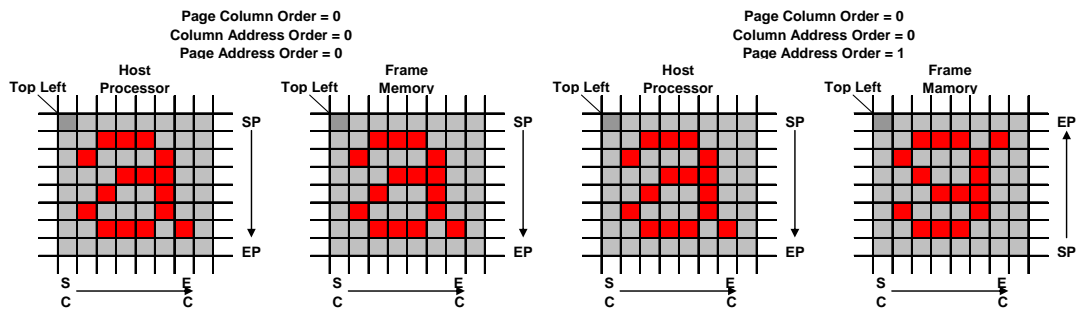


Figure 7-15: Page Address Order

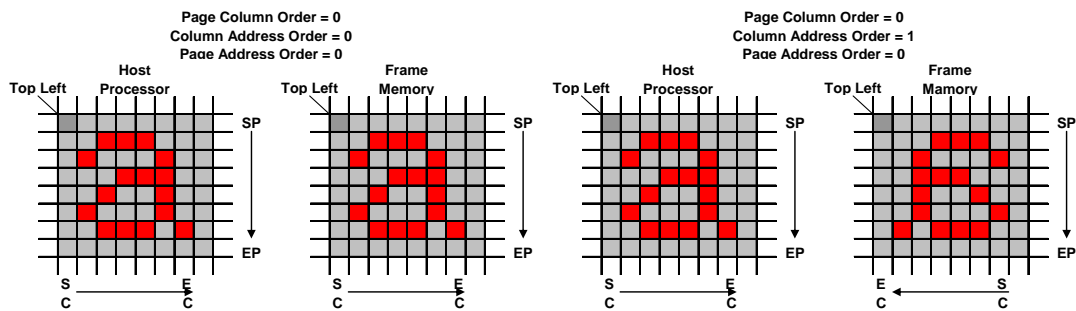
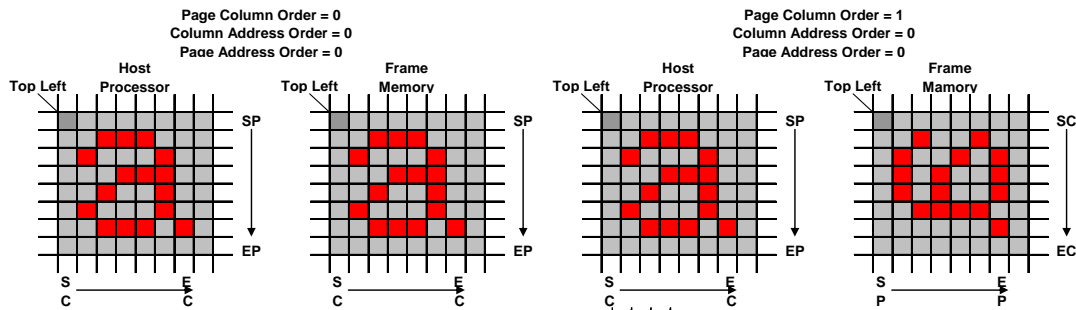


Figure 7-16: Column Address Order



Note : Column need to update in term of 4-pixel, this is due to the compressor/de-compressor is doing in 4-pixel segment

Figure 7-17: Page Column Order

Rotation 90°

The rotation mode are very similar to the Page Column Order, the only different is that it will perform data rotation when the frame data is read out from memory.

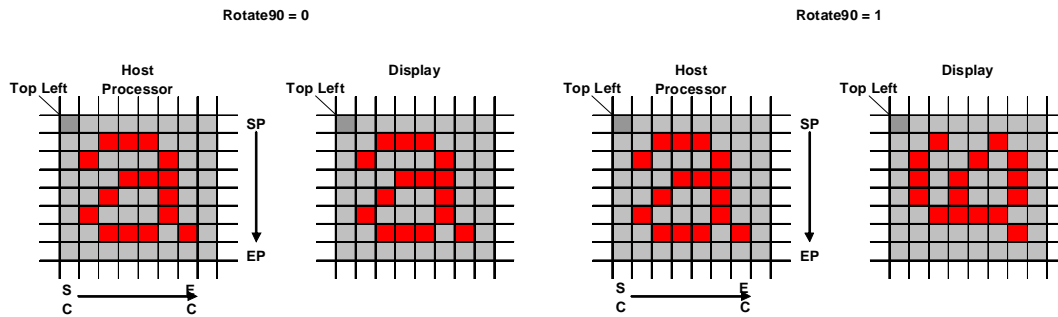


Figure 7-18: Rotate 90°

The data will be fetching from the top right column and down to the bottom right column, and then fetching the second column from the right and so on until it complete fetching till the first column on the left.

Partial Display

If End Row is set greater than or equal to Start Row then they will be a top and bottom black color bar on the display. When Start Row and End Row is both equal, then there will be one line display at Start Row or End Row position.

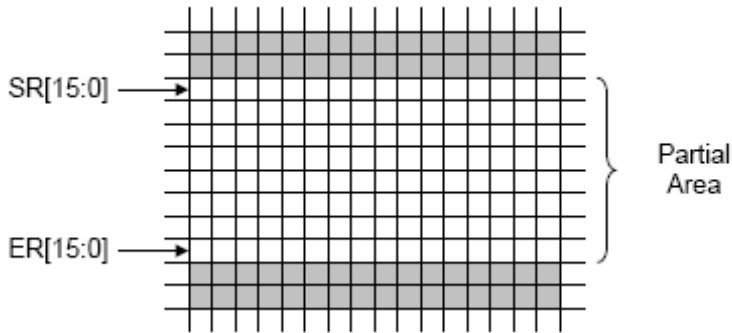


Figure 7-19: Partial Display with $ER \geq SR$

If Start Row is set greater than End Row then they will be black color bar at the middle of the display. When End Row is greater than Start Row + 1, then there is equal to disable the partial display.

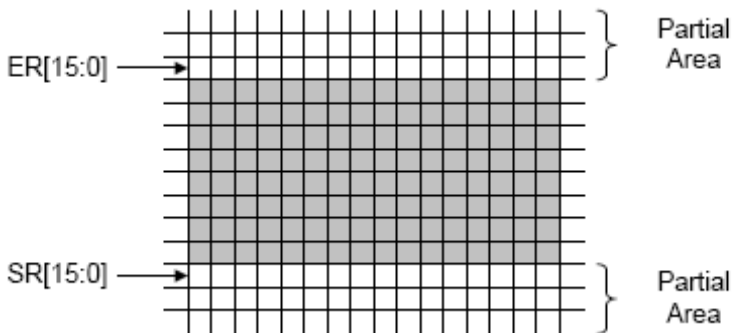


Figure 7-20: Partial Display with $SR > ER$

HSCA

HSCA performs cubic interpolation on the input line, and output variable number of samples per line depending on the scaling factor. See Section 4 for more information on the operation. HSCA uses an interpolation interval of 12-bit resolution and a sampling interval of 3-bit resolution. The cubic coefficients LUT is programmed before frame processing start and does not change within the frame operation. The filter coefficients [C0,C1,C2,C3] are applied to the 4-tap FIR as below.

$$Z = \text{CLIP}((T0 \cdot C0 + T1 \cdot C1 + T2 \cdot C2 + T3 \cdot C3 + 128) \gg 8)$$

where

T{0..3} = filter inputs <u,8,8,0>

C{0..3} = coefficients <s,10,10,0>

Z = filtered output

CLIP(X) = X < 0 ? 0 : (X > 255 ? 255 : X)

The table below highlights the configuration parameters of HSCA.

Table 7–36: HSCA Configuration Parameters

Term	Description	Value
owidth[12:0]	Output width, i.e. number of output samples.	0 to 8191
stepstart[24:0]	Start value to load into STEPCURR counter for each new line. stepstart[24:12] = fullpel stepstart[11:0] = subpel	0.0 to 8191.4095
stepsize[16:0]	Interpolation step size. stepsize[16:12] = fullpel stepsize[11:0] = subpel	0.0 to 31.4095
halign	Line preloading alignment.	0 to 1

The figure below is an algorithmic view of how **halign** is used to align the filter at various interpolation intervals given by STEPCURR. The first output sample is always given by **stepstart**, and thereafter as per interpolation algorithm given in Section 4.

VSCA

VSCA performs vertical cubic interpolation on the frame at line level, and output variable number of lines depending on the scaling factor. See section 4 for more information on the operation. As the processing is in raster order, the coefficients used for the cubic interpolation is the same for all samples within the same output line. VSCA uses an interpolation interval of 12-bit resolution and a sampling interval of 3-bit resolution. Like HSCA, the cubic coefficients LUT is programmed prior to starting frame operation.

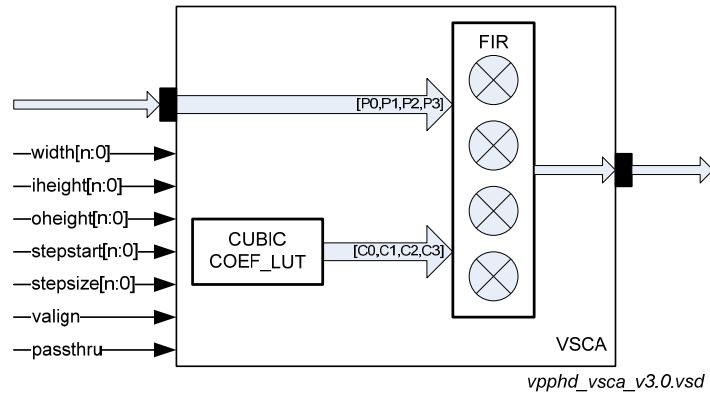


Figure 7–21: VSCA Functional Block Diagram

The filter coefficients `[C0,C1,C2,C3]` are applied to the 4-tap FIR as below.

```
Z = CLIP(( ( P0*C0 + P1*C1 + P2*C2 + P3*C3 + 128 ) >> 8 ))
```

where

```
P{0..3} = filter inputs <u,8,8,0>
```

```
C{0..3} = coefficients <s,10,10,0>
```

```
Z      = filtered output
```

```
CLIP(X) = X<0 ? 0:(X>255 ? 255:X)
```

The table below highlights the configuration parameters of VSCA.

Table 7–37: VSCA Configuration Parameters

Term	Description	Value
<code>width[12:0]</code>	width, i.e. number of samples per line.	0 to 8191
<code>iheight[11:0]</code>	input height, i.e. number of input lines.	0 to 4095
<code>oheight[11:0]</code>	output height, i.e. number of output lines.	0 to 4095
<code>stepstart[24:0]</code>	Start value to load into STEPCURR counter for each new line. stepstart[24:12] = fullpel stepstart[11:0] = subpel	0.0 to 8191.4095
<code>stepsize[16:0]</code>	Interpolation step size.	0.0 to

Term	Description	Value
	stepsize[16:12] = fullpel stepsize[11:0] = subpel	31.4095
valign	Frame preloading alignment.	0 to 1

The usage of **valign** in VSCA has the same analogy as **halign** HSCA. The filter operation is bypassed when **passthru** is asserted.

halign = 0				STEPCURR Range	halign = 1			
T3	T2	T1	T0		T3	T2	T1	T0
p1	p0	p0	p0	[0.0, 1.0)	p2	p1	p0	p0
p2	p1	p0	p0	[1.0, 2.0)	p3	p2	p1	p0
p3	p2	p1	p0	[2.0, 3.0)	p4	p3	p2	p1
p4	p3	p2	p1	[3.0, 4.0)	p5	p4	p3	p2
p5	p4	p3	p2	[4.0, 5.0)	p6	p5	p4	p3
...						
pN-2	pN-3	pN-4	pN-5	[(N-3).0, (N-2).0)	pN-1	pN-2	pN-3	pN-4
pN-1	pN-2	pN-3	pN-4	[(N-2).0, (N-1).0)	pN-1	pN-1	pN-2	pN-3
pN-1	pN-1	pN-2	pN-3	[(N-1).0, (N).0)	pN-1	pN-1	pN-1	pN-2
pN-1	pN-1	pN-1	pN-2	[(N).0, (N+1).0)	pN-1	pN-1	pN-1	pN-1
pN-1	pN-1	pN-1	pN-1	[(N+1).0, ∞)	pN-1	pN-1	pN-1	pN-1

vpphd_hsca_halign_v1.0.vsd

Figure 7–22: HSCA Filter Alignment - Halign

The filter operation is bypassed when **passthru** is asserted.

VPPHD Scaling Algorithm

This section provides an overview and background on the scaling algorithm employed in VPPHD. Scaling in both horizontal and vertical directions is the same. The material hereon will describe scaling in horizontal direction, but the same inference can be made for scaling in the vertical direction, with sample row replaced by sample column.

- **Interpolation Basic**

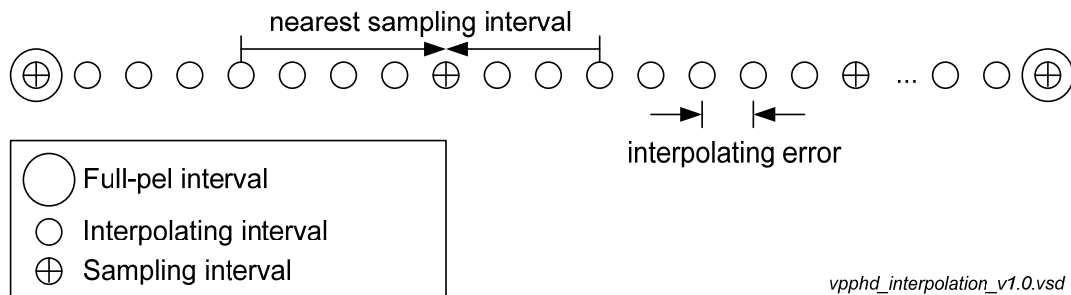


Figure 7–23: Fixed Point Interpolation

In non-integer scaling, it is required to create a new sample between two given samples. This is also generally known as resampling. Given a line of samples, these samples are termed to be located at full-pel (full pixel) position, i.e. the interval of these samples is taken as integer for reference. To obtain a new sample between two full-pel, the following is performed:

- Divide the interval between the two full-pel into 2^N intervals for interpolation purpose; these are called interpolation intervals. N is the resolution of the interpolation interval.
- Divide the interval between the two full-pel into 2^K intervals for resampling purpose ($K \leq N$); these are called sampling intervals. K is the resolution of the sampling interval.
- Derive at which interpolation interval the new sample should be. Typically this involves converting from a floating point value. The error incurred from this conversion is the interpolation error.
- If ($K = N$), the sampling interval is co-located with the interpolation interval. If ($K < N$), the sampling interval is obtained by round-off (round-half-up) the interpolation interval (see Figure above). Generally $K < N$ in order to reduce the size of the filter kernel. The smaller the filter kernel, the lesser the filter coefficients.
- The new sample value is obtained by applying a filter operation with the nearest X full-pel, X depending on exact algorithm. Generally the larger the X the better the estimation/interpolation. The filter coefficients to be used are dependent on the sampling interval obtained in step [d].

- ## Scaling Operation

The following quantities are defined:

Table 7–38: Scaling Terms

Term	Description
STEPCURR	Current step count.
STEP SIZE	Equivalent to the inversed scaling factor.
STEPSTART	Start value of stepcurr.
P(i)	Sample at fullpel location <i>.0.
LUT(s)	Look-up table of coefficient at index s. The number of entries depends on the resolution of sampling interval.
[C0,C1,C2,C3]	A set of cubic filter coefficients.

The following describes in general the process of scaling a given line to a new line with more or less samples (or even equal samples):

- Initialise STEPCURR to STEPSTART.
- Fullpel value of STEPCURR gives the nearest left sample P(i). The subpel value of STEPCURR gives the interpolation interval between P(i) and P(i+1). Round-off the interpolation interval to determine the sampling interval, Ts.
- Obtain the filter coefficients to use by indexing LUT with Ts, i.e. LUT(Ts)
- Obtain the new sample by applying filter operation with coefficients obtained in [c] to X nearest full-pel samples. For X=4, these will be {P(i-1), P(i), P(i+1), P(i+2)}. If any of the sample falls outside the line, the border sample is used instead, e.g. {P(-1), P(0), P(1), P(2)} → {P(0), P(0), P(1), P(2)}.
- Increment STEPCURR by STEP SIZE.
- Repeat [b] to [e] until the required number of new samples is obtained.

VPPHD Cubic Interpolation

VPPHD employs cubic interpolation (i.e. $X=4$), with $N=12$ -bit interpolation resolution, and $K=3$ -bit sampling resolution. The number of phases in the poly phase filter is $2^K = 8$. A straight forward implementation of the LUT is to use 8 entries, one entry for each phase.

However because the cubic kernel is symmetric about DC, the LUT can be optimised to use $(2^{K-1}+1) = 5$ entries, as shown below.

<p>LUT index = T_s when $0 \leq T_s \leq (2^{K-1})$ else -- (1)</p> <p> $(2^K)-T_s$ when $(2^{K-1}) < T_s \leq (2^K)-1$ -- (2)</p> <p>For case (2), the coefficients need to be reflected before applying to FIR, i.e.</p> <p>$C'0 = C3$</p> <p>$C'1 = C2$</p> <p>$C'2 = C1$</p> <p>$C'3 = C0$</p> <p>C' should be used instead of C for (2).</p>

The tables below gives the organization and programming view of the LUT. $FK[0..16]$ is the filter kernel impulse response.

Table 7–39: LUT Organization

Index T_s	C0	C1	C2	C3
0	FK[8]	FK[0]	FK[8]	FK[16]
1	FK[9]	FK[1]	FK[7]	FK[15]
2	FK[10]	FK[2]	FK[6]	FK[14]
3	FK[11]	FK[3]	FK[5]	FK[13]
4	FK[12]	FK[4]	FK[4]	FK[12]

Table 7–40: LUT Programming View

Index T_s	C0	C1	C2	C3
0	LUT[0]		LUT[1]	
1	LUT[2]		LUT[3]	
2	LUT[4]		LUT[5]	
3	LUT[6]		LUT[7]	
4	LUT[8]		LUT[9]	

8 Video Compression Unit (VCU)

Features

This module is mainly used to compress the video data into compressed video data in order to save bandwidth. Video data can be encoded using either SSL compression algorithm or Qualcomm compression algorithm. Registers are used to program the compression settings and monitor the compression process (for Qualcomm compression only).

References

- Qualcomm Frame Buffer Compression Algorithm and Design Document – Aug 31, 2012
- AMBA Specification – Rev 2.0 – May 13, 1999

Limitations

- The total number of input pixels per line is required to be even number.
- For Qualcomm compression algorithm, registers *VCU_QFBCCTRLR*, *VCU_QFBCSZR*, *VCU_QFBCCFGR*, *VCU_QFBCCTRL2R* and *VCU_QFBCCTRL3R* should be programmed before video data transmission. Programming of registers during the transmission is NOT allowed.

Programming Model

All reserved bits return zero on read and shall always be written with zero. Writing any other value to a reserved bit will result in indeterminate behavior. Registers are programmed using APB interface.

Table 8–1: VCU APB Register Summary

Offset	Name	Mnemonic	Reset Value
0x0000	VCU Device Identification Register	VCU_IDR	0x04800000
0x0004	VCU Capabilities Register	VCU_CAPR	TBD
0x0008	VCU Horizontal Display Configuration Register	VCU_HDCFGR	0x00000001
0x000C	VCU Qualcomm FBC Control Register	VCU_QFBCCTRLR	0x00000001
0x0010	VCU Qualcomm FBC Size Register	VCU_QFBCSZR	0x04380780
0x0014	VCU Qualcomm FBC Configuration Register	VCU_QFBCCFGR	0x00034534
0x0018	VCU Qualcomm FBC Control 2 Register	VCU_QFBCCTRL2R	0x00000005
0x001C	VCU Qualcomm FBC Control 3 Register	VCU_QFBCCTRL3R	0x02008000
0x0020	VCU Qualcomm FBC Status Register	VCU_QFBCSTSR	0x00000000

Register Description

VCU Device Identification Register

VCU_IDR		VCU Identification Register							Offset Address
									0x0000
BIT	31	30	29	28	27	26	25	24	
NAME	CLID[15:8]								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16	
NAME	CLID[7:0]								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8	
NAME	DSGNR[5:0]						MJR[3:2]		
TYPE	RO								
RESET	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0	
NAME	MJR[1:0]		MNR[5:0]						
TYPE	RO								
RESET	0	0	0	0	0	0	0	0	

Table 8-2: VCU Device Identification Register Description

Name	Description	Setting
CLID[15:0] Bit 31-16	<Device Class Name> – Based on PCI Device Class Name	0x0480
DSGNR[5:0] Bit 15-10	Design Number – This is a 0 counted design number administered by SSL Technical Committee for IP designs.	0x00
MJR[3:0] Bit 9-6	Major Revision Number	0x1
MNR[5:0] Bit 5-0	Minor Revision Number	0x00

VCU Capabilities Register

Offset Address

VCU_CAPR

VCU Capabilities Register

0x0004

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0

Table 8-3: VCU Capabilities Register Description

Name	Description	Setting
Reserved Bit 31–0	Reserved	

VCU Horizontal Display Configuration Register

Offset Address

VCU_HDCFGR VCU Display Horizontal Configuration Register 0x0008

BIT	31	30	29	28	27	26	25	24	
NAME									
TYPE	RO	RO	RO	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16	
NAME									
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8	
NAME				MHBP[12:8]					
TYPE	RO	RO	RO	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0	
NAME	MHBP[7:0]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	1	

Table 8-4: VCU Display Horizontal Configuration Register Description

Name	Description	Setting
Reserved Bit 31-13	Reserved	
MHBP Bit 12-0	Minimum Horizontal Back Porch – These bits define the minimum horizontal back porch of the output video data.	0-8192

VCU Qualcomm FBC Control Register

VCU_QFBCCTRLR								VCU Qualcomm FBC Control Register		Offset Address
										0x000C
BIT	31	30	29	28	27	26	25	24		
NAME									NON_INT_BIAS[9:8]	
TYPE	RO	RO	RO	RO	RO	RO	RW	RW		
RESET	0	0	0	0	0	0	0	0		
BIT	23	22	21	20	19	18	17	16		
NAME	NON_INT_BIAS[7:0]									
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8		
NAME	OPMODE	PADDING	BFLC_ALLOWED							
TYPE	RW	RW	RW	RO	RO	RO	RO	RO		
RESET	0	0	0	0	0	0	0	0		
BIT	7	6	5	4	3	2	1	0		
NAME			COM_MODE[1:0]						FBC_ENABLE	
TYPE	RW	RW	RW	RW	RO	RO	RO	RO	RW	
RESET	0	0	0	0	0	0	0	0	1	

Table 8-5: VCU Qualcomm FBC Control Register Description

Name	Description	Setting
Reserved Bit 31–26	Reserved	
NON_INT_BIAS Bit 25-16	Reserved	
OPMODE Bit 15	Operation Mode – This bit selects the Qualcomm compression mode	0 = Lossless + Lossy 1 = Lossless only
PADDING Bit 14	Padding Enable – This bit enables the padding for compressed video data for Qualcomm compression.	0 = Disabled 1 = Enabled
BFLC_ALLOWED Bit 13	BFLC Allowed – This bit enables the bflc mode encoding for Qualcomm compression	0 = Disabled 1 = Enabled
Reserved Bit 12-6	Reserved	
COM_MODE Bit 5-4	Compressor Mode – These bits select the compressor use for write data to frame buffer.	00 = Bypass compressor 01 = SSL compressor select. 10 = Qualcomm compressor select. 11 = Select the following compression algorithm. Write (48 bits to 24 bits) : write MSB of the pixels: B[23:20],B[15:12],B[7:4], into

		the RAM
Reserved Bit 3–1	Reserved	
FBC_ENABLE Bit 0	FBC Enable – This bit enable FBC.	0 = Disabled 1 = Enabled

VCU Qualcomm FBC Size Register

Offset Address

VCU_QFBCSZR

VCU Qualcomm FBC Size Register

0x0010

BIT	31	30	29	28	27	26	25	24
NAME	HEIGHT[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	0	0
BIT	23	22	21	20	19	18	17	16
NAME	HEIGHT[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	1	1	1	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	WIDTH[12:8]							
TYPE	RO	RO	RO	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	1	1	1
BIT	7	6	5	4	3	2	1	0
NAME	WIDTH[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	1	0	0	0	0	0	0	0

Table 8-6: VCU Qualcomm FBC Size Register Description

Name	Description	Setting
Reserved Bit 31–29	Reserved	
HEIGHT Bit 28-16	Height – These bits set the frame height.	0–8192
Reserved Bit 15–13	Reserved	
HEIGHT Bit 12-0	Width – These bits set the frame width.	0–8192

VCU Qualcomm FBC Configuration Register

Offset Address

VCU_QFBCCFGR

VCU Qualcomm FBC Configuration Register

0x0014

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME						LOSSY_Y_MODE_INDEX[2:0]		
TYPE	RO	RO	RO	RO	RO	RW	RW	RW
RESET	0	0	0	0	0	0	1	1
BIT	15	14	13	12	11	10	9	8
NAME	LOSSY_RGB_THD[3:0]				EXTRA_BUDGET_LEVEL[3:0]			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	1	0	0	0	1	0	1
BIT	7	6	5	4	3	2	1	0
NAME			PATTERN_ENABLE	BFLC_ENABLE	TARGET_SIZE[3:0]			
TYPE	RO	RO	RW	RW	RW	RW	RW	RW
RESET	0	0	1	1	0	1	0	0

Table 8-7: VCU Qualcomm FBC Configuration Register Description

Name	Description	Setting
Reserved Bit 31–3	Reserved	
LOSSY_MODE_Y_INDEX Bit 18–16	Lossy Mode Y Index – LUT index for lossy_y_bits vector.	0-7
Reserved Bit 15	Reserved	
LOSSY_RGB_THD Bit 15–12	Lossy RGB Threshold – If chroma block decision is 444 for a block, and number of chroma bits per pixel is less than this register, use RGB space rather than YC ₀ C _g space (set to 0 to disable).	0-6
EXTRA_BUDGET_LEVEL Bit 11–8	Extra Budget Level – Extra budget for early blocks in each line or frame. Increased chance of lossless block at cost of uniformity.	0-9
Reserved Bit 7–6	Reserved	
PATTERN_ENABLE Bit 5	Pattern Enable – This bit enable pattern.	0 = Disabled 1 = Enabled
BFLC_ENABLE Bit 4	BFLC Enable – This bit enable BFLC.	0 = Disabled 1 = Enabled
TARGET_SIZE Bit 3–0	Target Size – These bits select the target size.	0 = 8/24 1 = 9/24 ...

		10 = 18/24
--	--	------------

VCU Qualcomm FBC Control 2 Register

Offset Address

VCU_QFBCCTRL2R

VCU Qualcomm FBC Control 2 Register

0x018

BIT	31	30	29	28	27	26	25	24
NAME	PER_LINE_EXTRA_BUDGET[11:8]							
TYPE	RO	RO	RO	RO	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME	PER_LINE_EXTRA_BUDGET[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME	PER_BLK_BUDGET[7:0]							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	YUV_422							VLC_ENABLE
TYPE	RO	RO	RO	RO	RW	RW	RW	RW
RESET	0	0	0	0	0	1	0	1

Table 8-8: VCU Qualcomm FBC Control 2 Register Description

Name	Description	Setting
Reserved Bit 31–28	Reserved	
PER_LINE_EXTRA_BUDGET Bit 27-16	Per Line Extra Budget – Additional bit budget or each line (increased chance of lossless blocks at the beginning of the line).	0-2304
PER_BLK_BUDGET Bit 15-8	Per Block Budget – Bit budget for each block.	0-192
Reserved Bit 7–4	Reserved	
YUV_422 Bit 3-1	YUV 422 – Bias for chroma subsampling.	0-5 0 = favor 444 5 = favor 422
VLC_ENABLE Bit 0	VLC Enable – This bit enable VLC.	0 = Disabled 1 = Enabled

VCU Qualcomm FBC Control 3 Register

VCU_QFBCCTRL3R							VCU Qualcomm FBC Control 3 Register		Offset Address
									0x001C
BIT	31	30	29	28	27	26	25	24	
NAME							LOSSLESS_MODE_THD [9:8]		
TYPE	RO	RO	RO	RO	RO	RO	RW	RW	
RESET	0	0	0	0	0	0	1	0	
BIT	23	22	21	20	19	18	17	16	
NAME	LOSSLESS_MODE_THD[7:0]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8	
NAME	LOSSY_MODE_THD[7:0]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	1	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0	
NAME								CALC_422 QUANT_EN	
TYPE	RO	RO	RO	RO	RO	RO	RO	RW	
RESET	0	0	0	0	0	0	0	0	

Table 8-9: VCU Qualcomm FBC Control 3 Register Description

Name	Description	Setting
Reserved Bit 31–28	Reserved	
LOSSLESS_MODE_THD Bit 25-16	Lossless Mode Threshold – If the bit budget exceeds this register, then blocks can be encoded in lossless mode, even if the block requires more than MAX_LOSSLESS_BITS_PER_PX bits.	128-1023
LOSSY_MODE_THD Bit 15-8	Lossy Mode Threshold – Maximum bits for a lossless block.	128-192
Reserved Bit 7–1	Reserved	
CALC_422_QUANT_EN Bit 0	Calculate 422 Quantization Enable – Calculate quantization error in addition to interpolation error for making 422/444 chroma decision.	0 = Disabled 1 = Enabled

VCU Qualcomm FBC Status Register

Offset Address

VCU_QFBCSTSR

VCU Qualcomm FBC Status Register

0x0020

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME							DATA_OVR	LOSSY_STAT
TYPE	RO	RO	RO	RO	RO	RO	RW1C	RW1C
RESET	0	0	0	0	0	0	0	0

Table 8-10: VCU Qualcomm FBC Status Register Description

Name	Description	Setting
Reserved Bit 31–2	Reserved	
DATA_OVR Bit 1	Data Overrun – This bit indicate compressor data overrun detected.	0 = Compressor data overrun not detected 1 = Compressor data overrun detected
LOSSY_STAT US Bit 0	Lossy Status – This bit indicate lossy compression detected.	0 = Lossy Compression not detected 1 = Lossy Compression detected

9 General Purpose I/O (GPIO)

References

Pin Table Chapter

Introduction

The General Purpose Input/Output (GPIO) module provides six I/O ports. Each port is 32-bit and may be programmed as either input or output. It can be multiplexed with other dedicated functions. This allows the user to make use of the same I/O pads for alternative functions on the chip.

Features

The features of the GPIO include:

- Six 32-bit ports with programmable direction-configurable pins
 - For SSD2858, there are only 18 I/O pins, so only one 18-bit port (GPIO_0) is used.
- Four different sources for each output with three functional outputs from internal modules and one from the data register
- Input data can be sampled into a data register
- Input can be configured to logic 1 or 0 to ensure transitions are ignored
- Input interrupt can be triggered on rising-edge, falling-edge, or level sensitive
- Interrupts can be masked using 32-bit mask register at bit level or at port level

Architecture

Overview

The GPIO module provides general purpose I/O capability to the device. Each I/O can be programmed as an input or output. The GPIO has a register to allow programmability to select between the primary or alternative functions. The GPIO provides input to two alternative destinations and three alternative sources can be selected for the output.

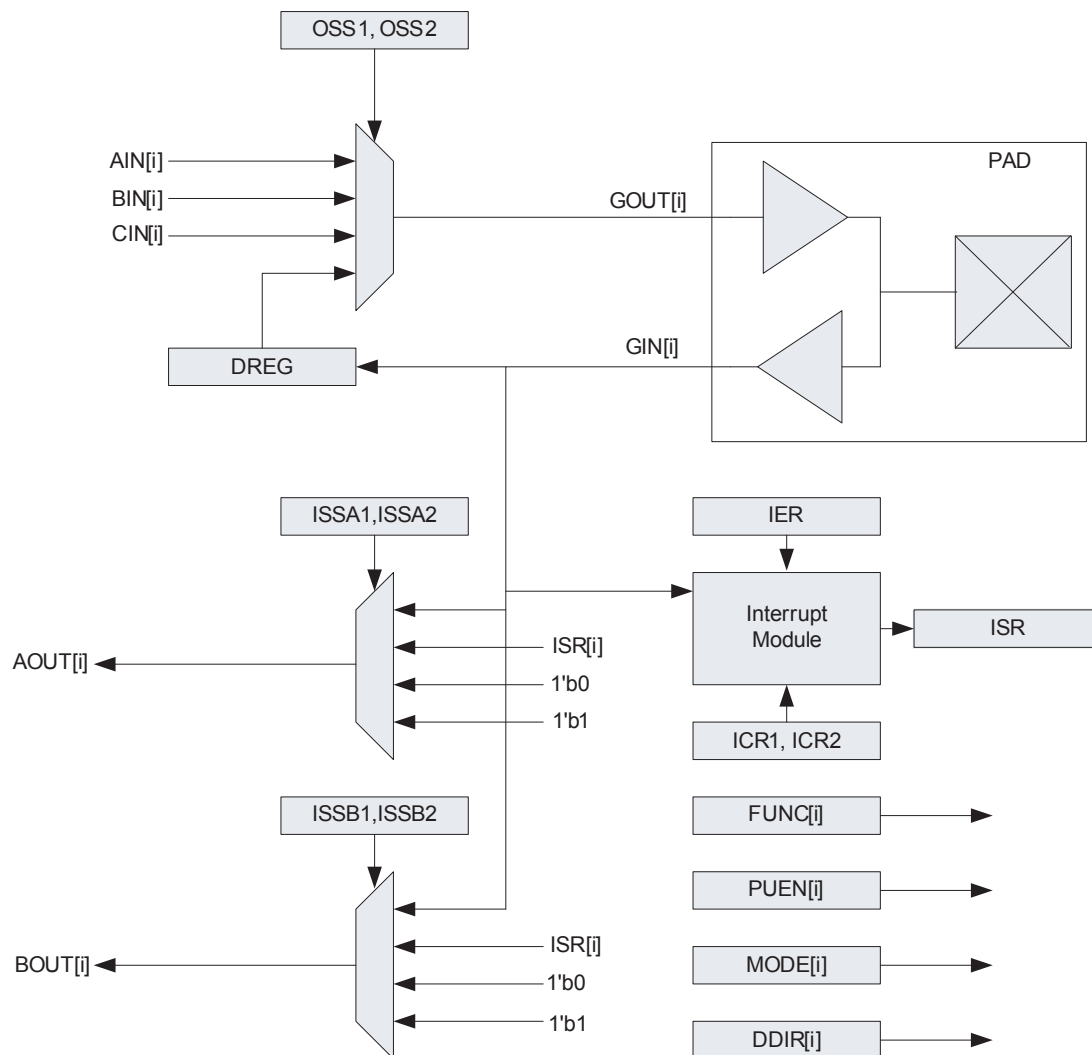


Figure 9-1: GPIO Port Muxing Diagram

Programming Model

Table 9-1: GPIO Register Summary

Offset	Name	Mnemonic	Reset Value
0x0000	GPIO Device Identification Register	GPIO_IDR	0x08100042
0x0004	GPIO Capabilities Register	GPIO_CAPR	0x00000000
0x0010	GPIO Control Register	GPIO_0_CTRL	0x00000000
0x0014	GPIO Function Register	GPIO_0_FUNC	0x00000000
0x0018	GPIO Mode Register	GPIO_0_GIUS	0x00000000
0x001C	GPIO Pull Enable Register	GPIO_0_PUEN	0xFFFFFFFF
0x0020	GPIO Data Direction Register	GPIO_0_DDIR	0x00000000
0x0024	GPIO Output Source Select Register 1	GPIO_0_OCR1	0x00000000
0x0028	GPIO Output Source Select Register 2	GPIO_0_OCR2	0x00000000
0x002C	GPIO Input Source Select A Register 1	GPIO_0_ICA1	0x00000000
0x0030	GPIO Input Source Select A Register 2	GPIO_0_ICA2	0x00000000
0x0034	GPIO Input Source Select B Register 1	GPIO_0_ICB1	0x00000000
0x0038	GPIO Input Source Select B Register 2	GPIO_0_ICB2	0x00000000
0x003C	GPIO Data Register	GPIO_0_DREG	0x00000000
0x0040	GPIO Interrupt Configuration Register 1	GPIO_0_ICR1	0x00000000
0x0044	GPIO Interrupt Configuration Register 2	GPIO_0_ICR2	0x00000000
0x0048	GPIO Interrupt Enable Register	GPIO_0_IMR	0x00000000
0x004C	GPIO Interrupt Status Register	GPIO_0_ISR	0x00000000
0x0050	GPIO Pull Select Register	GPIO_0_PUSE	0xFFFFFFFF
0x0110	GPIO Control Register	GPIO_1_CTRL	0x00000000
0x0114	GPIO Function Register	GPIO_1_FUNC	0x00000000
0x0118	GPIO Mode Register	GPIO_1_GIUS	0x00000000
0x011C	GPIO Pull Enable Register	GPIO_1_PUEN	0xFFFFFFFF
0x0120	GPIO Data Direction Register	GPIO_1_DDIR	0x00000000
0x0124	GPIO Output Source Select Register 1	GPIO_1_OCR1	0x00000000
0x0128	GPIO Output Source Select Register 2	GPIO_1_OCR2	0x00000000
0x012C	GPIO Input Source Select A Register 1	GPIO_1_ICA1	0x00000000
0x0130	GPIO Input Source Select A Register 2	GPIO_1_ICA2	0x00000000
0x0134	GPIO Input Source Select B Register 1	GPIO_1_ICB1	0x00000000
0x0138	GPIO Input Source Select B Register 2	GPIO_1_ICB2	0x00000000
0x013C	GPIO Data Register	GPIO_1_DREG	0x00000000
0x0140	GPIO Interrupt Configuration Register 1	GPIO_1_ICR1	0x00000000
0x0144	GPIO Interrupt Configuration Register 2	GPIO_1_ICR2	0x00000000
0x0148	GPIO Interrupt Enable Register	GPIO_1_IMR	0x00000000
0x014C	GPIO Interrupt Status Register	GPIO_1_ISR	0x00000000
0x0150	GPIO Pull Select Register	GPIO_1_PUSE	0x00000000
0x0210	GPIO Control Register	GPIO_2_CTRL	0x00000000
0x0214	GPIO Function Register	GPIO_2_FUNC	0x00000000
0x0218	GPIO Mode Register	GPIO_2_GIUS	0x00000000
0x021C	GPIO Pull Enable Register	GPIO_2_PUEN	0xFFFFFFFF
0x0220	GPIO Data Direction Register	GPIO_2_DDIR	0x00000000

0x0224	GPIO Output Source Select Register 1	GPIO_2_OCR1	0x00000000
0x0228	GPIO Output Source Select Register 2	GPIO_2_OCR2	0x00000000
0x022C	GPIO Input Source Select A Register 1	GPIO_2_ICA1	0x00000000
0x0230	GPIO Input Source Select A Register 2	GPIO_2_ICA2	0x00000000
0x0234	GPIO Input Source Select B Register 1	GPIO_2_ICB1	0x00000000
0x0238	GPIO Input Source Select B Register 2	GPIO_2_ICB2	0x00000000
0x023C	GPIO Data Register	GPIO_2_DREG	0x00000000
0x0240	GPIO Interrupt Configuration Register 1	GPIO_2_ICR1	0x00000000
0x0244	GPIO Interrupt Configuration Register 2	GPIO_2_ICR2	0x00000000
0x0248	GPIO Interrupt Enable Register	GPIO_2_IMR	0x00000000
0x024C	GPIO Interrupt Status Register	GPIO_2_ISR	0x00000000
0x0250	GPIO Pull Select Register	GPIO_2_PUSE	0x00000000
0x0310	GPIO Control Register	GPIO_3_CTRL	0x00000000
0x0314	GPIO Function Register	GPIO_3_FUNC	0x00000000
0x0318	GPIO Mode Register	GPIO_3_GIUS	0x00000000
0x031C	GPIO Pull Enable Register	GPIO_3_PUEN	0xFFFFFFFF
0x0320	GPIO Data Direction Register	GPIO_3_DDIR	0x00000000
0x0324	GPIO Output Source Select Register 1	GPIO_3_OCR1	0x00000000
0x0328	GPIO Output Source Select Register 2	GPIO_3_OCR2	0x00000000
0x032C	GPIO Input Source Select A Register 1	GPIO_3_ICA1	0x00000000
0x0330	GPIO Input Source Select A Register 2	GPIO_3_ICA2	0x00000000
0x0334	GPIO Input Source Select B Register 1	GPIO_3_ICB1	0x00000000
0x0338	GPIO Input Source Select B Register 2	GPIO_3_ICB2	0x00000000
0x033C	GPIO Data Register	GPIO_3_DREG	0x00000000
0x0340	GPIO Interrupt Configuration Register 1	GPIO_3_ICR1	0x00000000
0x0344	GPIO Interrupt Configuration Register 2	GPIO_3_ICR2	0x00000000
0x0348	GPIO Interrupt Enable Register	GPIO_3_IMR	0x00000000
0x034C	GPIO Interrupt Status Register	GPIO_3_ISR	0x00000000
0x0350	GPIO Pull Select Register	GPIO_3_PUSE	0x00000000
0x0410	GPIO Control Register	GPIO_4_CTRL	0x00000000
0x0414	GPIO Function Register	GPIO_4_FUNC	0x00000000
0x0418	GPIO Mode Register	GPIO_4_GIUS	0x00000000
0x041C	GPIO Pull Enable Register	GPIO_4_PUEN	0xFFFFFFFF
0x0420	GPIO Data Direction Register	GPIO_4_DDIR	0x00000000
0x0424	GPIO Output Source Select Register 1	GPIO_4_OCR1	0x00000000
0x0428	GPIO Output Source Select Register 2	GPIO_4_OCR2	0x00000000
0x042C	GPIO Input Source Select A Register 1	GPIO_4_ICA1	0x00000000
0x0430	GPIO Input Source Select A Register 2	GPIO_4_ICA2	0x00000000
0x0434	GPIO Input Source Select B Register 1	GPIO_4_ICB1	0x00000000
0x0438	GPIO Input Source Select B Register 2	GPIO_4_ICB2	0x00000000
0x043C	GPIO Data Register	GPIO_4_DREG	0x00000000
0x0440	GPIO Interrupt Configuration Register 1	GPIO_4_ICR1	0x00000000
0x0444	GPIO Interrupt Configuration Register 2	GPIO_4_ICR2	0x00000000
0x0448	GPIO Interrupt Enable Register	GPIO_4_IMR	0x00000000
0x044C	GPIO Interrupt Status Register	GPIO_4_ISR	0x00000000
0x0450	GPIO Pull Select Register	GPIO_4_PUSE	0x00000000

0x0510	GPIO Control Register	GPIO_5_CTRL	0x00000000
0x0514	GPIO Function Register	GPIO_5_FUNC	0x00000000
0x0518	GPIO Mode Register	GPIO_5_GIUS	0x00000000
0x051C	GPIO Pull Enable Register	GPIO_5_PUEN	0xFFFFFFFF
0x0520	GPIO Data Direction Register	GPIO_5_DIR	0x00000000
0x0524	GPIO Output Source Select Register 1	GPIO_5_OCR1	0x00000000
0x0528	GPIO Output Source Select Register 2	GPIO_5_OCR2	0x00000000
0x052C	GPIO Input Source Select A Register 1	GPIO_5_ICA1	0x00000000
0x0530	GPIO Input Source Select A Register 2	GPIO_5_ICA2	0x00000000
0x0534	GPIO Input Source Select B Register 1	GPIO_5_ICB1	0x00000000
0x0538	GPIO Input Source Select B Register 2	GPIO_5_ICB2	0x00000000
0x053C	GPIO Data Register	GPIO_5_DREG	0x00000000
0x0540	GPIO Interrupt Configuration Register 1	GPIO_5_ICR1	0x00000000
0x0544	GPIO Interrupt Configuration Register 2	GPIO_5_ICR2	0x00000000
0x0548	GPIO Interrupt Enable Register	GPIO_5_IMR	0x00000000
0x054C	GPIO Interrupt Status Register	GPIO_5_ISR	0x00000000
0x0550	GPIO Pull Select Register	GPIO_5_PUSE	0x00000000

Register Description

GPIO Device Identification Register

Offset Address

GPIO_IDR

GPIO Device Identification Register

0x0000

BIT	31	30	29	28	27	26	25	24
NAME	CLID[15:8]							
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	1	0	0	0
	0x08							
BIT	23	22	21	20	19	18	17	16
NAME	CLID[7:0]							
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	1	0
	0x10							
BIT	15	14	13	12	11	10	9	8
NAME	DSGNR[5:0]						MAJOR[3:2]	
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	MAJOR[1:0]		MINOR[5:0]					
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	1	0	0	0	0	1	0
	0x42							

Table 9-2: GPIO Device Identification Register Description

Name	Description	Setting
CLID[15:0] Bit 31-16	PCI Class Code – This field represents the PCI class code of the GPIO.	0x0810
DSGNR[5:0] Bit 15-10	Design Number – This field represents the design number of the GPIO.	0x00
MAJOR[3:0] Bit 9-6	Major Revision Number – This field represents the major release of the GPIO.	0x01
MINOR[5:0] Bit 5-0	Minor Revision Number – This field represents the minor release of the GPIO.	0x02

GPIO Capabilities Register

Offset Address

GPIO_CAPR

GPIO Capabilities Register

0x0004

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0

Table 9-3: GPIO Capabilities Register Description

Name	Description	Setting
Reserved Bit 31-0	Reserved	

GPIO Control Registers

The GPIO Control Register contains the software reset and the port interrupt mask bits of the port. The reset sequence will take a 3 operating clock cycles and will self-clear once the operation has completed. The PMSK bit provides the interrupt masking capability at the port level.

GPIO_<N>_CTRL		GPIO Control Register							Offset Address
									0x0010+N*0x100
BIT	31	30	29	28	27	26	25	24	
NAME									
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0	0	0	0	0	0	0	0	
0x00									
BIT	23	22	21	20	19	18	17	16	
NAME									
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0	0	0	0	0	0	0	0	
0x00									
BIT	15	14	13	12	11	10	9	8	
NAME									
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0	0	0	0	0	0	0	0	
0x00									
BIT	7	6	5	4	3	2	1	0	
NAME							PMSK	RST	
TYPE	RO	RO	RO	RO	RO	RO	RW	RWAC	
RESET	0	0	0	0	0	0	0	0	
0x00									

Table 9-4: GPIO Control Register Description

Name	Description	Setting
Reserved Bit 31–2	Reserved	
PMSK Bit 1	Port Interrupt Mask – Writing a ‘1’ to this bit masked the interrupt from the port.	0 = Interrupt is not masked (default) 1 = Interrupt is masked
RST Bit 0	Reset – Writing a ‘1’ to this bit will reset the port. This bit will be cleared after the reset is completed.	0 = Default 1 = Reset active

GPIO Function Registers

The GPIO Function Register controls the multiplexer in the IOMUX module to select between the primary peripheral function and alternate peripheral function.

GPIO_<N>_FUNC		GPIO Function Register							Offset Address
									0x0014+N*0x0100
BIT	31	30	29	28	27	26	25	24	
NAME	FUNC[31:24]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
	0x00								
BIT	23	22	21	20	19	18	17	16	
NAME	FUNC[23:16]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
	0x00								
BIT	15	14	13	12	11	10	9	8	
NAME	FUNC[15:8]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
	0x00								
BIT	7	6	5	4	3	2	1	0	
NAME	FUNC[7:0]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
	0x00								

Table 9-5: GPIO Function Register Description

Name	Description	Setting
FUNC[31:0] Bits 31-0	Function Register – This register selects between the primary and alternative functions of the pin. When the GPIO_MODE register is set for the corresponding pin, the register bit is ignored (not effective).	0 = Primary pin (default) 1 = Alternative pin

GPIO Mode Registers

The GPIO Mode Register controls a multiplexer in the IOMUX module to select between peripheral function and GPIO function.

GPIO_<N>_MODE		GPIO Mode Register							Offset Address
									0x0018+N*0x0100
BIT	31	30	29	28	27	26	25	24	
NAME	MODE[31:24]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
	0x00								
BIT	23	22	21	20	19	18	17	16	
NAME	MODE[23:16]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
	0x00								
BIT	15	14	13	12	11	10	9	8	
NAME	MODE[15:8]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
	0x00								
BIT	7	6	5	4	3	2	1	0	
NAME	MODE[7:0]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
	0x00								

Table 9-6: GPIO Mode Register Description

Name	Description	Setting
MODE[31:0] Bit 31-0	Mode Register – This register controls the IOMUX multiplexing function. When it is set, the GPIO function is active and primary or alternate function selection is ignored for the corresponding bit.	0 = Multiplexed function (default) 1 = GPIO function active

GPIO Pull Enable Registers

The GPIO Pull Enable Register enables or disables the weak pull-up/down resistor on the selected pin. Pin is tri-stated when the pull-up/down is disabled and not driven.

GPIO_<N>_PUEN		GPIO Pull Register							Offset Address
									0x001C+N*0x0100
BIT	31	30	29	28	27	26	25	24	
NAME	PUEN[31:24]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	1	1	1	1	1	1	1	1	
	0xFF								
BIT	23	22	21	20	19	18	17	16	
NAME	PUEN[23:16]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	1	1	1	1	1	1	1	1	
	0xFF								
BIT	15	14	13	12	11	10	9	8	
NAME	PUEN[15:8]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	1	1	1	1	1	1	1	1	
	0xFF								
BIT	7	6	5	4	3	2	1	0	
NAME	PUEN[7:0]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	1	1	1	1	1	1	1e	1	
	0xFF								

Table 9-7: GPIO Pull Register Description

Name	Description	Setting
PUEN[31:0] Bits 31-0	Pull Enable – The bits of this register are used to enable or disable a pull-up resistor connection to the corresponding pin. When a bit is set to ‘1’, a pull resistor is connected and when cleared to ‘0’, the resistor is disconnected.	0 = Pin is tri-state when not driven 1 = Pin is pulled high/low when not driven (default)

GPIO Data Direction Registers

The GPIO Data Direction Register determines the data direction of each pin.

GPIO_<N>_DIR		GPIO Data Direction Register							Offset Address
									0x0020+N*0x0100
BIT	31	30	29	28	27	26	25	24	
NAME	DIR[31:24]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
	0x00								
BIT	23	22	21	20	19	18	17	16	
NAME	DIR[23:16]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
	0x00								
BIT	15	14	13	12	11	10	9	8	
NAME	DIR[15:8]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
	0x00								
BIT	7	6	5	4	3	2	1	0	
NAME	DIR[7:0]								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
	0x00								

Table 9-8: GPIO Data Direction Register Description

Name	Description	Setting
DIR[31:-0] Bits 31-0	Data Direction Register – This register controls direction of the pins in the GPIO port.	0 = Pin configured as input (default) 1 = Pin configured as output

GPIO Output Source Select Registers 1

The GPIO Output Source Select Register selects one of the four possible sources for the output. Register 1 controls the lower 16 pins.

GPIO_<N>_OSS1		GPIO Output Source Select Register 1							Offset Address
									0x0024+N*0x0100
BIT	31	30	29	28	27	26	25	24	
NAME	OSS1								
	Pin 15		Pin 14		Pin 13		Pin 12		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16	
NAME	OSS1								
	Pin 11		Pin 10		Pin 9		Pin 8		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8	
NAME	OSS1								
	Pin 7		Pin 6		Pin 5		Pin 4		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0	
NAME	OSS1								
	Pin 3		Pin 2		Pin 1		Pin 0		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	

Table 9-9: GPIO Output Source Select Register 1 Description

Name	Description	Setting
OSS1 Bit 31-0	Output Source Select Register 1 – This register controls pins output selection from AIN, BIN, CIN, or data register.	00 = Data Register (default) 01 = AIN 10 = BIN 11 = CIN

GPIO Output Source Select Registers 2

The GPIO Output Source Select Register selects one of the four possible sources for the output. Register 2 controls the upper 16 pins.

GPIO_<N>_OSS2		GPIO Output Source Select Register 2							Offset Address
									0x0028+N*0x0100
BIT	31	30	29	28	27	26	25	24	
NAME	OSS2								
	Pin 31		Pin 30		Pin 29		Pin 28		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16	
NAME	OSS2								
	Pin 27		Pin 26		Pin 25		Pin 24		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8	
NAME	OSS2								
	Pin 23		Pin 22		Pin 21		Pin 20		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0	
NAME	OSS2								
	Pin 19		Pin 18		Pin 17		Pin 16		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	

Table 9-10: GPIO Output Source Select Register 2 Description

Name	Description	Setting
OSS2 Bit 31-0	Output Source Select Register 2 – This register controls pins output selection from AIN, BIN, CIN, or data register.	00 = Data Register (default) 01 = AIN 10 = BIN 11 = CIN

GPIO Input Source Select A Registers 1

The GPIO Input Source Select A Register selects one of the four possible sources for the alternative destination A. Register 1 controls the lower 16 pins.

GPIO_<N>_ISSA1		GPIO Input Source Select A Register 1							Offset Address
									0x002C+N*0x0100
BIT	31	30	29	28	27	26	25	24	
NAME	ISSA1								
	Pin 15		Pin 14		Pin 13		Pin 12		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16	
NAME	ISSA1								
	Pin 11		Pin 10		Pin 9		Pin 8		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8	
NAME	ISSA1								
	Pin 7		Pin 6		Pin 5		Pin 4		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0	
NAME	ISSA1								
	Pin 3		Pin 2		Pin 1		Pin 0		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	

Table 9-11: GPIO Input Configuration A Register 1 Description

Name	Description	Setting
ISSA1 Bit 31-0	Source Select A Register 1 – This register controls the value driven to the AOUT port. GIN is the input value from the pad.	00 = GIN (default) 01 = Interrupt Status Register [pin] 10 = 0 11 = 1

GPIO Input Source Select A Registers 2

The GPIO Input Source Select A Register selects one of the four possible sources for the alternative destination A. Register 2 controls the upper 16 pins.

GPIO_<N>_ISSA2		GPIO Input Source Select A Register 2								Offset Address
										0x0030+N*0x0100
BIT	31	30	29	28	27	26	25	24		
NAME	ISSA2									
	Pin 31		Pin 30		Pin 29		Pin 28			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16		
NAME	ISSA2									
	Pin 27		Pin 26		Pin 25		Pin 24			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8		
NAME	ISSA2									
	Pin 23		Pin 22		Pin 21		Pin 20			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0		
NAME	ISSA2									
	Pin 19		Pin 18		Pin 17		Pin 16			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	

Table 9-12: GPIO Input Source Select A Register 2 Description

Name	Description	Setting
ISSA2 Bit 31-0	Input Source Select A Register 2 – This register controls the value driven to the AOUT port. GIN is the input value of the pad.	00 = GIN (default) 01 = Interrupt Status Register [pin] 10 = 0 11 = 1

GPIO Input Source Select B Registers 1

The GPIO Input Source Select B Register selects one of the four possible sources for the alternate destination B. Register 1 controls the lower 16 pins.

GPIO_<N>_ISSB1		GPIO Input Source Select B Register 1								Offset Address
										0x0034+N*0x0100
BIT	31	30	29	28	27	26	25	24		
NAME	ISSB1									
	Pin 15		Pin 14		Pin 13		Pin 12			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16		
NAME	ISSB1									
	Pin 11		Pin 10		Pin 9		Pin 8			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8		
NAME	ISSB1									
	Pin 7		Pin 6		Pin 5		Pin 4			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0		
NAME	ISSB1									
	Pin 3		Pin 2		Pin 1		Pin 0			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	

Table 9-13: GPIO Input Source Select B Register 1 Description

Name	Description	Setting
ISSB1 Bit 31-0	Input Source Select B Register 1 – This register controls the value driven to the BOUT port. GIN is the input value on the pad.	00 = GIN (default) 01 = Interrupt Status Register [pin] 10 = 0 11 = 1

GPIO Input Source Select B Registers 2

The GPIO Input Source Select B Register selects one of the four possible sources for the alternate destination B. Register 2 controls the upper 16 pins.

GPIO_<N>_ISSB2		GPIO Input Source Select B Register 2							Offset Address
									0x0038+N*0x0100
BIT	31	30	29	28	27	26	25	24	
NAME	ISSB2								
	Pin 31		Pin 30		Pin 29		Pin 28		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16	
NAME	ISSB2								
	Pin 27		Pin 26		Pin 25		Pin 24		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8	
NAME	ISSB2								
	Pin 23		Pin 22		Pin 21		Pin 20		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0	
NAME	ISSB2								
	Pin 19		Pin 18		Pin 17		Pin 16		
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	

Table 9-14: GPIO Input Source Select B Register 2 Description

Name	Description	Setting
ISSB2 Bit 31-0	Input Source Select B Register 2 – This register controls the value driven to the BOUT port. GIN is the input value on the pad.	00 = GIN (default) 01 = Interrupt Status Register [pin] 10 = 0 11 = 1

GPIO Data Registers

The GPIO Data Register contains the data to be driven to the output when selected by Output Configuration register. When read, it provides the sampled value of the GPIO input.

GPIO_<N>_DREG		GPIO Data Register							Offset Address
									0x003C+N*0x0100
BIT	31	30	29	28	27	26	25	24	
NAME	DREG								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16	
NAME	DREG								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8	
NAME	DREG								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0	
NAME	DREG								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	

Table 9-15: GPIO Data Register Description

Name	Description	Setting
DREG Bit 31-0	Data Register – This register contains the GPIO output values when the Output Configuration Register selects the DREG as the output for the pin. When read, it provides the sampled value of the GPIO pins.	0 = Output driven low (default) 1 = Output driven high

GPIO Interrupt Configuration Registers 1

The GPIO Interrupt Configuration Register controls the interrupt configuration of the pin. Register 1 controls the lower 16 pins of the port.

GPIO_<N>_ICR1		GPIO Interrupt Configuration Register 1								Offset Address
										0x0040+N*0x0100
BIT	31	30	29	28	27	26	25	24		
NAME	ICR1									
	Pin 15		Pin 14		Pin 13		Pin 12			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16		
NAME	ICR1									
	Pin 11		Pin 10		Pin 9		Pin 8			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8		
NAME	ICR1									
	Pin 7		Pin 6		Pin 5		Pin 4			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0		
NAME	ICR1									
	Pin 3		Pin 2		Pin 1		Pin 0			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	

Table 9-16: GPIO Interrupt Configuration Register 1 Description

Name	Description	Setting
ICR1 Bit 31-0	GPIO Interrupt Configuration Register 1 – This register configures sensitivity of the interrupt based on one of the four options.	00 = Rising edge sensitive (default) 01 = Falling edge sensitive 10 = High level 11 = Low level

GPIO Interrupt Configuration Registers 2

The GPIO Interrupt Configuration Register controls the interrupt configuration of the pin. Register 2 controls the upper 16 pins of the port.

GPIO_<N>_ICR2		GPIO Interrupt Configuration Register 2								Offset Address
										0x0044+N*0x0100
BIT	31	30	29	28	27	26	25	24		
NAME	ICR2									
	Pin 31		Pin 30		Pin 29		Pin 28			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16		
NAME	ICR2									
	Pin 27		Pin 26		Pin 25		Pin 24			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8		
NAME	ICR2									
	Pin 23		Pin 22		Pin 21		Pin 20			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0		
NAME	ICR2									
	Pin 19		Pin 18		Pin 17		Pin 16			
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	0	

Table 9-17: GPIO Interrupt Configuration Register 2 Description

Name	Description	Setting
ICR2 Bit 31-0	GPIO Interrupt Configuration Register 1 – This register configures sensitivity of the interrupt based on one of the four options.	00 = Rising edge sensitive (default) 01 = Falling edge sensitive 10 = High level 11 = Low level

GPIO Interrupt Enable Registers

The GPIO Interrupt Enable Register controls the interrupt bit masking of the pin.

GPIO_<N>_IER		GPIO Interrupt Enable Register							Offset Address
									0x0048+N*0x0100
BIT	31	30	29	28	27	26	25	24	
NAME	IER								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16	
NAME	IER								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8	
NAME	IER								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0	
NAME	IER								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0	0	0	0	0	0	0	0	

Table 9-18: GPIO Interrupt Enable Register Description

Name	Description	Setting
IER Bit 31-0	Interrupt Enable Register – This register is used to enable or disable the interrupt for the corresponding pin. Writing a ‘1’ to the bit enables the interrupt and writing a ‘0’ the bit disables the interrupt. The bit has no effect if the corresponding pin has not been configured as an interrupt input pin.	0 = Interrupt is disabled (default) 1 = Interrupt is enabled

GPIO Interrupt Status Registers

The GPIO Interrupt Status Register indicates the occurrence of I/O interrupts. The associated bit is set when an event occurred.

GPIO_<N>_ISR		GPIO Interrupt Status Register							Offset Address
									0x004C+N*0x0100
BIT	31	30	29	28	27	26	25	24	
NAME	ISR								
TYPE	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	
RESET	0	0	0	0	0	0	0	0	
BIT	23	22	21	20	19	18	17	16	
NAME	ISR								
TYPE	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	
RESET	0	0	0	0	0	0	0	0	
BIT	15	14	13	12	11	10	9	8	
NAME	ISR								
TYPE	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	
RESET	0	0	0	0	0	0	0	0	
BIT	7	6	5	4	3	2	1	0	
NAME	ISR								
TYPE	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	
RESET	0	0	0	0	0	0	0	0	

Table 9-19: GPIO Interrupt Status Register Description

Name	Description	Setting
ISR Bit 31-0	GPIO Interrupt Status Register – This register indicates the occurrence of the interrupt in the GPIO port. A bit is cleared by writing a “1” to the bit.	0 = No interrupt (default) 1 = Interrupt has occurred

GPIO Pull Select Registers

The GPIO Pull Select Register controls the pull-up or pull-down of the pin.

GPIO_[1-6]_PSR		Pull Select Register							Offset Address
									0x0050+N*0x0100
BIT	31	30	29	28	27	26	25	24	
NAME	PUSE								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	1	1	1	1	1	1	1	1	
BIT	23	22	21	20	19	18	17	16	
NAME	PUSE								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	1	1	1	1	1	1	1	1	
BIT	15	14	13	12	11	10	9	8	
NAME	PUSE								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	1	1	1	1	1	1	1	1	
BIT	7	6	5	4	3	2	1	0	
NAME	PUSE								
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	1	1	1	1	1	1	1	1	

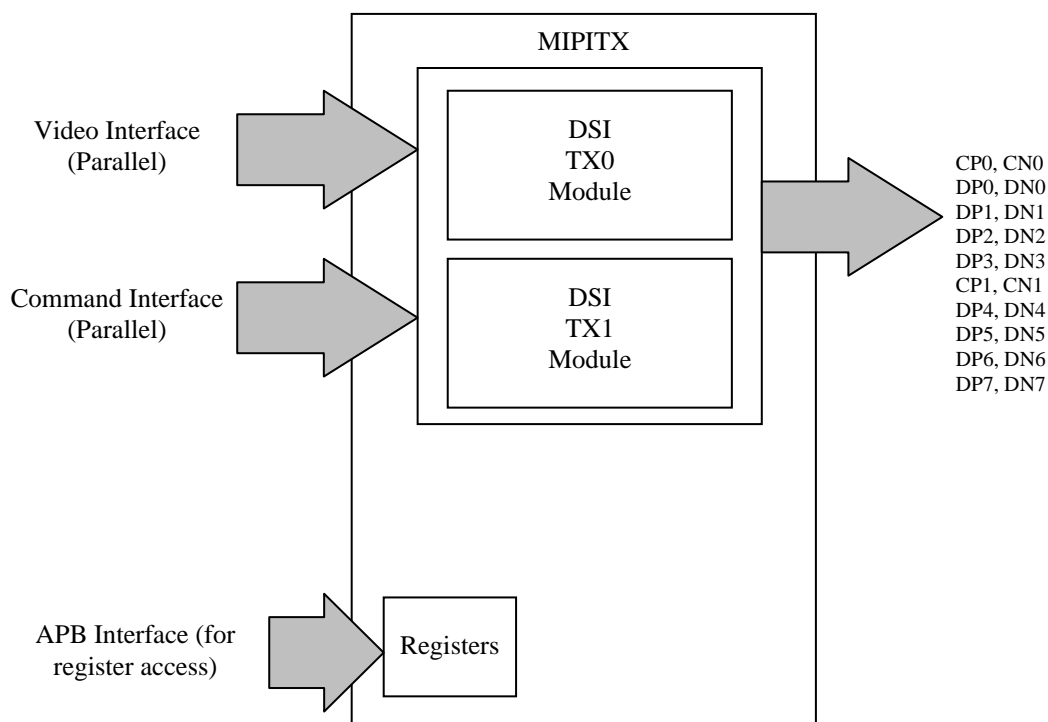
Table 9-20: GPIO Interrupt Enable Register Description

Name	Description	Setting
PUSE Bit 31-0	Pull Select Register – This register bit level control the pull-up/pull-down selection for each pin of the GPIO port. The register bit control will only be effective if the corresponding Pull Enable Register bit was set.	1 = Pull-up 0 = Pull-down (default)

10 MIPI DSI TX (MIPITX)

Features

MIPITX is a dual DSI TX module, support up to 2 clock lanes, 8 data lanes each capable of up to 1.5Gbps.



References

MIPI DSI, DCS, D-PHY Standard

Definitions

HS High Speed

LP Low Power

MCU Proprietary parallel interface between the MIPI RX IP and display display driver, which is for display driver register and memory access

RGB MIPI Alliance Standard for Display Pixel Interface v2.0 (DPI-2)

Detailed Descriptions

Multiple DSI Output (Video and Command)

MIPITX can support 1 DSI output.

For command outputs, the access would only be done on enabled DSI. Further, for write, it would be broadcast to whichever DSI that is forward-write enabled. For read command, if only one of the DSI is reverse-read enabled, then MIPITX will return the read data to upstream module from the particular DSI port. If multiple DSI are reverse-read enabled, only DSI0 read data is returned to upstream module.

Programming Model

Table 10-1: DSITX Register Summary

Offset	Name	Mnemonic	Reset Value
0x000	Identification Register	IDR	0x0000_0040
0x004	Capability register	CAPR	0x0000_0000
0x008	Control Register	CTLR	0x0003_0008
0x00C	Video Timing Control 1 Register	VTC1R	0x0214_020A
0x010	Video Timing Control 2 Register	VTC2R	0x0438_020A
0x014	Video Configuration Register	VCFR	0x0100_0101
0x018	Trimming Control Register	TMCR	0x0000_0000
0x030	Watermark Register	WMR	0x0000_FFFF
0x034	Partition Register	PSTR	0x0000_FFFF
0x038	HS Transmission Timer Register	HTTR	0x0010_0000
0x03C	LP Receiving Timer Register	LRTR	0x0010_0000
0x040	Delay Adjust 1 Register	DA1R	0x2803_1402
0x044	Delay Adjust 2 Register	DA2R	0x0A0A_0416
0x048	Delay Adjust 3 Register	DA3R	0x1000_4510
0x04C	Analog Control Register	ACR	0xE31C_19A3
0x050	Video Bist 1 Register	VB1R	0x0000_0000
0x054	Video Bist 2 Register	VB2R	0x0000_0000
[0x080+(n*32)] + 0x000	DSIn Control Register	DSInCR	0x0300_000F(for n=0), 0x0300_000A(for n!=1)
[0x080+(n*32)] + 0x004	DSIn Video Register	DSInVR	0x0000_0400
[0x080+(n*32)] + 0x008	DSIn Ack Response Register	DnARR	0x0000_0000
[0x080+(n*32)] + 0x00C	DSIn Status Register	DnSR	0x0000_03C0
[0x080+(n*32)] + 0x010	DSIn Delay Control 1 Register	DSInDC1R	0x4040_4040
[0x080+(n*32)] + 0x014	DSIn Delay Control 2 Register	DSInDC2R	0x0040_4040

Note : n is the number of DSITX instantiated minus 1. For example if number of DSITX is 4, n = 3.

Register Descriptions

Device Identification Register

Offset Address

IDR Device Identification Register **0x000**

BIT	31	30	29	28	27	26	25	24
NAME	CLID[15:8]							
TYPE	RO							
RESET	0x00							
BIT	23	22	21	20	19	18	17	16
NAME	CLID[7:0]							
TYPE	RO							
RESET	0x00							
BIT	15	14	13	12	11	10	9	8
NAME	DSGNR[5:0]					MAJOR[3:2]		
TYPE	RO					RO		
RESET	0x00					0x0		
BIT	7	6	5	4	3	2	1	0
NAME	MAJOR[1:0]		MINOR[5:0]					
TYPE	RO		RO					
RESET	0x1		0x00					

Table 10-2: Device Identification Register Description

Name	Description	Setting
CLID Bit 31-16	PCI Class Code	0x00
DSGNR Bit 15-10	Design Number	0x00
MAJOR Bit 9-6	Major Release	0x1
MINOR Bit 5-0	Minor Release	0x00

Capability Register

Offset Address

CPAR

Capability Register

0x004

BIT	31	30	29	28	27	26	25	24
NAME	CAP[31:24]							
TYPE	RO							
RESET	0x00							
BIT	23	22	21	20	19	18	17	16
NAME	CAP[23:16]							
TYPE	RO							
RESET	0x00							
BIT	15	14	13	12	11	10	9	8
NAME	CAP[15:8]							
TYPE	RO							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	CAP[7:0]							
TYPE	RO							
RESET	0x00							

Table 10-3: Capability Register Description

Name	Description	Setting
CAP Bit 31-0	Capability	0x0000

Control Register

Offset Address

CTLR

Control Register

0x008

BIT	31	30	29	28	27	26	25	24
NAME	TM[1:0]		IBC	EIC[4:0]				
TYPE	RW		RW	RW				
RESET	0x0		0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME	LS_OUT[1:0]		LPD[5:0]					
TYPE	RW		RW					
RESET	0x0		0x03					
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
BIT	7	6	5	4	3	2	1	0
NAME	VCTX	VBC	TXD	LPE	EOT	ECD	HCLK	CKE
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x1	0x0	0x0	0x0

Table 10-4: Control Register Description

Name	Description	Setting
CKE Bit 0	Clock Lane Enable – This bit controls the clock lane mode when data lane enters LP mode	0 = Clock lane will enter LP mode, if it is not in reverse direction communication. Clock lane will follow the setting of HCLK , if it is in reverse direction communication. 1 = Clock lane will enter HS mode for all the cases.
HCLK Bit 1	HS Clock Disable – This bit controls the clock lane behavior during the reverse direction communication. This bit takes effect only when both CKE and VEN are 0.	0 = HS clock is enabled 1 = HS clock is disabled
ECD Bit 2	ECC CRC Check Disable – This bit specifies whether DSITX will perform ECC and CRC checking for the packets received from the MIPI slave.	0 = Enabled 1 = Disabled
EOT Bit 3	EOT Packet Enable – This bit specifies whether the SSD2850 will send out the EOT packet at the end of HS transmission or not.	0 = Do not send 1 = Send
LPE Bit 4	Long Packet Enable – This bit specifies whether the DSITX will send out a Generic Long Write Packet or Generic Short Write Packet when the payload is no more than 2 bytes. It also specifies whether the DSITX will send out a DCS Long Write Packet or DCS Short Write Packet when the payload is no more than 1 byte.	0 = Short Packet 1 = Long Packet
TXD	Transmit Disable – This bit specifies whether	0 = Transmit on

Bit 5	<p>the DSITX will disable the sending of MIPI Packets stored in the buffers.</p> <p>Software can enable TXD, fill out the buffers and then disable it to send all packets out in 1 burst.</p>	1 = Transmit halt
VBC Bit 6	Video BroadCast – This bit defines how DSITX handles video line input.	<p>0 = Video line is sliced according to number of MIPI DSITX selected.</p> <p>1 = Video line is repeated according to number of MIPI DSITX selected.</p>
VCTX Bit 7	Output VC follows TX – This bit controls the output VC for DSITX.	<p>0 = Output VC follows the input VC</p> <p>1 = Output VC follows the registered VC</p>
Reserved Bit 9-8	Reserved	
Reserved Bit 10	Reserved	
Reserved Bit 11	Reserved	
Reserved Bit 15-12		
LPD Bit 21-16	LP Clock Divider – These bits give the divider value for generating the LP mode clock from the byte clock.	<p>0x0 = Divide by 1</p> <p>0x1 = Divide by 2</p> <p>...</p> <p>0x3F = Divide by 64</p>
LS_OUT Bit 23-22	<p>Lane Select Output – These bits select the number of lane used for all DSITX.</p> <p>Note : In 3-DSI mode, only 1-lane or 2-lane mode is possible.</p>	<p>00 = 1-lane mode</p> <p>01 = 2-lane mode</p> <p>10 = 3-lane mode</p> <p>11 = 4-lane mode</p>
EIC Bit 28-24	Error Injection Control – These bits control the position of the error being injected for testing. It is only applicable when TM is 01.	
IBC Bit 29	<p>Ignore Bus Contention – This bit is to disable bus contention reported by the Analog Phy.</p> <p>If this bit is disabled, whenever bus contention is detected, the state machine will ignore it and continue sending new packet if available. If this bit is enabled, the state machine will halt further transmission.</p>	<p>0 = Detect Bus contention from Analog Phy</p> <p>1 = Ignore Bus contention from Analog Phy</p>
TM Bit 31-30	Test Mode – These bits select whether to inject CRC/ECC error for the outgoing streams. They are used for debugging purpose only. They should be set to 00 in normal mode.	<p>00 = Normal mode</p> <p>01 = Inject CRC error</p> <p>10 = Inject 1 bit ECC error</p> <p>11 = Inject 2 bit ECC error</p>

Video Timing Control 1 Register

Offset Address

VTC1R

Video Timing Control Register

0x00C

BIT	31	30	29	28	27	26	25	24
NAME	VBP[7:0]							
TYPE	RW							
RESET	0x02							
BIT	23	22	21	20	19	18	17	16
NAME	HBP[7:0]							
TYPE	RW							
RESET	0x14							
BIT	15	14	13	12	11	10	9	8
NAME	VSA[7:0]							
TYPE	RW							
RESET	0x02							
BIT	7	6	5	4	3	2	1	0
NAME	HSA[7:0]							
TYPE	RW							
RESET	0x0A							

Table 10-5: Video Timing Control 1 Register Description

Name	Description	Setting
HSA Bit 7-0	Horizontal Sync Active period for DSITX – These bits specify the Hsync active period. The Hsync active period is from the Hsync falling edge to rising edge, in terms of pclk. It is only used in non-burst mode with Sync pulses when VM = 00 , where MIPITX generates blanking packet in-between the Hsync Sync Start and End packet.	The minimum value is 1.
VSA Bit 15-8	Vertical Sync Active Period for DSITX – These bits specify the Vsync active period. The Vsync active period is from the Vsync falling edge to rising edge, in terms of Hsync pulses. It is only used in non-burst mode with Sync pulses when VM = 00 , where MIPITX generates the Hsync Sync Start and End packet per line.	The minimum value is 1.
HBP Bit 23-16	Horizontal Back Porch Period for DSITX – These bits specify the horizontal back porch period in terms of pclk. The horizontal back porch period depends on the non-burst mode setting, VM . If the mode is non-burst mode with Sync pulses (VM = 00), it is from the Hsync rising edge to the start of the valid display pixel. If the mode is non-burst mode with Sync events, it is from the Hsync falling edge to the start of the valid display pixel. If the mode is burst mode, it is the same as the non-burst mode with Sync events.	<u>Non-burst Sync Event or Burst mode</u> HT = HBP + HACT + HFP <u>Non-burst Sync Pulses</u> VT = HSA + HBP + HACT + HFP
VBP Bit 31-24	Vertical Back Porch Period for DSITX – These bits specify the vertical back porch period in terms of Hsync pulses. The vertical back porch period depends on the video mode setting,	<u>Non-burst Sync Event or Burst mode</u> VT = VBP + /VEN + VFP

	<p>VM.</p> <p>If the mode is non-burst mode with Sync pulses, it is from the Vsync rising edge to the Hsync of the first line of active display.</p> <p>If the mode is non-burst mode with Sync events, it is from the Vsync falling edge to the Hsync of the first line of active display.</p> <p>If the mode is burst mode, it is the same as the non-burst mode with Sync events.</p>	<p><u>Non-burst Sync Pulses</u></p> $VT = VSA + VBP + VACT + VFP$
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Video Timing Control 2 Register

Offset Address

VTC2R

Video Timing Control 2 Register

0x010

BIT	31	30	29	28	27	26	25	24
NAME	VACT[15:8]							
TYPE	RW							
RESET	0x04							
BIT	23	22	21	20	19	18	17	16
NAME	VACT[7:0]							
TYPE	RW							
RESET	0x38							
BIT	15	14	13	12	11	10	9	8
NAME	VFP[7:0]							
TYPE	RW							
RESET	0x02							
BIT	7	6	5	4	3	2	1	0
NAME	HFP[7:0]							
TYPE	RW							
RESET	0x0A							

Table 10-6: Video Timing Control 2 Register Description

Name	Description	Setting
HFP Bit 7-0	Horizontal Front Porch Period for DSITX – These bits specify the horizontal front porch period in terms of pelk. The horizontal front porch period is from the end of the valid display pixel to the next Hsync falling edge.	
VFP Bit 15-8	Vertical Front Porch Period for DSITX – These bits specify the vertical front porch period in terms of Hsync pulses. The vertical front porch period is from the first Hsync after the last line of active display to the next Vsync falling edge.	
VACT Bit 31-16	Vertical Active Period for DSITX – These bits specify the vertical active period in terms of Hsync pulses of the output video packet of DSITX.	

Video Configuration Register

Offset Address

VCFR

Video Configuration Register

0x014

BIT	31	30	29	28	27	26	25	24
NAME	VBS	VBE	PNB[5:0]					
TYPE	RW	RW	RW					
RESET	0x0	0x0	0x01					
BIT	23	22	21	20	19	18	17	16
NAME	VCN[3:0]				VFN[3:0]			
TYPE	RW				RW			
RESET	0x0				0x0			
BIT	15	14	13	12	11	10	9	8
NAME	VB_MODE[1:0]						END	CO
TYPE	RW			RO	RO	RO	RW	RW
RESET	0x0			0x0	0x0	0x0	0x0	0x1
BIT	7	6	5	4	3	2	1	0
NAME		VEC	CBM	NVB	BLLP	VCS	VM[1:0]	
TYPE	RO	RW	RW	RW	RW	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x1

Table 10-7: Video Configuration Register Description

Name	Description	Setting
VM Bit 1-0	Video Mode – These bits specify the video mode the DSITX will use when RGB interface is selected. Please refer to MIPI DSI for the definition of different modes.	00 = Non burst mode with sync pulses 01 = Non burst mode with sync events 10 = Burst mode 11 = Reserved
VCS Bit 2	Video Clock Suspend – This bit specifies the clock lane behavior. This bit is only applicable for burst mode. When the video mode is non-burst mode, the clock lane will remain in HS mode all the time.	0 = The clock lane remains in HS mode, when there is no data to transmit. 1 = The clock lane enters LP mode when there is no data to transmit.
BLLP Bit 2	Blanking or Low Power Interval – This bit specifies the DSITX operation during BLLP period. This bit takes effect only for non burst mode. When the video mode is burst mode, the DSITX will not send any blanking packet during BLLP. It will enter LP mode. The DSITX will stay in LP mode after sending the non video data (if there is any), until the BLLP period ends. The DSITX will use this bit to decide whether to send blanking packet or enter LP mode after sending non video data (if there is any), until the BLLP period ends. Please note that entering and exiting from LP mode needs more time, as the speed of LP mode is slow. It is the responsibility of the host processor to make sure that the period is long enough to finish the data transfer and the timing of Hsync and Vsync is not affected.	0 = Blanking packet will be sent during BLLP period. 1 = LP mode will be used during BLLP period.
NVB Bit 4	Non Video Data Burst Mode Control – This bit specifies how non-video data will be	0 = Non video data will be transmitted during any BLLP

	interleaved with video data transmission in burst mode.	period 1 = Non video data will only be transmitted during vertical blanking period
CBM Bit 5	Compress Burst Mode Control – If the mode is burst and this bit is 1, DSITX will send video packet in compressed burst mode (i.e. no blanking packet after horizontal sync packet)	0 = Video with blanking packet 1 = Video with no blanking packet
VEC Bit 6	Video Enable Control – This bit controls how command is handled during video mode, VEN . When VEC =0, any command received will output immediately if there is no video packet to send. When VEC =1, any command received will only be output during the blanking period after first video packet is received. If there is no video packet to be sent, the command is held.	0 = Command packet will be sent immediately when there is no video to send. 1 = Command packet will be sent after video packet are sent during Vertical blanking period for Non-burst video transfer or Vertical/Horizontal blanking period for Burst video transfer.
Reserved Bit 7		
CO Bit 8	Color Order – This bit specifies the order of the color component in the pixel. During video mode transmission, this bit must be set to 1 so as to follow the MIPI DSI specification.	0 = RGB. R is in the higher portion of the pixel. 1 = BGR. B is in the higher portion of the pixel.
END Bit 9	ENDian-ness – This bit specifies the endianness of the data transmitted over the serial link. During video mode transmission, this bit must be set to 0 so as to follow the MIPI DSI specification.	0 = Least significant byte sent first 1 = Most significant byte sent first
Reserved Bit 12-10		
VB_MODE Bit 15-13	Video Bist Mode – These bits select the Video BIST mode to be used when Video Bist is enabled.	000 = Fixed data 001 = In Increment order 010 = In decrement order 011 = Random data 1xx = Follow a color sequence (Red -> Green -> Blue -> Black-> White)
VFN Bit 19-16	Vertical Front Porch Non-video data window – These fields specify the number of vertical back porch counting backward from the first vertical active line in which non-video data is not allowed to be sent via MIPI link. This field is only valid when VEN is 1. This field should not larger than VBP . If it is larger, the internal logic will cap this field to VBP .	
VBN Bit 23-20	Vertical Back Porch Non-video data window – These fields specify the number of vertical front porch from the last vertical active line in which non-video data is not allowed to be sent via MIPI link. This field is only valid when VEN is 1. This field should not larger than VFP . If it is larger, the internal logic will cap this field to VFP .	
PNB Bit 29-24	Packet Number in Blanking Period – These bits control the number of packet to send during	

	video mode blanking period.	
VBE Bit 30	Video Bist Enable – This bit enables the video bist function. The DSITX will automatically send the color, red, green, blue, black and white repeatedly base on current setting. This bit should be 0 in normal mode	
VBS Bit 31	Video Bist Start – This bit starts the video bist process. Once clear, the video bist engine will stop at the frame boundary. The software should wait for at least 1 frame time before disabling the VBE bit.	

Trimming Control Register

Offset Address

TMCR

Trimming Control Register

0x018

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME						FBW	REN	DCS
TYPE	RO	RO	RO	RO	RO	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	TDC[7:0]							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	TRM_CMD[7:4]				TRM_CMD[3:0]/XR_FLT[3:0]			
TYPE	RW				RW			
RESET	0x0				0x0			

Table 10-8: Trimming Control Register Description

Name	Description	Setting
TRM_CMD [3:0]/XR_FLT Bit 3-0	Trimming Command[3:0]/XOR FILTER[3:0] – These bits define the lower 4 bits of the command header byte to be used in auto-trimming mode, when TRIM_EN =1, where DSITX send out a read request to the MIPI receiver. When XOR calibration is enabled, these bits define the filter to qualify the XOR calibration pulse width.	
TRM_CMD [7:4] Bit 7-4	Trimming Command[7:4]	
TDC Bit 15-8	Transmit Data Count – These bits indicate the number of bytes to write to the MIPI slave when auto-trimming mode is enabled.	
DCS Bit 16	DCS or Generic – This bit indicates the type of DSI packet sent when auto-trimming mode is enabled.	
REN Bit 17	Read Enable – This bit indicates the type of access to the MIPI slave when auto-trimming mode.	
FBW Bit 18	Force Bus Turnaround after Write – This bit will force an automatic Bus Turnaround when a write is initiated to the MIPI slave when auto-trimming mode is enabled.	
Reserved Bit 31-19		

Watermark Register

Offset Address

WMR

Watermark Register

0x030

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	WM[15:8]							
TYPE	RW							
RESET	0xFF							
BIT	7	6	5	4	3	2	1	0
NAME	WM[7:0]							
TYPE	RW							
RESET	0xFF							

Table 10-9: Watermark Register Description

Name	Description	Setting
WM Bit 15-0	<p>WaterMark – These bits specify when the buffer will start transferring relative to hsync.</p> <p>By allowing simultaneous read and write on the line buffer, it can support video line longer than the physical line buffer.</p> <p>The watermark has to be more than half a line to avoid buffer underflow</p> <p>If the next hsync is detected before the watermark is reached, then the buffer will start transferring anyway and the watermark counter will be reset.</p> <p>Unit : # byte clock</p>	
Reserved Bit 31-16		

Partition Register

Offset Address

PSTR

Partition Register

0x034

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	PST[15:8]							
TYPE	RW							
RESET	0xFF							
BIT	7	6	5	4	3	2	1	0
NAME	PST[7:0]							
TYPE	RW							
RESET	0xFF							

Table 10-10: Partition Register Description

Name	Description	Setting
PST Bit 15-0	<p>Packet Size Threshold – These bits give the threshold value for partitioning the incoming long packet data into smaller packets. The partitioning only applies to the DCS Long Write packet with DCS command being 0x2C or 0x3C. The payload will be partitioned into multiple packets.</p> <p>The PST represents the threshold in term of bytes.</p>	<p>The maximum value allowed is the line buffer size.</p> <p>PST will allows auto insertion of 0x3C at the PST boundary(Partition mode).</p> <p>If the user tries to program a larger value than the maximum allowed value into this field, DSITX will cap the value to the maximum value.</p>
Reserved Bit 31-16		

HS Transmit Timer Register

Offset Address

HTTR

HS Transmit Timer Register

0x038

BIT	31	30	29	28	27	26	25	24
NAME	HTT[31:24]							
TYPE	RW							
RESET	0x00							
BIT	23	22	21	20	19	18	17	16
NAME	HTT[23:16]							
TYPE	RW							
RESET	0x10							
BIT	15	14	13	12	11	10	9	8
NAME	HTT[15:8]							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	HTT[7:0]							
TYPE	RW							
RESET	0x00							

Table 10-11: HS Transmit Timer Register Description

Name	Description	Setting
HTT[31:0] Bit 31-0	<p>HS TX Timer – These bits specify the HS TX timer timeout value. PLL reference clock is used to increment an internal timer.</p> <p>The timer starts when the DSITX enters HS transmit mode. When the DSITX exits from HS transmit mode, the timer will be reset. If the timer expires before the end of HS transmission, the DSITX will signal an error and switch to LP mode to continue the transmission.</p> <p>Software intervention is required so that the DSITX can go back to proper HS transmission mode.</p>	

LP Receive Timer Register

Offset Address

LRTR

LP Receive Timer Register

0x03C

BIT	31	30	29	28	27	26	25	24
NAME	LRT[31:24]							
TYPE	RW							
RESET	0x00							
BIT	23	22	21	20	19	18	17	16
NAME	LRT[23:16]							
TYPE	RW							
RESET	0x10							
BIT	15	14	13	12	11	10	9	8
NAME	LRT[15:8]							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	LRT[7:0]							
TYPE	RW							
RESET	0x00							

Table 10-12: LP Receive Timer Register Description

Name	Description	Setting
LRT[31:0] Bit 31-0	<p>LP RX Timer – These bits specify the LP RX timer timeout value. PLL reference clock is used to increment an internal timer.</p> <p>The timer starts when the DSITX enters LP receive mode. When the DSITX exits from LP receive mode, the timer will be reset. If the timer expires before exiting from LP receive mode, the DSITX will signal an error and switch to LP transmit mode. The DPHY will drive the data lane to LP11 state.</p> <p>Software intervention is required so that any possible error could be cleared.</p>	

Delay Adjustment 1 Register

Offset Address

DA1R

Delay Adjustment 1 Register

0x040

BIT	31	30	29	28	27	26	25	24
NAME	CZD[7:0]							
TYPE	RW							
RESET	0x14							
BIT	23	22	21	20	19	18	17	16
NAME	CPD[7:0]							
TYPE	RW							
RESET	0x02							
BIT	15	14	13	12	11	10	9	8
NAME	HZD[7:0]							
TYPE	RW							
RESET	0x14							
BIT	7	6	5	4	3	2	1	0
NAME	HPD[7:0]							
TYPE	RW							
RESET	0x02							

Table 10-13: Delay Adjustment 1 Register Description

Name	Description	Setting
HPD Bit 7-0	HS Prepare Delay – These bits specify the number of byte clock for HS prepare delay period $T_{HS-PREPARE}$ for DSITX.	Minimum value is 1.
HZD Bit 15-8	HS Zero Delay – These bits specify the number of byte clock for HS zero delay period $T_{HS-ZERO}$ for DSITX.	Minimum value is 1.
CPD Bit 23-16	CLK Prepare Delay – These bits specify the number of byte clock for CLK prepare delay period $T_{CLK-PREPARE}$ for DSITX.	Minimum value is 1.
CZD Bit 31-24	CLK Zero Delay – These bits specify the number of byte clock for CLK zero delay period $T_{CLK-ZERO}$ for DSITX.	Minimum value is 1.

Delay Adjustment 2 Register

Offset Address

DA2R

Delay Adjustment 2 Register

0x044

BIT	31	30	29	28	27	26	25	24
NAME	CTD[7:0]							
TYPE	RW							
RESET	0x0A							
BIT	23	22	21	20	19	18	17	16
NAME	HTD[7:0]							
TYPE	RW							
RESET	0x0A							
BIT	15	14	13	12	11	10	9	8
NAME	CPED[7:0]							
TYPE	RW							
RESET	0x04							
BIT	7	6	5	4	3	2	1	0
NAME	CPTD[7:0]							
TYPE	RW							
RESET	0x16							

Table 10-14: Delay Adjustment 2 Register Description

Name	Description	Setting
CPED Bit 7-0	CLK Pre Delay – These bits specify the number of byte clock for CLK pre delay period $T_{CLK-PER}$ for DSITX.	Minimum value is 1.
CPTD Bit 15-8	CLK Post Delay – These bits specify the number of byte clock for CLK post delay period $T_{CLK-POST}$ for DSITX.	Minimum value is 1.
HTD Bit 23-16	HS Trail Delay – These bits specify the number of byte clock for HS trail delay period $T_{HS-TRAIL}$ for DSITX. Please note that the minimum value for the $T_{HS-TRAIL}$ is 3.	Minimum value is 1.
CTD Bit 31-24	CLK Trail Delay – These bits specify the number of byte clock for CLK trail delay period $T_{CLK-TRAIL}$ for DSITX.	Minimum value is 1.

Delay Adjustment 3 Register

Offset Address

DA3R

Delay Adjustment 3 Register

0x048

BIT	31	30	29	28	27	26	25	24	
NAME	WUD[15:8]								
TYPE	RW								
RESET	0x10								
BIT	23	22	21	20	19	18	17	16	
NAME	WUD[7:0]								
TYPE	RW								
RESET	0x00								
BIT	15	14	13	12	11	10	9	8	
NAME	TGO[3:0]				TGET[3:0]				
TYPE	RW				RW				
RESET	0x4				0x5				
BIT	7	6	5	4	3	2	1	0	
NAME	HED[5:0]								
TYPE	RO	RO						RW	
RESET	0x0	0x0						0x10	

Table 10-15: Delay Adjustment 3 Register Description

Name	Description	Setting
HED Bit 5-0	HS Exit Delay – These bits specify the number of byte clock for HS exit delay period for data and clock lane.	Minimum value is 1.
Reserved Bit 7-6		
TGET Bit 11-8	TA Get Delay – These bits specify the number of T_{LPX} for TA get delay period T_{TA-GET} for DSITX.	
TGO Bit 15-12	TA Go Delay – These bits specify the number of T_{LPX} for TA go delay period T_{TA-GO} for DSITX.	
WUD Bit 31-16	Wake Up Delay – These bits specify the number of clock cycles for wake up delay period T_{WAKEUP} for DSITX. The delay is used to wake up the MIPI slave from ULPS state. The clock is the low power clock.	Minimum value is 1.

Analog Control Register

Offset Address

ACR

Analog Control Register

0x04C

BIT	31	30	29	28	27	26	25	24
NAME	CONTE2	CONTE1	CONTE0	ATC_V_DS11			ATC_I_DS11	
TYPE	RW	RW	RW	RW			RW	
RESET	0x1	0x1	0x1	0x0			0x3	
BIT	23	22	21	20	19	18	17	16
NAME	ATC_V_DSIn			ATC_I_DSIn		ABE	THFT1	THFT0
TYPE	RW			RW		RW	RW	RW
RESET	0x0			0x3		0x1	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	TLFT1	TLFT0	PREEM_SEL[2:0]			PREEM_MOD[1:0]		
TYPE	RW	RW	RW			RW		
RESET	0x0	0x0	0x3			0x1		
BIT	7	6	5	4	3	2	1	0
NAME	PREEM_E	HSTX_Z[1:0]		LPTXDS[1:0]		HSTX_DS[2:0]		
TYPE	RW	RW		RW		RW		
RESET	0x1	0x1		0x0		0x3		

Table 10-16: Analog Control Register Description

Name	Description	Setting
HSTX_DS Bit 2-0	High Speed TX current Driver Selection – These bits control the driving current for the TX in high speed mode.	
LPTXDS Bit 4-3	Low Power TX Drive strength Selection – These bits control the drive strength for the TX in low power mode.	
HSTX_Z Bit 6-5	High Speed TX trimming – These bits control the input trimming bits for the output impedance control.	
PREEM_E Bit 7	PRE-EMphasis Enable – This bit is used for HSTX.	
PREEM_MDOE Bit 10-8	PRE-EMphasis Mode – These bits are used for pre-emphasis mode selection.	
PREEM_SEL Bit 13-11	PRE-EMphasis Select – These bits are used for tap selection for pre-emphasis.	
TLFT0 Bit 14	Low power Low threshold 0 – This bit controls the low power receiver schmitt trigger low threshold selection bit 0.	
TLFT1 Bit 15	Low power Low threshold 1 – This bit controls the low power receiver schmitt trigger low threshold selection bit 1.	
THFT0 Bit 16	Low power High threshold 0 – This bit controls the low power receiver schmitt trigger high threshold selection bit 0.	
THFT1 Bit 17	Low power High threshold 1 – This bit controls the low power receiver schmitt trigger high threshold selection bit 1.	
ABE Bit 18	Analog Bias Enable – This bit enables the bias current to the MIPI TX block.	
ATC_I[0] Bit 20:19	Analog Test Control pads for Current selection for DSITX0 – These bits provide the current selection for analog test control pads	

ATC_V[0] Bit 23:21	Analog Test Control pads for Voltage selection for DSITX0 – These bits provide the voltage selection for analog test control pads	
ATC_I[1] Bit 25:24	Analog Test Control pads for Current selection for DSITX1 – These bits provide the current selection for analog test control pads	
ATC_V[1] Bit 28:26	Analog Test Control pads for Voltage selection for DSITX1 – These bits provide the voltage selection for analog test control pads	
CONTE0 Bit 29	Contention Enable for DSITX0 – This bit enables the MIPI Phy contention detection feature on DSITX0.	
CONTE1 Bit 30	Contention Enable for DSITX1 – This bit enables the MIPI Phy contention detection feature on DSITX1.	
CONTE2 Bit 31	Contention Enable for DSITX2 – This bit enables the MIPI Phy contention detection feature on DSITX2.	

Video Bist 1 Register

Offset Address

VB1R

Video Bist 1 Register

0x050

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME	VBTD1[23:16]							
TYPE	RW							
RESET	0x00							
BIT	15	14	13	12	11	10	9	8
NAME	VBTD1[15:8]							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	VBTD1[7:0]							
TYPE	RW							
RESET	0x00							

Table 10-17: Video Bist 1 Register Description

Name	Description	Setting
VBTD1 Bit 23-0	Video Bist Test Data 1 – These bits are used for the first pixel of the video bist data input.	
Reserved Bit 31-24		

Video Bist 2 Register

Offset Address

VB2R

Video Bist 2 Register

0x054

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME	VBTD2[23:16]							
TYPE	RW							
RESET	0x00							
BIT	15	14	13	12	11	10	9	8
NAME	VBTD2[15:8]							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	VBTD2[7:0]							
TYPE	RW							
RESET	0x00							

Table 10-18: Video Bist 2 Register Description

Name	Description	Setting
VBTD2 Bit 23-0	Video Bist Test Data 2 – These bits are used for the second pixel of the video bist data input. It is used only when VB_MODE = 0(Fixed Mode), VB_MODE = 3(Random Mode).	
Reserved Bit 31-24		

DSIn Control Register(where n = 0 to 2)

DSInCR		DSIn Control Register							Offset Address
									[0x080+(n*32)] + 0x000
BIT	31	30	29	28	27	26	25	24	
NAME									
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
BIT	23	22	21	20	19	18	17	16	
NAME	DXEn	DFEn	D3FEn	D2FEn	D1FEn	D0FEn	XTEn	RCTRn	
TYPE	RW	RW	RW	RW	RW	RW	RW	RW	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
BIT	15	14	13	12	11	10	9	8	
NAME		DBGn	TMDn	TMPn	XRDn	XRSn	XREn	TMEn	
TYPE	RO	RW	RO	RO	RO	RW	RW	RW	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
BIT	7	6	5	4	3	2	1	0	
NAME	TRn	VCn[1:0]		TESMn	VEN_CT Rn	DRn	DWn	DSI_ ENn	
TYPE	RWAC	RW		RW	RW	RW	RW	RW	
RESET	0x0	0x0		0x0	0x1	0x*	0x1	0x*	

Table 10-19: DSIn Control Register Description

Name	Description	Setting
DSI_ENn Bit 0	DSITX n Enable – This bit enables DSITX n function.	0 = Disable 1 = Enable Note : For n=0, this bit is always 1.
DWn Bit 1	DSITX n Forward Write Enable – This bit enables all forward command write(DCS or Generic) packets. When disabled, DSITX will not transmit any command write packets. This bit is not valid when either DSIn_EN is 0.	0 = Disable 1 = Enable
DRn Bit 2	DSITX n Reverse Read Enable – This bit enables all reverse communication from MIPI slave device to DSITX n when the command read(DCS or Generic) packets are received. When disabled, DSITXn will not transmit the command read packet. If there are multiple DSITX instances, n=0 has the highest priority for read and the data from DSITXn will return to the MIPI host controller regardless of other reverse read enable bits. The priority of the DSITX starts from 0 to the last DSITX n-1.	0 = Disable 1 = Enable Note : For n=0, this default bit is 1.
VEN_CTRn Bit 3	DSITX n Video Enable Control – This bit enables video transmission from MIPI slave device to DSITX n when MIPI slave receive Video data.	0 = Disable 1 = Enable
TESMn Bit 4	DSITXn Error Status Mask – This bit enables the masking of error response received by DSITXn when it is selected for read operation.	0 = Disable Mask 1 = Enable Mask

VCn Bit 6-5	Virtual Channel ID for DSITXn – These bits specify the VC ID for the packets written by DSITXn.	
TRn Bit 7	Trigger Reset for DSITXn – This bit enables the DSI trigger reset function control feature on DSITXn. It is only valid when DSIn_EN is 1.	
TME n Bit 8	Trimming Enable for DSITXn – This bit starts the internal XOR calibration process and when the calibration is done, this bit will be auto clear and the status bit TMPn indicates that the calibration process is done. Note : TME n is only valid for first(DSI0CR) and second(DSI1CR) DSI.	
XRE n Bit 9	XOR Calibration Enable for DSITXn – This bit starts the internal XOR calibration process and when the calibration is done, this bit will be auto clear and the status bit TMPn indicates that the calibration process is done. Note : XRE n is only valid for first(DSI0CR) and second(DSI1CR) DSI. The DSI_ENn should be disabled first another re-calibration is required.	
XRSn Bit 10	XOR Calibration Select for DSITXn – This bit selects the internal byte data for calibration to be 8'hAA or 8'h55. Note : XRSn is only valid for first(DSI0CR) and second(DSI1CR) DSI.	
XRDn Bit 11	XOR Calibration Done for DSITXn – This bit indicates if the trimming process is done. This bit will be cleared when read. Note : XRDn is only valid for first(DSI0CR) and second(DSI1CR) DSI.	
TMPn Bit 12	Trimming Pass for DSITXn – This bit indicates if the trimming process is successful. It is valid when XRDn is set to 1. Note : TMPn is only valid for first(DSI0CR) and second(DSI1CR) DSI.	
TMDn Bit 13	Trimming Done for DSITXn – This bit indicates if the trimming process is done.	
DBGn Bit 14	Debug Select for DSITXn – This bit enables the debug control feature on DSITXn. It is only valid when DSIn_EN is 1.	
Reserved Bit 15		
RCTRn Bit 16	Analog Register Control for DSITXn – This bit enables the control of the XOR feedback tuning through register bit [7:1] or through Analog Test mode. This bit is used for internal testing and should be programmed to 0 for normal use.	0 = Controlled by Analog Test mode 1 = Controlled from Bit[7:1]
XTE n Bit 17	XOR Tune Enable for DSITXn – This bit enables the XOR Feedback Tuning when RCTRn is set.	0 = Disable 1 = Enable

	<p>This bit is used for internal testing and should be programmed to 0 for normal use.</p> <p>Note : XTEn is only valid for first(DSI0CR) and second(DSI1CR) DSI.</p>	
D0FEn Bit 18	<p>D0 Feedback Enable for DSITXn – This bit enables the XOR Feedback Tuning for lane 0 when RCTRn is set.</p> <p>This bit is used for internal testing and should be programmed to 0 for normal use.</p>	<p>0 = Disable 1 = Enable</p>
D1FEn Bit 19	<p>D1 Feedback Enable for DSITXn – This bit enables the XOR Feedback Tuning for lane 0 when RCTRn is set.</p> <p>This bit is used for internal testing and should be programmed to 0 for normal use.</p>	<p>0 = Disable 1 = Enable</p>
D2FEn Bit 20	<p>D2 Feedback Enable for DSITXn – This bit enables the XOR Feedback Tuning for lane 0 when RCTRn is set.</p> <p>This bit is used for internal testing and should be programmed to 0 for normal use.</p>	<p>0 = Disable 1 = Enable</p>
D3FEn Bit 21	<p>D3 Feedback Enable for DSITXn – This bit enables the XOR Feedback Tuning for lane 0 when RCTRn is set.</p> <p>This bit is used for internal testing and should be programmed to 0 for normal use.</p>	<p>0 = Disable 1 = Enable</p>
DFEn Bit 22	<p>Decoder Feedback Enable for DSITXn – This bit enables the Decoder Function when RCTRn is set.</p> <p>This bit is used for internal testing and should be programmed to 0 for normal use.</p>	
DXEn Bit 23	<p>Decoder XOR Enable for DSITXn – This bit enables the Decoder XOR Enable when RCTRn is set.</p> <p>This bit is used for internal testing and should be programmed to 0 for normal use.</p>	
Reserved Bit 31-24		

DSIn Video Register

DSInVR		DSIn Video Register								Offset Address
										[0x080+(n*32)] + 0x004
BIT	31	30	29	28	27	26	25	24		
NAME										
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
BIT	23	22	21	20	19	18	17	16		
NAME										
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
BIT	15	14	13	12	11	10	9	8		
NAME						HACTn[11:8]				
TYPE	RO	RO	RO	RO		RW				
RESET	0x0	0x0	0x0	0x0		0x04				
BIT	7	6	5	4	3	2	1	0		
NAME	HACTn[7:0]									
TYPE	RW									
RESET	0x00									

Table 10-20: DSIn Video Register Description

Name	Description	Setting
HACTn Bit 11-0	Horizontal Active Period for DSITXn –These bits specify the horizontal active period in terms of pixel clk of output video packet of DSITXn. The HACTn must be multiply of 64-bits, except the last DSITXn when there is more than 1 DSITX.	
Reserved Bit 31-12		

DSIn Ack Resp Register

DnARR		DSIn Ack Resp Register								Offset Address
										$[0x080+(n*32)] + 0x008$
BIT	31	30	29	28	27	26	25	24		
NAME										
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
BIT	23	22	21	20	19	18	17	16		
NAME										
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
BIT	15	14	13	12	11	10	9	8		
NAME	ARn[15:8]									
TYPE	RO									
RESET	0x00									
BIT	7	6	5	4	3	2	1	0		
NAME	ARn[7:0]									
TYPE	RO									
RESET	0x00									

Table 10-21: DSIn Ack Resp Register Description

Name	Description	Setting
ARn Bit 15-0	DSITXn Acknowledge Response – These bits specify the acknowledge response received.	
Reserved Bit 31-16		

DSIn Status Register

DnSR		DSIn Status Register								Offset Address
										[0x080+(n*32)] + 0x00C
BIT	31	30	29	28	27	26	25	24		
NAME										
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
BIT	23	22	21	20	19	18	17	16		
NAME										
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
BIT	15	14	13	12	11	10	9	8		
NAME		CRCEn	ECCE2_n	ECCE1_n	CONTn	VMMn	BE n	BAn		
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RO	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
BIT	7	6	5	4	3	2	1	0		
NAME	CSTn	DSTn	LPTOn	HSTOn	ATRn	ARRn	BTARn	RDRn		
TYPE	RO	RO	RW1C	RW1C	RW1C	RW1C	RW1C	RO		
RESET	0x1	0x1	0x0	0x0	0x0	0x0	0x0	0x0		

Table 10-22: DSIn Status Register Description

Name	Description	Setting
RDRn Bit 0	DSITXn Read Data Ready – This bit reflects whether the data from the MIPI slave is ready for read by the MIPI host controller. This bit is valid only during the read operation. This bit will be automatically cleared when all the received data are read out.	0 = Not ready 1 = Ready
BTARn Bit 1	DSITXn BTA Response – This bit reflects the DSITXn data lane status after DSITXn has made a BTA.	0 = The MIPI slave has not passed the lane authority back. 1 = The MIPI slave has passed the lane authority back.
ARRn Bit 2	DSITXn ACK Response Ready – This bit reflects whether the ACK response has been received or not by MIPI TX DSI_<n> TX. The ACK response can be an ACK trigger message or ACK with Error Report packet.	0 = Response has not been received. 1 = Response has been received.
ATRn Bit 3	DSITXn ACK Trigger Response – This bit reflects whether the ACK trigger message has been received or not by DSITXn.	0 = ACK trigger message has not been received. 1 = ACK trigger message has been received.
HSTOn Bit 4	DSITXn HS TX Time Out – This bit reflects the status of the HS TX timer for DSITXn.	0 = The HS TX timer has expired. 1 = The HS TX timer has not expired.
LPTOn Bit 5	DSITXn LP RX Time Out – This bit reflects the status of the LP RX timer for DSITXn.	0 = The LP RX timer has expired. 1 = The LP RX timer has not expired.
DSTn Bit 6	DSITXn Data Lane Status – This bit reflects the status at the MIPI Data lane for DSITXn.	0 = Data lane is not in LP-11. 1 = Data lane is in LP-11.
CSTn Bit 7	DSITXn Clock Lane Status – This bit reflects the status at the MIPI Clock lane for DSITXn.	0 = Clock lane is not in LP-11. 1 = Clock lane is in LP-11.
BAn Bit 8	DSITXn Command Buffer Available – This bit reflects the status of the DSITXn command buffer. If the buffer is not full, this bit will be set	0 = The command buffer is full. 1 = The command buffer is not

	to 1. The MIPI host controller can write at least 1 packet to the buffer.	full.
BE_n Bit 9	DSITX_n Command Buffer Empty – This bit reflects the status of the DSITX _n command buffer. If the buffer is empty, this bit will be set to 1. The MIPI host controller can write up to the maximum size of the buffer.	0 = The command buffer is not empty. 1 = The command buffer is empty.
VMM_n Bit 10	DSITX_n VC Mis-Match – This bit reflects whether there is a mismatch between the VC ID transmitted by the DSITX _n and the VC ID received from the MIPI slave.	0 = No mismatch 1 = Mismatch has occurred
CONT_n Bit 11	DSITX_n Contention – This bit reflects the status of the data lane contention detector.	0 = No contention 1 = Contention has occurred
ECCE1_n Bit 12	DSITX_n ECC Single Bit Error – This bit reflects the status of ECC checking for the packets received from the MIPI slave from DSITX _n . The status is valid only when the ECD bit is set to 0. Once an ECC single-bit error occurs, this bit will be set to 1. It will remain as 1 until the MIPI host controller writes 1 to clear it.	0 = No ECC single-bit error since this bit is cleared 1 = At least 1 ECC single-bit error since this bit is cleared
ECCE2_n Bit 13	DSITX_n ECC Multi Bit Error – This bit reflects the status of ECC checking for the packets received from the MIPI slave from DSITX _n . The status is valid only when the ECD bit is set to 0. Once an ECC multi-bit error occurs, this bit will be set to 1. It will remain as 1 until the MIPI host controller writes 1 to clear it.	0 = No ECC multi-bit error since this bit is cleared 1 = At least 1 ECC multi-bit error since this bit is cleared
CRCE_n Bit 14	DSITX_n CRC Error – This bit reflects the status of CRC checking for the packets received from the MIPI slave from DSITX _n . The status is valid only when the ECD bit is set to 0. Once a CRC error occurs, this bit will be set to 1. It will remain as 1 until the MIPI host controller writes 1 to clear it.	0 = No CRC error since this bit is cleared 1 = At least 1 CRC error since this bit is cleared
Reserved Bit 31:15		

DSIn Delay Control 1 Register

Offset Address

DSInDC1R

DSIn Delay Control 1 Register

[0x080+(n*32)] + 0x0010

BIT	31	30	29	28	27	26	25	24
NAME	D3_DELAY_SELn[6:0]							
TYPE	RW							
RESET	0x40							
BIT	23	22	21	20	19	18	17	16
NAME	D2_DELAY_SELn[6:0]							
TYPE	RW							
RESET	0x40							
BIT	15	14	13	12	11	10	9	8
NAME	D1_DELAY_SELn[6:0]							
TYPE	RW							
RESET	0x40							
BIT	7	6	5	4	3	2	1	0
NAME	D0_DELAY_SELn[6:0]							
TYPE	RW							
RESET	0x40							

Table 10-23: DSIn Delay Control 1 Register Description

Name	Description	Setting
D0_DELAY_SELn Bit 6-0	D0 Delay Select for DSITXn – These bits select the delay for the data lane 0. For n = 2, the effect of this delay will take effect when both DSI0DC1R[0x090] and DSI1DC1R[0x0B0] are programmed.	
Reserved Bit 7		
D1_DELAY_SELn Bit 14-8	D1 Delay Select for DSITXn – These bits select the delay for the data lane 1. For n = 2, the effect of this delay will take effect when both DSI0DC1R[0x090] and DSI1DC1R[0x0B0] are programmed.	
Reserved Bit 15		
D2_DELAY_SELn Bit 22-16	D2 Delay Select for DSITXn – These bits select the delay for the data lane 2. In 3-DSI mode, these values have no effect as only up to 2-lanes mode is supported.	
Reserved Bit 23		
D3_DELAY_SELn Bit 30-24	D3 Delay Select for DSITXn – These bits select the delay for the data lane 3. In 3-DSI mode, these values have no effect as only up to 2-lanes mode is supported.	
Reserved Bit 31		

DSIn Delay Control 2 Register

Offset Address

DSInDC2R

DSIn Delay Control 2 Register

[0x080+(n*32)] + 0x014

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME	MAX_SELn	MAX_1_3_SELn[6:0]						
TYPE	RW	RO						
RESET	0x0	0x40						
BIT	15	14	13	12	11	10	9	8
NAME		MAX_0_2_SELn[6:0]						
TYPE	RW	RO						
RESET	0x0	0x40						
BIT	7	6	5	4	3	2	1	0
NAME		CLK_DELAY_SELn[6:0]						
TYPE	RO	RW						
RESET	0x0	0x40						

Table 10-24: DSIn Delay Control 2 Register Description

Name	Description	Setting
CLK_DELAY_SELn Bit 6-0	Clock Delay Select for DSITXn – These bits select the delay for the clock lane. For n = 0 or 1, the effect of this delay will take effect when either DSI0DC1R[0x090] or DSI1DC1R[0x0B0] is programmed. For n = 2, the effect of this delay will take effect when both DSI0DC1R[0x090] and DSI1DC1R[0x0B0] are programmed.	
Reserved Bit 7		
MAX_0_2_SELn Bit 14-8	Max Select for lane 0 and 2 – These bits display the maximum delay calculated from XOR calibration for lane 0 or lane 2.	
Reserved Bit 15		
MAX_1_3_SELn Bit 22-16	Max Select for lane 1 and 3 – These bits display the maximum delay calculated from XOR calibration for lane 1 or lane 3.	
MAX_SELn Bit 23	Max Select for lane 2 and 3 – This bit select the MAX value for lane 2 and 3 when read from this register.	0 = Select Max value for lane 0 in [14:8] Max value for lane 1 in [22:16] when read. 1 = Select Max value for lane 2 in [14:8] Max value for lane 3 in [22:16] when read.
Reserved Bit 31-24		

11 Electrical Characteristics

MAXIMUM RATINGS

Table 11-1: Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{AVDD_RX}	Analog Core Power Supply for RX	-0.3 to 1.44	V
V_{AVDD_TX}	Analog Core Power Supply for TX	-0.3 to 1.44	V
V_{VDD_IO}	I/O Power Supply	-0.3 to 2.5	V
V_{VCL_CP}	Analog Power Supply	-0.3 to 2.5	V
V_{VCL_BG}	Analog Power Supply	-0.3 to 2.5	V
T_{SOL}	Solder Temperature / Time	225 for 40 sec max at solder ball	°C
T_{STG}	Storage Temperature	-40 to 150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits specified in the electrical characteristics tables and Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

RECOMMENDED OPERATING CONDITIONS

Table 11-2: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{AVDD_RX}	Analog Core Power Supply for MIPI RX	1.14	1.20	1.26	V
V_{AVDD_TX}	Analog Core Power Supply for MIPI TX	1.14	1.20	1.26	V
V_{VDD}	Digital Core Power Supply	1.14	1.20	1.26	V
V_{AVDD_PLL}	Analog PLL Power Supply	1.14	1.20	1.26	V
V_{VDD_IO}	I/O Power Supply	1.71	1.80	1.89	V
V_{VCL_CP}	Analog Power Supply for Charge Pump	1.71	1.80	1.89	V
V_{VCL_BG}	Analog Power Supply for Bandgap	1.71	1.80	1.89	V
T_A	Operating Temperature	-40	25	125	°C

DC Characteristics

Conditions

Voltage referenced to VSSIO = AVSS = VSSBG = VSSCP

AVDDR_X = AVDDT_X = V_{CORE} = 1.2V

VDDIO = VCICP = VCIBG = 1.8V

VDDRAM = 3.3V

T_A = 25°C

Table 11-3: DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ (*Estimated)	Max	Unit
I _{DD_1.2V_playback}	Active Mode (Playback)	1920x1080 Playback, white pattern MIPIRX@30Hz (command mode) MIPITX@60Hz (video mode)	-	110	170	mA
I _{DD_1.8V_playback}			-	4.5	8	mA
I _{DD_VDDRAM_playback}			-	9	20	mA
I _{DD_1.2V_still}	Active Mode (Still Image)	1920x1080 Self-Refresh MIPIRX Off MIPITX@60Hz (video mode)	-	89	150	mA
I _{DD_1.8V_still}			-	4.5	8	mA
I _{DD_VDDRAM_playback}			-	7	20	mA
I _{DD_1.2V_sleep}	Sleep Mode	MIPIRX and MIPITX Off. Entry by sending sleep in command (DCS cmd 10h) to SSD2858	-	14	17	mA
I _{DD_1.8V_sleep}			-	1	2	mA
I _{DD_VDDRAM_sleep}			-	26	150	μA
I _{DD_1.2V_pwrdown}	Power Down Mode	Power Down mode Internal 1.2V power is cut off and can be exit only by asserting reset	-	15	50	μA
I _{DD_1.8V_pwrdown}			-	1.3	10	μA
I _{DD_VDDRAM_pwrdown}			-	1	10	μA
V _{OH} (CMOS)	Output High Voltage (CMOS)	I _{OH} = -2 ~ -16 mA	1.44	-	-	V
V _{OL} (CMOS)	Output Low Voltage (CMOS)	I _{OL} = 2 ~ 16 mA	-	-	0.27	V
V _{IH} (CMOS)	Input High Voltage (CMOS)		1.26	-	-	V
V _{IL} (CMOS)	Input Low Voltage (CMOS)		-	-	0.36	V
I _{oZ}	Tri-state Output		-	±1	-	μA

	Leakage Current					
I_{IN}	Input Leakage Current	$V_{IN} = V_{DDIO}$ or V_{SS}	-	± 1	-	μA
C_{IN}	Input Capacitance		-	2.2	-	pF

12 AC Characteristics

RESET Timing

Table 12-1: RESET Timing

Symbol	Parameters	Min	Typ	Max	Units
T_{RESET}	RESET “Low” Pulse Width	20	-	-	ms

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