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1. Features

The features of BTL507212-W680L are as follows

- * Display mode : TFT 16M Colors, Transmissive, Normally Black
- * Driving Condition : 720x3Ch-Source / 1280Ch-Gate
- * Connection : ZIF Type (27Pins, FH26-27S-03SHW)
- * LCD Driver & Control IC : HX8394-A(HIMAX)
- * Back Light : White LED BackLight (12 Chips)
- * MPU Interface : MIPI 4-Lane
- * Type of Surface Contion : Clear Type

2. Mechanical Specifications

Item		Specification	Unit
Resolution	Main	720(x RGB) x 1280	Dot
	Sub	NA	
LCM Outline Demension		66.7x120.3x1.75(TYP.)	mm
Active Area (W x H)	Main	62.1x110.4	mm
	Sub	NA	
Pixel Pitch (W x H)	Main	0.08625x0.08625	mm
	Sub	NA	
Viewing Direction (Human Eye)	Main	Wide View	O'clock
	Sub	NA	
Gray Scale Inversion Direction (Contrast Ratio)	Main	Wide View	O'clock (Rubbing Direction)
	Sub	NA	
Weight		15	g

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3. Absolute Maximum Ratings

(Ta=25°C Note1)

Items	Symbol	Min.	Max.	Unit	Remark
Logic voltage	I_{OVCC}	-0.3	4.4	V	
Analog voltage	V_{CI}	-0.3	4.4	V	
Input signal voltage	V_{IN}	-0.3	$I_{OVCC}+0.3$	V	
LED forward current	I_{LED}	20	25	mA	For each LED
Operation temperature	T_{OPR}	-20	70	°C	
Storage temperature	T_{STG}	-30	80	°C	
Humidity (ambient temperature= T_a)	$T_a \leq 60^\circ\text{C}$		90% RH Max.		

Note1 : Device is subject to be damaged permanently,
if stresses beyond those absolute maximum ratings listed above.

4. Electrical Characteristics

Main		Ta=25°C					
Items	Symbol	Min.	Typ.	Max.	Unit	Remark	
Logic voltage	I_{OVCC}	1.65	1.8/2.8	3.6	V		
Analog(Power) voltage	V_{CC}	2.72	2.8	2.88	V		
Gate voltage	High level	V_{GH}	10	-	13	V	Note 1
	Low level	V_{GL}	-13	-	-10	V	
Input signal voltage	High level	V_{IH}	$0.8 \times IOVCC$	-	$IOVCC$	V	
	Low level	V_{IL}	0	-	$0.2 \times IOVCC$	V	
Current consumption	I_{CC}	-	45	67.5	mA	Note 2	

Note 1) The value can be adjusted by software to optimize display quality

Note 2) Display White Pattern

5.Recommended Software Setting Value (LDI: HX8394-A)

NOTE: BOE requires the customer to follow the above instructions strictly. If customer would like to change the above instructions,the customer should inform BOE and get re-check from BOE, or the customer will be responsible for any unexpected result because of the change.

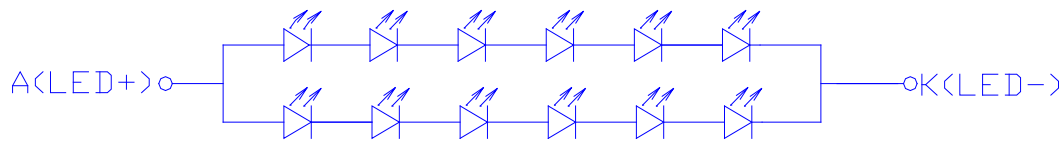
6. Back Light System Characteristics

Ta=25°C

Items	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward current	If	-	20	-	mA	Note1
Forward voltage	Vf	3.0	-	3.4	V	Note1
B/L Power consumption	P_{BL}	-	-	816	mW	Note2

Note 1: The Driving condition is defined for each LED chip.

Note 2: The B/L Power consumption is defined for the backlight module.the schematic drawing of the backlight module as the figure.



Ref. Total power consumption(max) depends on LED current/ LED driver efficiency, etc.

7. Optical Characteristics

Transmissive Mode

Ta=25°C

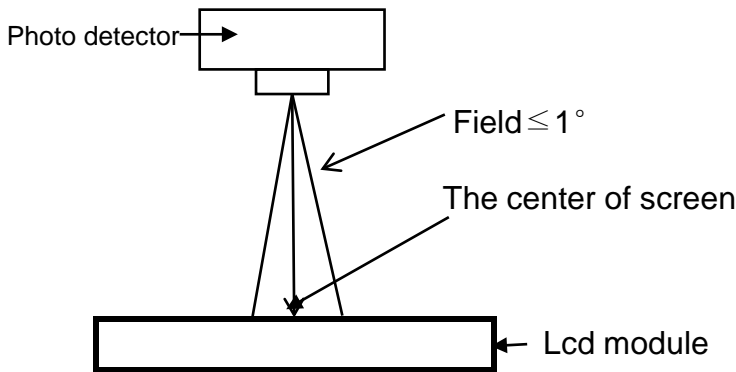
Item	Symbol	Min.	Typ.	Max.	Unit	Condition	Note	
Viewing Angle	θ	$\theta=0^\circ$ (X1)	70	80	-	deg.	Cr > 10	Note2
		$\theta=180^\circ$ (X2)	70	80	-			
		$\theta=90^\circ$ (Y1)	70	80	-			
		$\theta=270^\circ$ (Y2)	70	80	-			
Contrast ratio (transmissive)	Cr	600	900	-	-	$\theta = 0$	Note1 Note4	
Response Time	Tr + Tf	30	35	-	ms	$\theta = 0$	Note3	
CIE Coordinate	R	(x,y)	0.62,0.30	0.65,0.33	0.68,0.36	$\theta = 0$		
	G	(x,y)	0.26,0.59	0.29,0.62	0.32,0.65			
	B	(x,y)	0.11,0.05	0.14,0.08	0.17,0.11			
	W	(x,y)	0.25,0.29	0.28,0.32	0.31,0.35			
Brightness	L	400	450	-	cd/m ²	20mA/LED	Note5	
Uniformity		80		-		20mA/LED	Note6	

* $\theta = 0^\circ$, $\theta = 90^\circ$, $\theta = 180^\circ$, $\theta = 270^\circ$ means viewing direction.

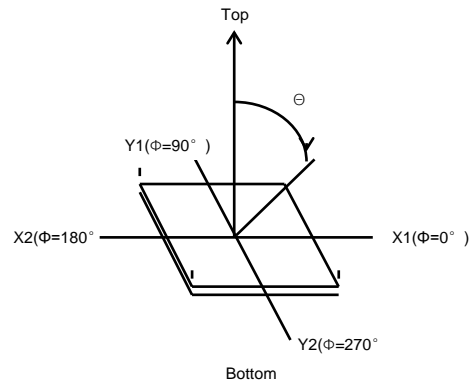
* B/L is turned on.

The optical characteristics should be measured in dark room, and after 5 minutes operation, the measurement begin.

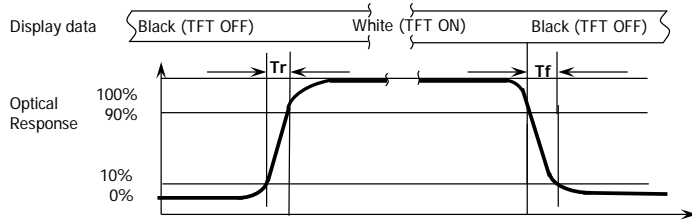
Note1. Definition of Measure System



Note2. Definition of Angle Θ .



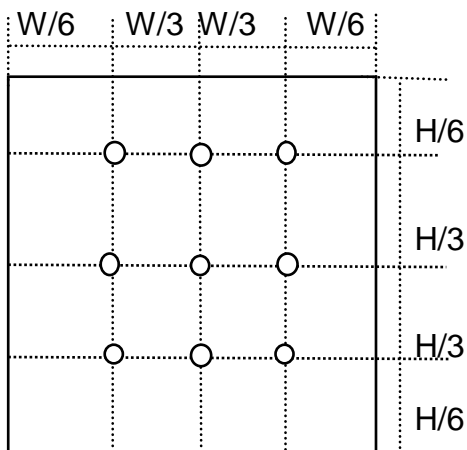
Note3. Definition of Response Time



Note4.definition of contrast ratio

$$Cr = \frac{\text{Luminance of LCD White state}}{\text{Luminance of LCD Black state}}$$

Note 5. Measuring Point(9 Points) (WxH)

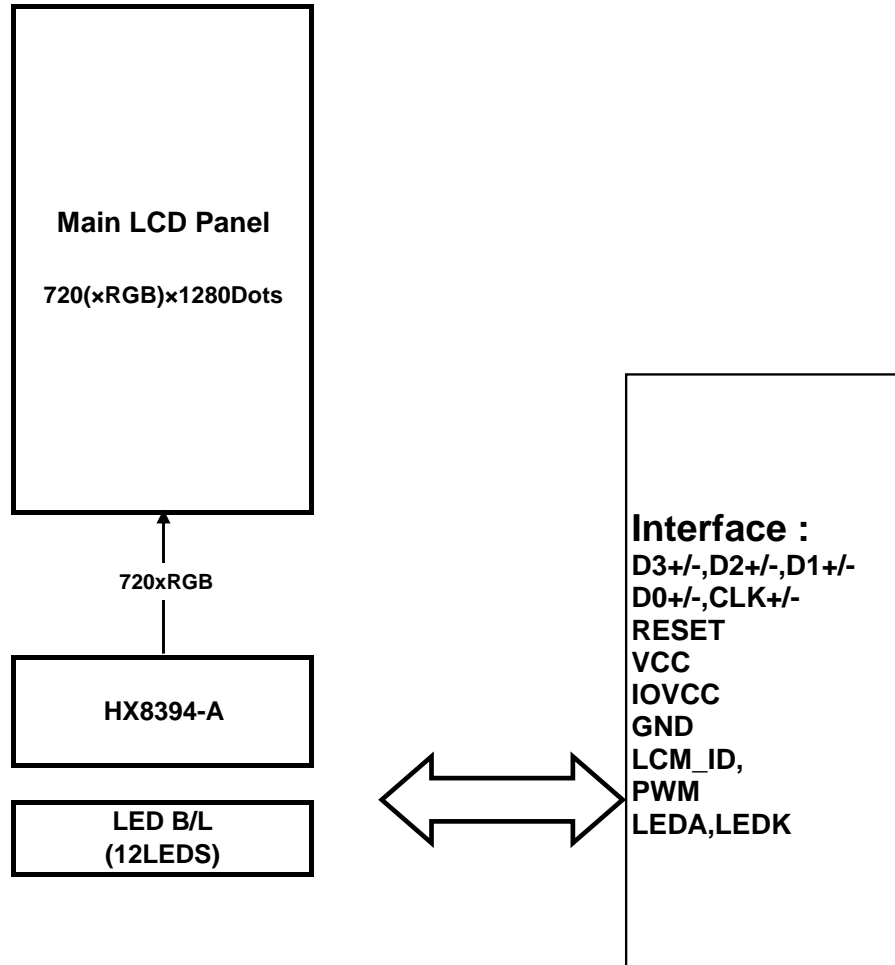


Rating is defined as the average brightness inside the viewing area

Note 6. definition of Uniformity

$$\text{Uniformity} = \frac{\text{min. Luminance of measured point}}{\text{max. Luminance of measured point}}$$

8. Block Diagram



9. Interface Pin Assignment

No	Symbol	Description
1	LED+(A)	LED Anode(+)
2	LED-(K)	LED Cathode(-)
3	GND	Ground
4	TE	NC
5	RESET	RESET
6	IOVCC	Power Supply for Internal Logic (1.8V/2.8V)
7	VCC	Power Supply (2.8V)
8	LCM_ID(1.4V)	Identify Signal(1.4V)
9	GND	Ground
10	GND	Ground
11	DSI_D0N	MIPI DATA LANE
12	DSI_D0P	MIPI DATA LANE
13	GND	Ground
14	DSI_D1N	MIPI DATA LANE
15	DSI_D1P	MIPI DATA LANE
16	GND	Ground
17	DSI_CN	MIPI CLOCK LANE
18	DSI_CP	MIPI CLOCK LANE
19	GND	Ground
20	DSI_D2N	MIPI DATA LANE
21	DSI_D2P	MIPI DATA LANE
22	GND	Ground
23	DSI_D3N	MIPI DATA LANE
24	DSI_D3P	MIPI DATA LANE
25	GND	Ground
26	LEDPWM	CABC PWM OUTPUT
27	NC	NC

10. Power Supply Sequence

VDD1, VDD2 and VDD3 can be applied in any order. VDD1, VDD2 and VDD3 can be powered down in any order. During power off, if LCD is in the Sleep Out mode, VDD1 and VDD2 must be powered down minimum 120msec after RESX has been released. During power off, if LCD is in the Sleep In mode, VDD1, VDD2 and VDD3 can be powered down minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence. If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.11.1 and 5.11.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed. The power on/off sequence is illustrated below.

11. Timing Characteristics (MIPI)

The Electrical Characteristics of D-PHY Layer

In general, the DSI D-PHY may contain the following electrical functions: High-Speed Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). Figure 8.6 shows the complete set of electrical functions required for a fully featured PHY transceiver.

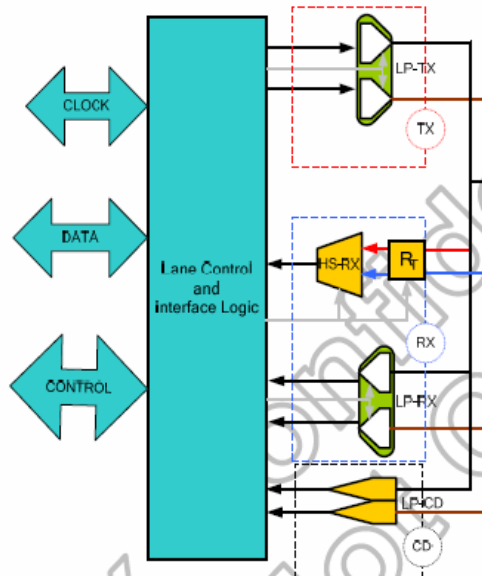


Figure 8.6: Electrical functions of a fully D-PHY transceiver

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. The Figure 8.7 shows both the HS and LP signal levels on the left and right sides, respectively.

Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

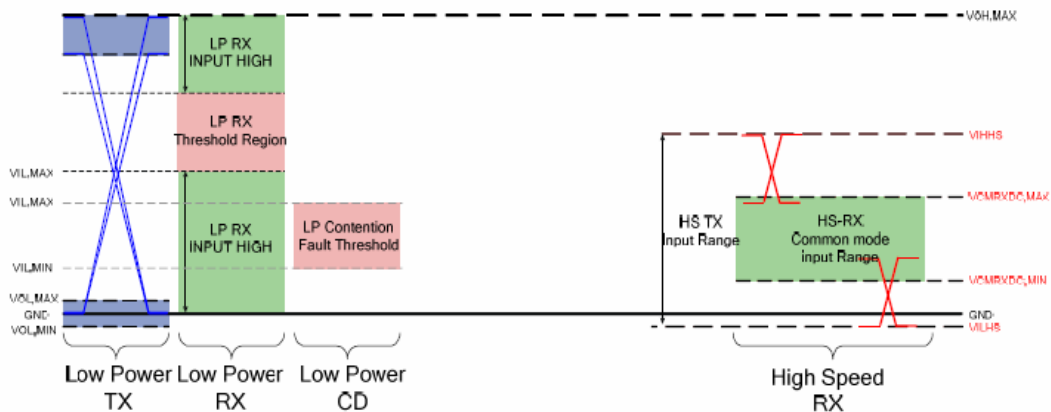


Figure 8.7: Shows both the HS and LP signal levels

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The Electrical Characteristics of Low-Power Transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes. It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tables list DC and AC characteristic for LP-TX

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OL}	Thevenin output low level	-50	-	50	mV	-
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1) Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 8.8: LP Transmitter DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
$\delta V/\delta t_{SR}$	Slew rate @ $C_{LOAD} = 0pF$	-	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ $C_{LOAD} = 5pF$	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ $C_{LOAD} = 20pF$	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ $C_{LOAD} = 70pF$	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ $C_{LOAD} = 0$ to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
	Slew rate @ $C_{LOAD} = 0$ to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ $C_{LOAD} = 0$ to 70pF (Rising Edge Only)	30 – 0.075 * ($V_{O,INST} - 700$)	-	-	mV/ns	(1),(8),(9)
C_{LOAD}	Load capacitance	0	-	70	pF	-

Note: (1) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be $<10pF$. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

(2) When the output voltage is between 400 mV and 930 mV.

(3) Measured as average across any 50 mV segment of the output signal transition.

(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.

(5) This value represents a corner point in a piecewise linear curve.

(6) When the output voltage is in the range specified by VPIN(absmax).

(7) When the output voltage is between 400 mV and 700 mV.

(8) Where $V_{O,INST}$ is the instantaneous output voltage, VDP or VDN, in millivolts.

(9) When the output voltage is between 700 mV and 930 mV.

Table 8.9: LP Transmitter AC Specifications

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The Electrical Characteristics of High-Speed Receiver

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, Z_{ID} , between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 8.10: HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV _{pp}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.

(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 8.11: HS Receiver AC Specifications

The Electrical Characteristics of Low-Power Receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSpike. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The related diagram shows as Figure 8.4 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

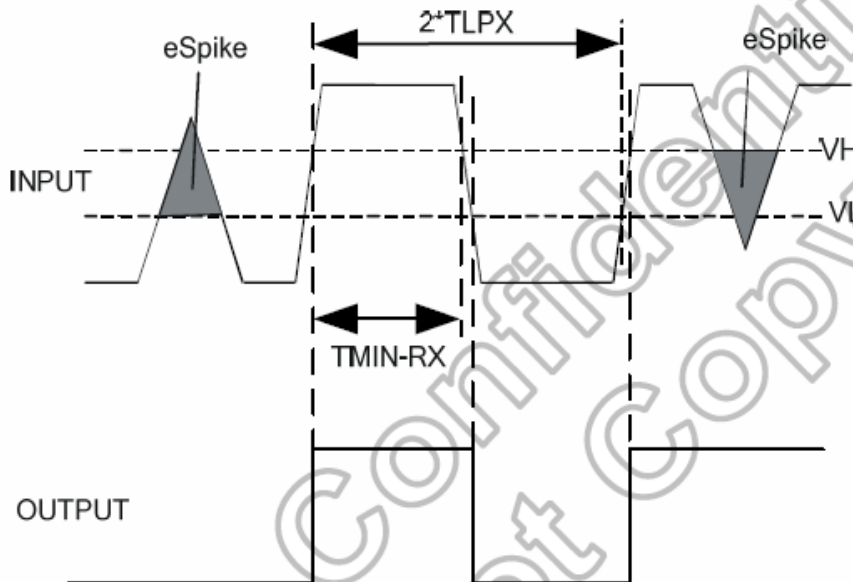


Figure 8.8: Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IL}	Logic 0 input threshold	-	-	550	mV	-
V_{IH}	Logic 1 input threshold	880	-	-	mV	-

Table 8.12: LP Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

Table 8.13: LP Receiver AC Specifications

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Line Contention Detection

Contention can be inferred from any of the following conditions:

- A. An LP high fault shall be detected when the LP transmitter is driving high and the pin voltage is less than V_{IL} .
- B. An LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than V_{IL} .

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

Table 8.14: Contention Detector DC Specifications

High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CP – CN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 8.5.

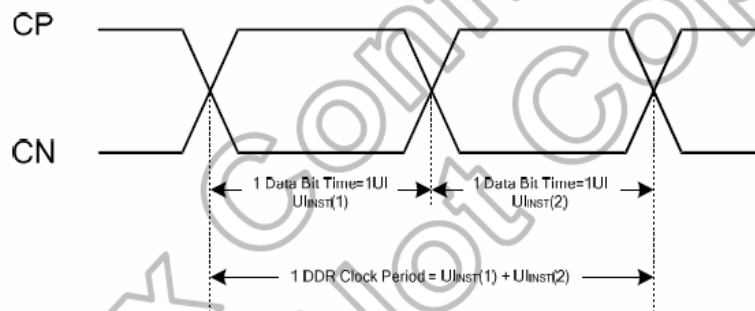


Figure 8.9: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

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High-Speed Data-Clock Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	U_{INST}	-	-	12.5	ns	(1), (2), (3), (4)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.

(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

(3) Maximum total bit rate is 1.5Gbps of 3 data lanes 24-bit data format/ 1.12Gbps of 3 data lane 18-bit data format/ 1Gbps of 3 data lane 16-bit data format.

(4) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

Table 8.15: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.10. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

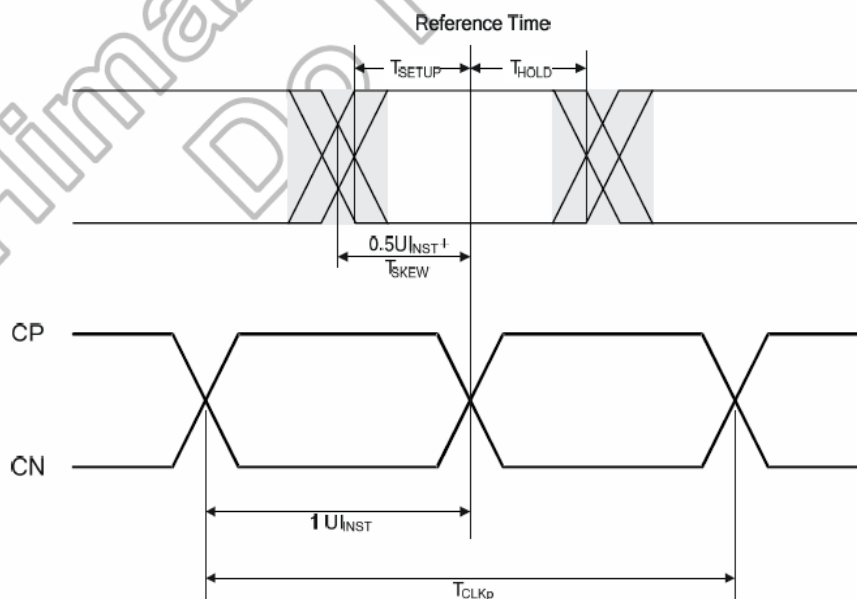


Figure 8.10: Data to Clock Timing Definitions

Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 8.16. Implementers shall specify a value $U_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.16 are specified as a part of this value. The skew specification, $T_{SKEW[TX]}$, is the allowed deviation of the data launch time to the ideal $\frac{1}{2}U_{INST}$ displaced quadrature clock edge. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4 \cdot U_{INST}$, i.e. $\pm 0.2 \cdot U_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [Receiver]	$T_{SETUP[RX]}$	0.15	-	-	U_{INST}	1
Clock to Data Hold Time [Receiver]	$T_{HOLD[RX]}$	0.15	-	-	U_{INST}	1

Note: (1) Total setup and hold window for receiver of $0.3 \cdot U_{INST}$.

Table 8.16: Data to Clock Timing Specifications

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Timings for DSI Video mode

Vertical Timings

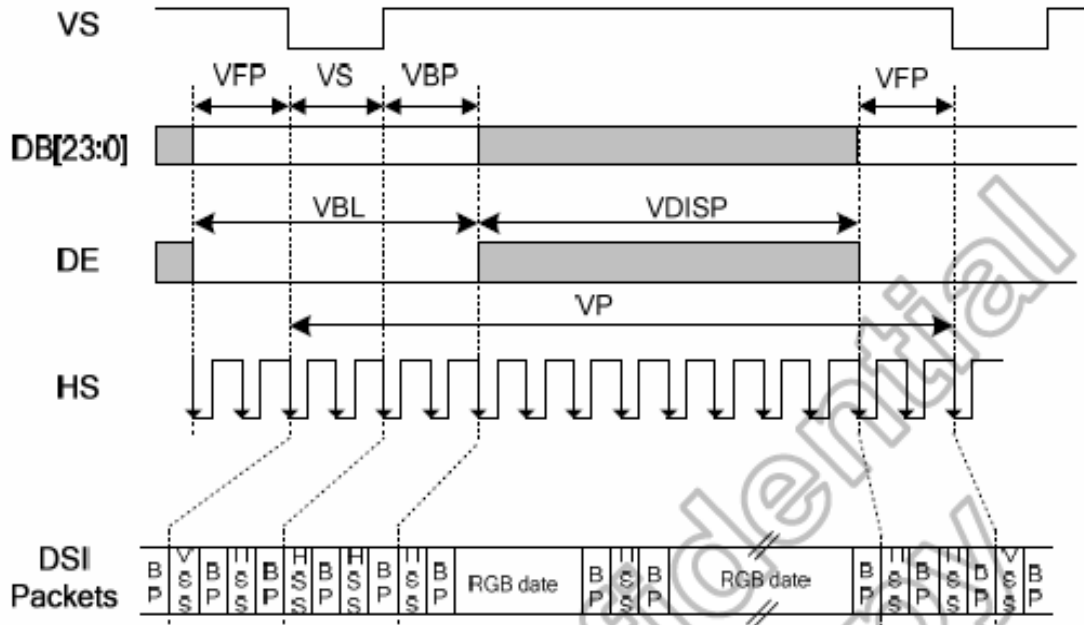


Figure 8.11: Vertical Timings for DPI I/F

Resolution=800x1280(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	1286	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical data start point	-	VS+VBP	4	-	Note(1)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GSP and GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display.

Table 8.17: Vertical Timings for DPI I/F

Timings for DSI Video mode

Horizontal Timings

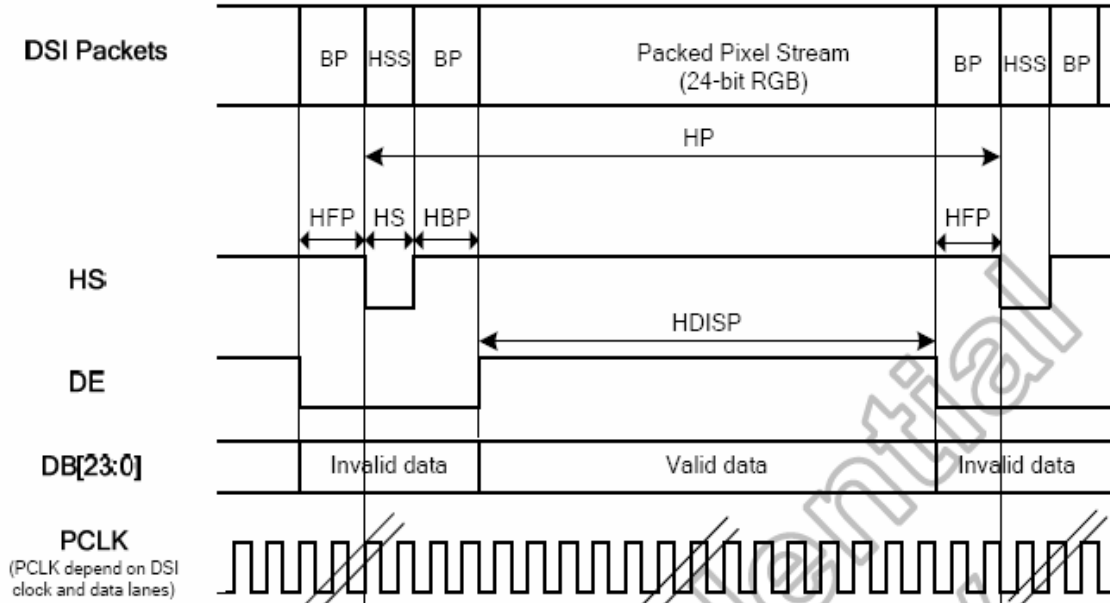


Figure 8.12: Horizontal Timing for DSI Video mode I/F

Resolution=800x1280 (VSSA=0V, VDD1=1.8V, VDD2=VDD3=HS_VCC=2.8V, T_A=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	-	815	-	888	DCK
HS low pulse width	HS	-	5	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal data start point	-	HS+HBP	10	-	83	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	15	-	88	DCK
Horizontal active area	HDISP	-	-	800	-	DCK

Table 8.18: Horizontal Timings for DSI Video mode I/F

3) Reset Timing characteristics

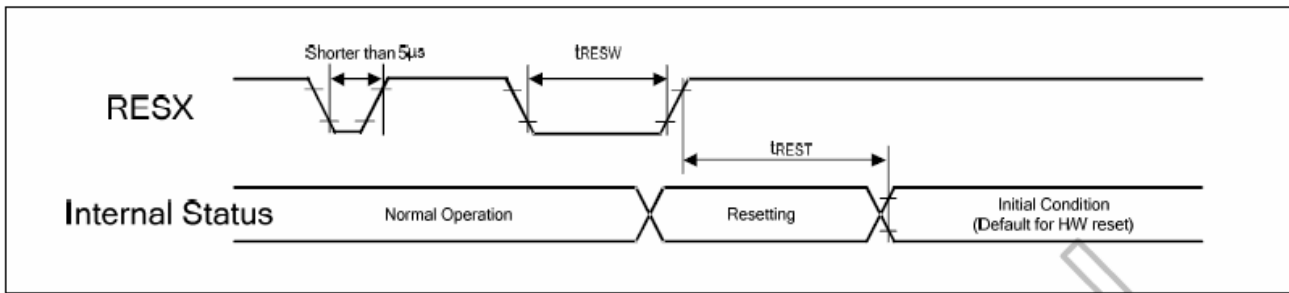


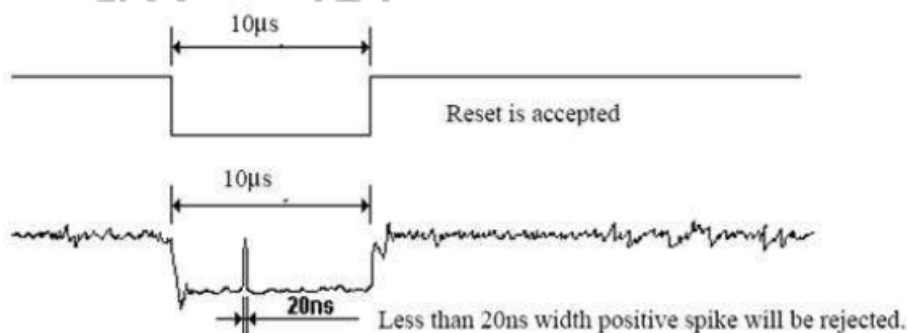
Figure 8.5: Reset input timing

Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width ⁽¹⁾	RESX	10	-	-	-	μs
t_{REST}	Reset complete time ⁽²⁾	-	5	-	-	When reset is applied during Sleep In mode	ms
		-	120	-	-	When reset is applied during Sleep Out mode	ms

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for HW reset.
- (3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is HW reset complete time (t_{REST}) within 5ms after a rising edge of RESX.
- (4) Spike Rejection also applies during a valid reset pulse as shown below:

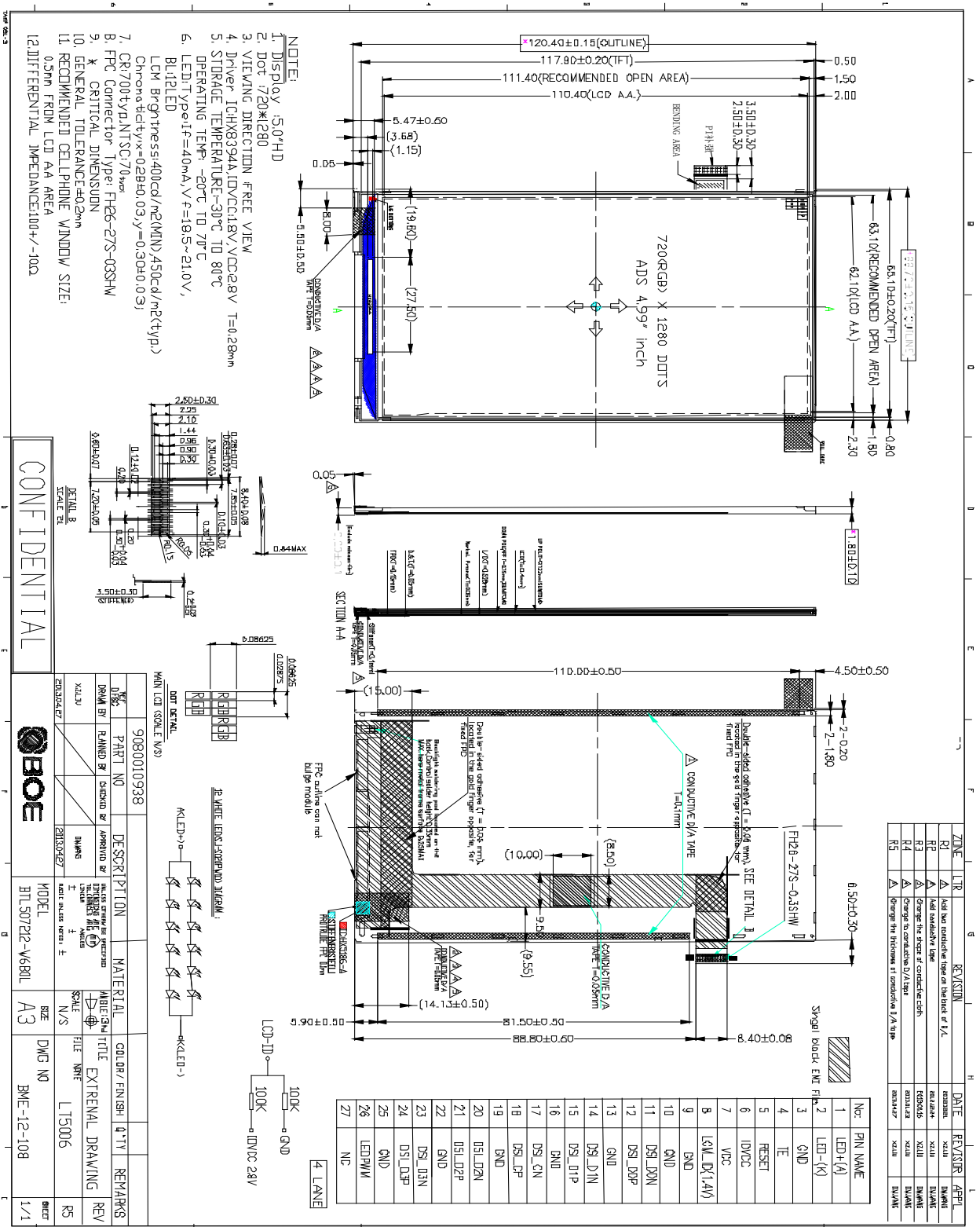


- (5) When Reset is applied during Sleep In Mode.
- (6) When Reset is applied during Sleep Out Mode.
- (7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Table 8.7: Reset timing

Model	BTL507212-W680L	24/36	PRODUCT SPECIFICATION
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12. External Dimension



CONFIDENTIAL



MODEL	BTL507212-W680L	SIZE	A3	DWG NO	BME-12-108
REV	1/1	EXT. DRAWING	FILE NAME	L15006	SCALE

13. Color LCD Module Numbering System

B	T	L	5	0	7	2	1	2	-	W		6	8	0	L		
(1)	(2)	(3)	(4)	(5)			(6)	(7)		(8)	(9)	(10)					

(1) B: BHL

(2) Drive System

C: CSTN T: TFT E: OLED M: MONO

(3) Product Status

L: LCD Model F: FOG Model G: COG Model P: PANEL Model C: CELL Model

(4) Display size(精确到小数点后1位,四舍五入)

EX) 2.22 inch:22 1.76 inch:18 2.0 inch:20 10.1inch:A1
1.9 inch:19 1.12 inch:11 1.8 inch:18 15.5inch:F5

(5) Resolution

Number of Row Dots * Number of column Dots(前两位有效)

EX) 128 * 128 = 1212 96 * 64 = 9664 128 * 160 = 1216 101 * 80 = 1080
176 * 220 = 1722 128 * 96 = 1296 320 * 240 = 3224 1024 * 576 = 1057

(6) Viewing Direction

Nil: 6 H U: 12 H L: 9 H R: 3 H W: Wide view E: 其他

(7) Serial Number (*001-9999: 按照产品状态, 各类产品序列号实行大排行处理, *为0时省略不写)

(8) Back Light

Nil: Without backlight + Reflective H: CCFL + Translective
T: Without backlight + Transflective E: LED Frontlight + Reflective
F: CCFL Frontlight + Reflective D: LED + Transflective
L: LED + Transmissive

(9) DUAL LCD

Nil: Single LCD M: MONO C: CSTN T: TFT O: OLED

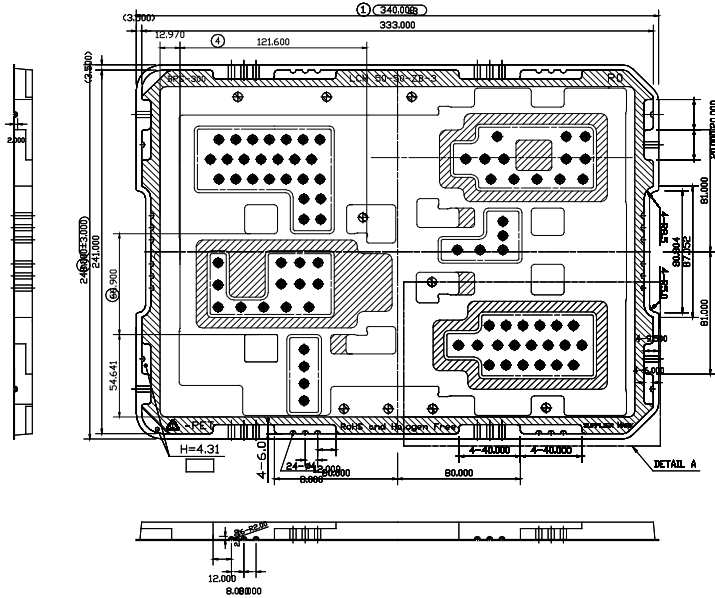
(10) TOUCH PANEL

Nil: Without TP P: with TP

Model	BTL507212-W680L	26/36	PRODUCT SPECIFICATION
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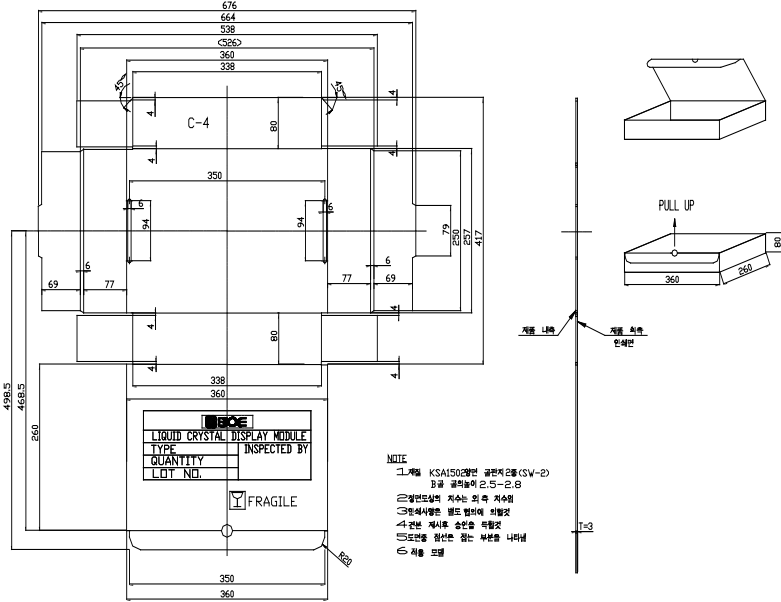
14. Package Terms

- 1、Tray Size
 L:340mm
 W:248mm
 (3PCS LCM/Tray)



Tray Drawing

- 2、Inner BOX Size
 L:360mm
 W:260mm
 H:80mm
 (9PCS Tray) / Inner Box)

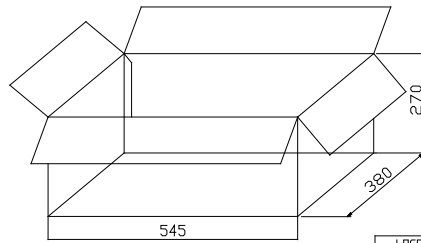
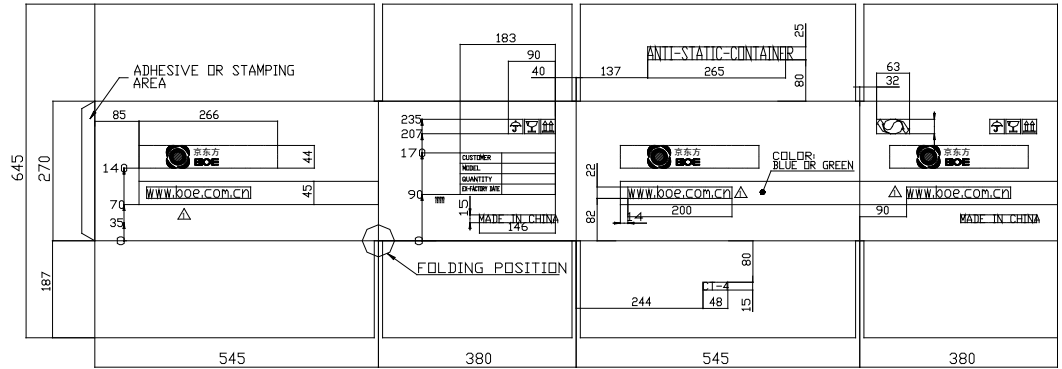


Inner Box Drawing

Model	BTL507212-W680L	27/36	PRODUCT SPECIFICATION
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3、Out BOX Size

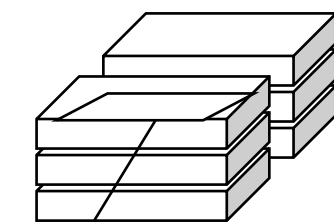
L: 545mm
W: 380mm
H: 270mm
(6pcs Inner / Out)



NOTE
1.MATERIAL: KSA 1531,DW2(CT=8mm)
2.DRAWING DIMENSIONS ARE EQUAL TO OUTSIDE DIMENSION.
3.INNER BOX(C-4) ARRANGEMENT: 3STEPS X2ROWS
4.MARKS ARE REFER TO SEPERATE CONSULTATION.

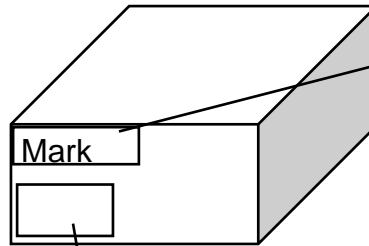
LOGO	COLOR
	BLUE OR GREEN
WWW.BOE.COM.CN	CLEARNESS
OTHERS	BLUE OR GREEN

4、Packing label content



HYE LCD		
LIQUID CRYSTAL DISPLAY MODULE		
TYPE		INSPECTED BY
QUANTITY	EA	
LOT NO		

Inner Box



HYE LCD Hyundai LCD Inc			
CUSTOMER		QTY	
MODEL		DATE	YYYY-MM-DD
RUN NO		LOC CODE	
ORIGIN		(QA)	

OUT BOX

Custmer Address
Product No.
P/O No.
LOT NO.
Box No.

Mark Item

5、Packing notice

- [1]Sub LCD should be placed upwardly while in the tray.
- [2] Every seven full trays with a blank one while twining twice on both sides by adhesive tape.
- [3].Every tray should be put crossedly.

6、Product label

- [1] There should be Logo and product modle of BOE on FPC ASS'Y.

7、Packing Q'ty list

	INNER BOX	TRAY	MODULE
OUT BOX	6	54	144
INNER BOX	1	9	24
TRAY	-	1	3

Model	BTL507212-W680L	28/36	PRODUCT SPECIFICATION
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1.LCD Module Out-Going Quality Level

(1.0) Purpose

The LCD specification provides outgoing provision and its expected quality level based on our outgoing inspection of LCD.

(2.0) Applicable Scope

The LCD specification is applicable to the arrangement in regard to outgoing Inspection and quality assurance after it.

(3.0) Quality Specification

(3.1) Quality Level

The quality level of BHL&BMDT are based on GB/T2828.1-2003, Apply Level II, normal inspection by single sampling.

Rank	Item	AQL	Note
Major(MA)	Parts Short, Parts Mounting Back Light, Open Solder Bridging Outside Dimension Solder Ball, Cold Solder	0.65	
Minor (MI)	Stains on LCD Panel Surface Color Variation Stains, Scratches, Foreign Substance, Spots, Air Bubbles, Parts Alignment	1.0	

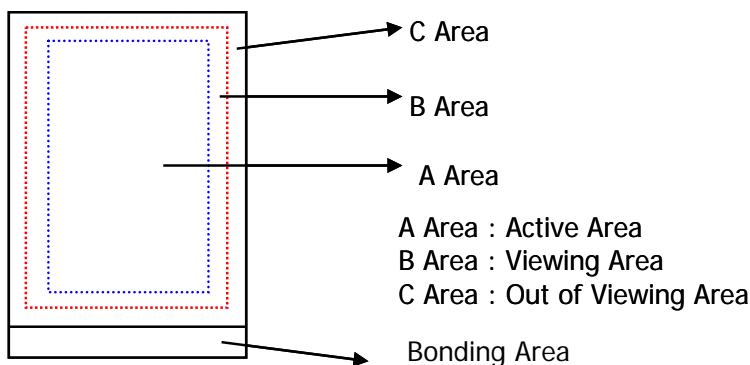
(3.2) Appearance Standards

1) Inspection Conditions

The inspection shall be applied under 20W white fluorescent lamp light at a distance between 400-500mm, with the eyes 300mm away from products and and the angle of view within 30° to perpendicular line.

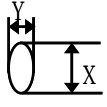
The mobile lens should be fixed on when doing inspection in case the mobile with l

2) Definition of the Area



Model	BTL504885-W640L	29/36	PRODUCT SPECIFICATIONS
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(3.3) Appearance Spec

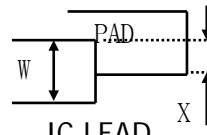
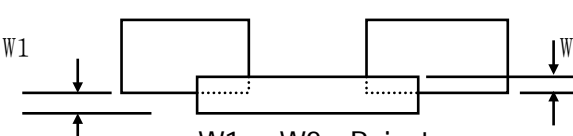
No	Item	Criteria	Rank	Remark																						
1	Parts Short	Not allowed	MA																							
2	Solder Bridging	Any bridging between components, except common circuit, is not allowed	MA																							
3	Outside Dimension	Drawing & specification must be within permissible tolerance	MA																							
4	Open	Not allowed	MA																							
5	Cold Solder	Not allowed	MA																							
6	Stains On LCD Panel Surface	<p>Stains which can be wiped off with soft cloth are counted as defect</p> <p>Stains which can't be removed even with soft cloth are not allowed</p>	MI	 <p>Diameter (X + Y)/2</p>																						
7	Back Light	No light and short of light and abnormal lighting are not allowed	MA																							
8	Air Bubbles Between Glass & Polarizer (Polarizer Defects)	<table border="1"> <thead> <tr> <th rowspan="2">Area Dimension**</th> <th colspan="2">Acceptable Q'ty</th> <th rowspan="2">Remark</th> </tr> <tr> <th>A Area</th> <th>B Area</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.15$</td> <td colspan="2">Ignore</td> <td rowspan="5"></td> </tr> <tr> <td>$0.15 < \Phi \leq 0.30$</td> <td>3</td> <td>Ignore</td> </tr> <tr> <td>$0.30 < \Phi \leq 0.50$</td> <td>2</td> <td>Ignore</td> </tr> <tr> <td>$0.50 < \Phi \leq 0.70$</td> <td>1</td> <td>Ignore</td> </tr> <tr> <td>Total</td> <td>5</td> <td>Ignore</td> </tr> </tbody> </table>	Area Dimension**	Acceptable Q'ty		Remark	A Area	B Area	$\Phi \leq 0.15$	Ignore			$0.15 < \Phi \leq 0.30$	3	Ignore	$0.30 < \Phi \leq 0.50$	2	Ignore	$0.50 < \Phi \leq 0.70$	1	Ignore	Total	5	Ignore	MI	
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$0.50 < \Phi \leq 0.70$	1	Ignore																								
Total	5	Ignore																								

Model

BTL504885-W640L

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PRODUCT SPECIFICATIONS

No	Item	Criteria	Rank	Remark																																													
9	Parts Mounting	Parts mounting failure is not allowed Wrong parts mounted is not allowed	MA																																														
10	Stains Foreign Substance Scratches Spots	<p>(1) Round shape</p> <table border="1"> <thead> <tr> <th rowspan="2">Area Dimension</th> <th colspan="2">Acceptable Q'ty</th> <th rowspan="2">Remark</th> </tr> <tr> <th>A Area</th> <th>B Area</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.10$</td> <td colspan="2">Ignore</td> <td rowspan="4"></td> </tr> <tr> <td>$0.10 < \Phi \leq 0.20$</td> <td>2</td> <td>Ignore</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.30$</td> <td>1</td> <td>Ignore</td> </tr> <tr> <td>$0.30 < \Phi$</td> <td>0</td> <td>Ignore</td> </tr> </tbody> </table> <p>(2) Line shape</p> <table border="1"> <thead> <tr> <th colspan="2">Dimension</th> <th colspan="2">Acceptable Q'ty</th> <th rowspan="2">Remark</th> </tr> <tr> <th>Length</th> <th>Width</th> <th>A Area</th> <th>B Area</th> </tr> </thead> <tbody> <tr> <td>-</td> <td>≤ 0.025</td> <td colspan="2">Ignore</td> <td rowspan="4"></td> </tr> <tr> <td>≤ 2.5</td> <td>≤ 0.05</td> <td>3</td> <td>Ignore</td> </tr> <tr> <td>≤ 1.5</td> <td>≤ 0.075</td> <td>2</td> <td>Ignore</td> </tr> <tr> <td></td> <td>$0.075 <$</td> <td colspan="2">Follow round shape</td> </tr> </tbody> </table> <p>(1) & (2) total defect q'ty can not exceed 5</p>	Area Dimension	Acceptable Q'ty		Remark	A Area	B Area	$\Phi \leq 0.10$	Ignore			$0.10 < \Phi \leq 0.20$	2	Ignore	$0.20 < \Phi \leq 0.30$	1	Ignore	$0.30 < \Phi$	0	Ignore	Dimension		Acceptable Q'ty		Remark	Length	Width	A Area	B Area	-	≤ 0.025	Ignore			≤ 2.5	≤ 0.05	3	Ignore	≤ 1.5	≤ 0.075	2	Ignore		$0.075 <$	Follow round shape		MI	
Area Dimension	Acceptable Q'ty			Remark																																													
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≤ 2.5	≤ 0.05	3	Ignore																																														
≤ 1.5	≤ 0.075	2	Ignore																																														
	$0.075 <$	Follow round shape																																															
11	Color Variation	Refer to the limit sample consented by both parties for judgement	MI																																														
12	Solder Ball	1)Acceptable if the size of void is less than $\Phi 0.13\text{mm}$ 2)Acceptable if a solder ball is up to $\Phi 0.2\text{mm}$ but on shield space	MA																																														
13	Parts Alignment	<p>1)Acceptable if it dose not exceed 50% of the lead width IC</p>  <p>$X \leq W/2$: Accept $X > W/2$: Reject</p> <p>IC LEAD</p> <p>2)Rejectable, provided that it does exceed 50% of the component termination width</p>  <p>$W1 > W2$: Reject</p>	MI																																														

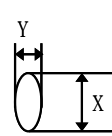
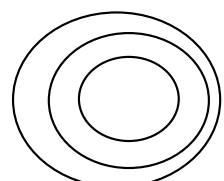
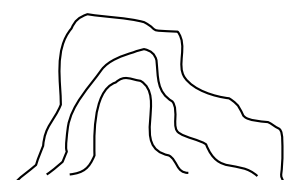
Note : A limitation sample is given top priority

(4.0) Specification for Touch Panel Inspection

(4.1) Inspection Criterion and Level

Rank	Item	AQL	Note
Major (MA)	Function Failure	0.65	
Minor (MI)	Bubble, Scratch, Foreign Particle Newton Ring	1.0	

(4.2) Inspection Criterion

No	Item	Criteria	Rank	Note																																																				
1	Function	Fail to adjust, hard to adjust (can't be adjusted within 3 times): Reject Stroke Drift, Stroke Suspension: Reject	MA																																																					
2	Air Bubble Scratch Foreign Particle	<p>1) Round shape</p> <table border="1"> <thead> <tr> <th rowspan="2">Dimension</th> <th colspan="2">Acceptable Q'ty</th> <th rowspan="2">Remark</th> </tr> <tr> <th>A area</th> <th>B area</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.10$</td> <td colspan="2">Ignore</td> <td></td> </tr> <tr> <td>$0.10 < \Phi \leq 0.20$</td> <td>2</td> <td>Ignore</td> <td></td> </tr> <tr> <td>$0.20 < \Phi \leq 0.30$</td> <td>1</td> <td>Ignore</td> <td></td> </tr> <tr> <td>$0.30 < \Phi$</td> <td>0</td> <td>Ignore</td> <td></td> </tr> </tbody> </table> <p>2) Line shape</p> <table border="1"> <thead> <tr> <th colspan="2">Dimension</th> <th colspan="2">Acceptable Q'ty</th> <th rowspan="2">Remark</th> </tr> <tr> <th>length</th> <th>Width</th> <th>A area</th> <th>B area</th> </tr> </thead> <tbody> <tr> <td>-</td> <td>$W \leq 0.025$</td> <td colspan="2">Ignore</td> <td rowspan="4">Ignore</td> </tr> <tr> <td>$L \leq 3.0$</td> <td rowspan="2">$W \leq 0.05$</td> <td colspan="2">Ignore</td> </tr> <tr> <td>$3.0 < L \leq 5.0$</td> <td colspan="2">2</td> </tr> <tr> <td>≤ 7</td> <td>$W \leq 0.1$</td> <td colspan="2">1</td> </tr> <tr> <td>-</td> <td>$W > 0.1$</td> <td colspan="2">Follow Round shape</td> <td></td> </tr> </tbody> </table>	Dimension	Acceptable Q'ty		Remark	A area	B area	$\Phi \leq 0.10$	Ignore			$0.10 < \Phi \leq 0.20$	2	Ignore		$0.20 < \Phi \leq 0.30$	1	Ignore		$0.30 < \Phi$	0	Ignore		Dimension		Acceptable Q'ty		Remark	length	Width	A area	B area	-	$W \leq 0.025$	Ignore		Ignore	$L \leq 3.0$	$W \leq 0.05$	Ignore		$3.0 < L \leq 5.0$	2		≤ 7	$W \leq 0.1$	1		-	$W > 0.1$	Follow Round shape			MI	 <p>** : 平均直径 (X + Y)/2</p>
Dimension	Acceptable Q'ty			Remark																																																				
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$\Phi \leq 0.10$	Ignore																																																							
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≤ 7	$W \leq 0.1$	1																																																						
-	$W > 0.1$	Follow Round shape																																																						
3	Newton Ring	<p>a) Regular</p>  <p>Ring area more than 1/3 of screen area: Reject Ring area less than 1/3 of screen area: Accept</p> <p>b) Irregular</p>  <p>Ring area more than 1/2 of screen area: Reject Ring area less than 1/2 of screen area: Accept</p>	MI																																																					

(5.0) Reliability Test

Item	Content
Room Temperature Operation	50,000 hrs

(5.1) Reliability Test - Module Middle Reliability

No.	Item	Condition	Duration	Sample Quantity	Criteria (Acc/Rej)	Note
1	High Temp Operation	70 ± 2℃	120 hrs	3	0/1	
2	High Temp Storage	80 ± 2℃	120 hrs	3	0/1	
3	Low Temp Operation	-20 ± 2℃	120 hrs	3	0/1	
4	Low Temp Storage	-30 ± 2℃	120 hrs	3	0/1	
5	High Temp and High Humidity Storage	60℃, 90% RH	120 hrs	3	0/1	
6	High Temp and High Humidity Operation	60℃, 90% RH	120 hrs	3	0/1	
7	Thermal Shock	-25℃ (0.5h) ↔ 70℃ (0.5h)	20cycle	3	0/1	
8	Packaging Vibration Test	To be measured after subjecting to total fixed amplitude of 1.5mm vibrating frequency 10 to 55Hz, one cycle 60 seconds to direction of X,Y,Z for each 15 minutes,(Total 45minutes) and after removing vibration				
9	Packaging Drop Test	To be measured after dropping from 80cm high onto steel board of 15mm thick and from 6 face				
10	ESD	- Condition:150pf, 330Ω, ±8KV, 5 times Air Discharge (ESD which is made by above condition should be shot on LCD glass panel, not other's area(such as on IC and so on) - After testing, cosmetic and electrical defects should not happen. -Total current consumption should be below double of initial value. -In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.				

(5.2) Criteria

- a. No. 1 ~ 9 : No changes for indication and appearance.
- b. No. 1 ~ 3, 5 ~ 9 : Leave the all samples under room temperature 4 hours after reliability
- c. No. 4 : Leave the all samples under room temperature 12 hours after reliability test ends.

(5.3) Reliability Test - Touch Panel Reliability

No.	项目	条件	时间/次数	样本数量	标准 (Acc/Rej)	备注
1	Pen Sliding	Polyacetal Pen, 150gf 60mm/s frequency	10 ⁵ times	1	0/1	
2	Hitting	Polyacetal Pen, HRR60-80 150gf, 2 times/s frequency	10 ⁶ times	1	0/1	

Model	BTL504885-W640L	33/36	PRODUCT SPECIFICATIONS
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2. Notes on the design and use of touch panel:

- (2.1) Designing the housing, it is recommended to cover the edge of the housing bezel to the between the viewing areas and active areas of touch panel, to protect the bank line of vulnerable areas within the 2 mm region, which shown in figure 1 and figure 2;
- (2.2) Between panel and housing should be leaved by 0.5+/-0.2mm gap with cushion material or other gasket, which shown in figure 2;
- (2.3) In order to prevent suppressing the active area of touch panel by gasket, it should be keep away from the edge of active area more than 1.5mm pitch, which shown in figure 2;
- (2.4) Due to the operating unbearable areas of the edge of the viewing areas, keep your company from testing the touch-screen with pen sliding in the processes of inspection and using, which shown in figure 3.

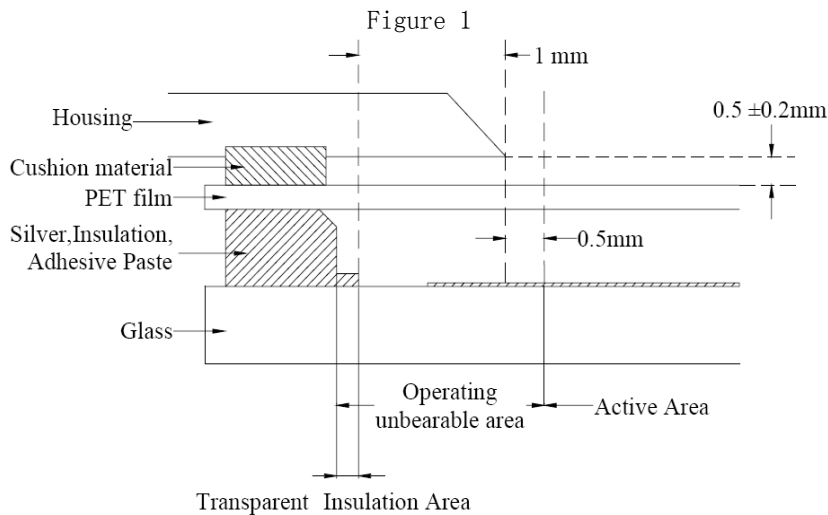
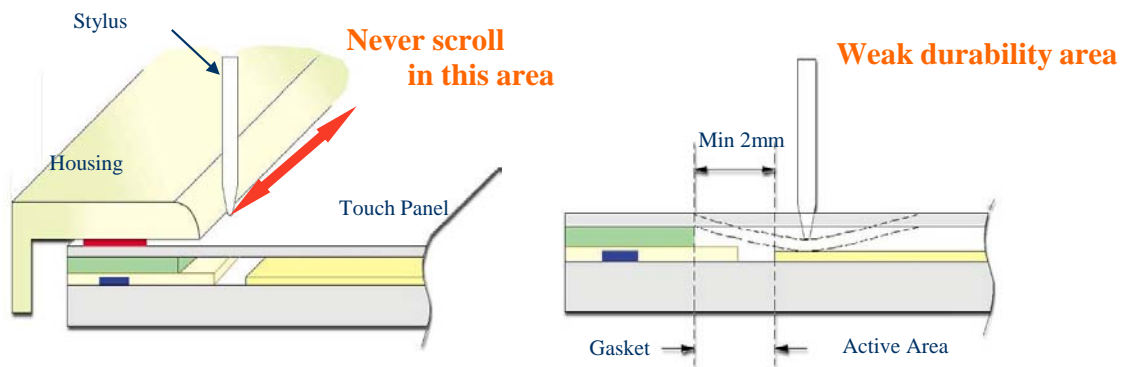


Figure 2

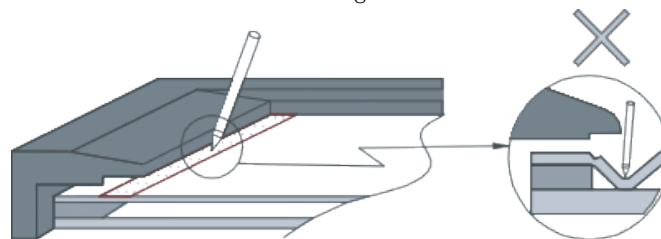


Figure 3

3. BHL&BMDT Customer Quality Service Process

In order to provide better service for Customer, BHL&BMDT shall apply the after-sales product quality service process as below:

- 1> According to the P/O from Customer, BHL&BMDT should deliver required product to the right place appointed by Customer.
- 2> Customer shall apply inspection to the incoming product.
- 3> Inspection standard should be provided by BHL&BMDT, and it will become effective after confirmed by Customer. Inspection and Defects determination should be carried out according to the standard agreed by both Parties.
- 4> In order to guarantee in-time communication of product quality situation and effective service, QA staff on Customer side should send Weekly Quality Report to the appointed CS staff in BHL&BMDT.
- 5> After BHL&BMDT get related information, both sides should arrange time and place to determine the non-performing products found by Customer.
- 6> BHL&BMDT should cooperate with Customer in case of special quality requirement.
- 7> After confirmed by both side, BHL&BMDT should be responsible for the defect part caused by our quality problem. BHL&BMDT take back the confirmed defect products and return normal goods to customer.
- 8> BHL&BMDT agree to provide related training of LCD product technology and usage.
- 9> Customer should use the LCD product according to the instruction. BHL&BMDT will not be responsible for the defect product caused by violation of Users' Instruction.
- 10> Both parties should deal with the quality problem under the principle of mutual consultation and cooperation. And both parties should negotiate to handle the defect products of which the cause isn't clear.

4.LCD Module Operation Instruction

4.1 Cautions for storage

- 1> Avoid hitting the LCD Panel in any way because the LCD is made of glass.
- 2> Physical status of liquid crystal will change under extrem temperature, and it can not be resumed when the temperature returns to normal. So LCD module should be stored in required temperature. Same reason, LCD module should be stored in required humidity. Low humidity may add static, while high humidity may corrode the ITO circuit of LCD product. The suitable storage environment is: temperature: $22\pm 5^{\circ}\text{C}$, humidity: $55\%\pm 10\%$.
- 3> Avoid exposing LCD module under sunshine, strong fluorescence or ultraviolet radiation for a long time. It should be stored in dark area.
- 4> Chemical liquid is forbidden to clean the LCD, such as alcohol, acetone and IPA. Because all of these can do damage to the LCD. Water on the LCD surface must be cleaned as soon as possible, or it will cause POL color change or other defect. It is forbidden that the reflect film of BLU makes contact directly with solder pad of mobile telephone's mainboard, otherwise it is easy to happen corrosion or scratch on reflect film of BLU; please make sure that solder pad of mobile telephone's mainboard is covered with insulation tape.
- 5> LCD products should be stored in static-protective polythene bag under certain requirement.

4.2 Cautions for installing and assembling

- 1> Please make sure that operators wear static-protective bands correctly and working tables are effectively grounded during operation.
- 2> Please place LCD module on the tray provided by BHL&BMDT while moving it, in order to avoid mechanical damage. Hold the module's side frames to avoid damage during moving. Please move and assemble LCD very carefully during assembly, and avoid pushing or twisting it.
- 3> Avoid disassembling LCD module or damage the FPC or permanent defect may happen.
- 4> Avoid cleaning the LCD surface with hard materials. Please clean LCD with Air-gun or very soft cloth when necessary. The protective film on the POL is prohibited to be removed until assembly, otherwise, dust, spit or other foreign matter may fall on the LCD surface. After the protective film is removed, only air-gun can be applied to remove any dust or foreign matter. Fingure or cloth MUST NOT be used in such cases.
- 5> Avoid twisting, disassembling, squeezing or hitting the PCB. It will damage the circuit or component on PCB and cause functional defect.
- 6> Please use the connector according to the instruction provided by BHL&BMDT.
- 7> Please place dual module with the sub-panel upward. Trays should be placed in contrary direction. An empty tray should be placed on the top.
- 8> Sealing operation on PCB must be very careful to avoid short or cutting the original circuit on PCB. Otherwise, permanent damage to the LCD may happen.
- 9> Please take great care to use connector. Defect caused by wrong or careless operation on Customer side are not within the compensation range.

4.3 Cautions for operation

- 1> Avoid adding direct DC or high voltage to LCD panel. It will cause functional damage to the LCD or shorten the life of LCD product.
- 2> LCD may respond slowly or display abnormally in extrem temperature (lower than -20°C or higher than 50°C). But this doesn't mean LCD functional defect. LCD will display normally in regular temperature. Therefore, avoid using LCD product in extrem temperature.
- 3> Avoid pushing the display area of LCD panel which may cause abnormal display. This doesn't mean LCD functional defect, neither. LCD will display normally in regular temperature.
- 4> Electrical inspection for LCD product is carried out by using mobile phone provided by Customer. Special test equipment could be applied under mutual consent.

Model	BTL504885-W640L	36/36	PRODUCT SPECIFICATION
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